Errata on AT91SAM9G45 Engineering Sample Devices

1. Scope

This document describes the known errata found on Atmel's AT91 ARM® Thumb®-based Microntroller series **AT91SAM9G45** device engineering samples with a date code prior to 0927.

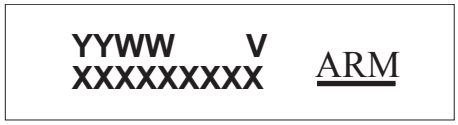
It applies to devices:

- AT91SAM9G45 (with marking: CU-ES)

1.1 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking is as follows:



where

- "YY": manufactory year
- "WW": manufactory week
- "V": revision
- "XXXXXXXXX": lot number

AT91 ARM Thumb-based Microcontrollers

AT91SAM9G45

Errata Sheet

6485A–ATARM–30-Jul-09

2. Errata

2.1 DDRSDRAM Controller (DDRSDRC)

2.1.1 DDRSDRC: DDR2 Multi-port Read Optimization

Read optimization does not work for the multi-port DDR2. This feature is enabled by default in the DDRSDRC_HS register at offset 0x2C in the DDRSDRC user interface.

Problem Fix/Workaround

Read optimization must be disabled by software by setting the DIS_ANTICIP_READ bit.

2.2 Error Corrected Code Controller (ECC)

2.2.1 ECC: Computation with a 1 clock cycle long NRD/NWE pulse

If the SMC is programmed with NRD/NWE pulse length equal to 1 clock cycle, HECC can't compute the parity.

Problem/Fix Workaround

It is recommanded to program SMC with a value superior to 1.

2.3 Internal Memory

2.3.1 ROM Code: SAM-BA® through USB

The connection through USB to the SAM-BA monitor does not work.

Problem Fix/Workaround

Use JTAG or serial port to communicate with SAM-BA monitor.

Note: See the steps described below.

2.3.2 AT91SAM9G45-ES ROM Code Replacement

Procedure to install AT91SAM9G45-ES ROM code replacement:

Prior to any operation, the user needs to install *AT91-ISP.exe 1.13* and unzip *AT91SAM9G45_RomCode_Replacement.zip* file that contains a version of ROM binary code with USB issue fixed. Once done the following steps are necessary to store this version of ROM code in DataFlash.

1. unplug power supply
2. unplug usb device cable
3. remove jumper JP10 (NandFlash Chip Select) & JP12 (DataFlash Chip Select)
4. plug serial cable
5. lauch hyper terminal (115200 bauds, 8 bits, parity none, 1 stop bit, no flow control)
6. plug-in power supply
7. type on hyper terminal : "Alt-0128 Alt-0128 #"
8. AT91SAM9G45-EKES returns ">"
9. close hyper terminal
10. close jumper JP12 (DataFlash® Chip Select)
11. launch SAM-BA (Choose right COM port and AT91SAM9G45-EKES)
12. choose DataFlash media tab in the SAM-BA GUI interface

13. initialize DataFlash, choosing the Enable action in the Scripts rolling menu and press Execute
14. choose Send boot file, press Execute
15. select *AT91SAM9G45_RomCode_Replacement.bin* binary file and press Open; the media is written down
16. close SAM-BA

On Reset, the faulty ROM code will copy the fixed ROM code in SRAM and launch it. The connexion through USB to the SAM-BA monitor will work.

Note: Boot from DataFlash media will no longer be available for other purpose.

2.3.3 ROM Code: SDCARD and MMC boot

SDCARD and MMC boot are not supported.

Problem Fix/Workaround

None

2.4 Image Sensor Interface (ISI)

2.4.1 ISI: Codec Path is diabled

The ISI Codec path is disabled after the capture of each frame and so requires to be enabled before the capture of the next frame. This may lead to discarding some frames if the frame rate is high.

Problem Fix/Workaround

None

2.5 LCD Controller (LCDC)

2.5.1 LCDC: LCD formula to compute LCD Pixel Clock

The LCD formula to compute the LCD pixel clock is system_clock/2*(CLKVAL+1) instead of system_clock/(CLKVAL+1).

Problem Fix/Workaround

None

2.6 High Speed MultiMedia Card Interface (HSMCI)

2.6.1 HSMCI: R1B Busy Timing

Busy line is sampled 2 clock cycles after the command End Bit when the R1B response type is expected.

This timing is not strictly defined in SD mode.

This timing is defined in MMC Specification V4.3. (R1B busy Timing)

Problem/Fix Workaround

The user must poll the D0 (busy line) through the PIO Controller and wait for a rising edge on that line.

2.7 Pulse Width Modulation Controller (PWM)

2.7.1 PWM: Zero Period

It is impossible to update a period equal to 0 by using the PWM_CUPD register.

Problem/Fix Workaround

None

2.8 Reset Controller (RSTC)

2.8.1 RSTC: NRST Signal, input mode not available at startup

The NRST input mode power-up is not available at reset. The NRST mode is output at power-up.

Problem Fix/Workaround

None

2.9 Serial Synchronous Controller (SSC)

2.9.1 SSC: Clock is Transmitted before the SSC is enabled

SSC configuration:

- Performs a SW reset,
- Program the receive and the transmit frame synchro,
- Program the transmit and the receive clock as continuous (CKO = Continuous Receive and Transmit Clock)

=> the clock is transmitted.

Problem Fix/Workaround

Configure PIO lines for SSC usage after first enabling the SSC.

2.9.2 SSC: Last RK Clock Cycle when RK Outputs a Clock during data transfer

When the SSC receiver is used with the following conditions:

- the internal clock divider is used (CKS = 0 and DIV different from 0)
- RK pin set as output and provides the clock during data transfer (CKO = 2)
- data sampled on RK falling edge (CKI = 0)

At the end of the data cycle, the RK pin is set in high impedance which might be seen as an unexpected clock cycle.

Problem Fix/Workaround

Enable the pull-up on RK pin.

2.9.3 SSC: First RK Clock Cycle when RK Outputs a Clock during data transfer

When the SSC receiver is used with the following conditions:

- RX clock is divided clock (CKS = 0 and DIV different from 0)
- RK pin set as output and provides the clock during data transfer (CKO = 2)
- data sampled on RK falling edge (CKI = 0)

The first clock cycle time generated by the RK pin is equal to MCK /(2 x (value +1)).

Problem Fix/Workaround

None.

2.9.4 SSC: Data sent without any frame synchro

When SSC is configured with the following conditions:

- RF is in input,
- TD is synchronized on a receive START (any condition: START field = 2 to 7)
- TF toggles at each start of data transfer
- Transmit STTDLY = 0
- Check TD and TF after a receive START,

The data is sent but there is not any toggle of the TF line

Problem Fix/Workaround

Transmit STTDLY must be different from 0.

2.9.5 SSC: Unexpected delay on TD output

When SSC is configured with the following conditions:

- TCMR.STTDLY more than 0
- RCMR.START = Start on falling edge/Start on Rising edge/Start on any edge
- RFMR.FSOS = None (input)
- TCMR.START = Receive Start

Unexpected delay of 2 or 3 system clock cycles is added to TD output.

Problem Fix/Workaround

None

2.10 USB Host Port (UHP)

2.10.1 UHP: OHCI Mode not functional

The USB Host Port does not work in OHCI mode.

Problem Fix/Workaround

None

2.11 USB High Speed Device Port (UDPHS)

2.11.1 UDPHS and UHPHS shared UTMI transceiver

The switch allowing to share a UTMI transceiver between the host port and the device port works only when switching from host to device. It does not work when switching from device to host.

Problem Fix/Workaround

None

2.12 Universal Synchronous Asynchronous Receiver Transmitter (USART)

2.12.1 USART: RX impossible after any TX in ISO7816 mode T1

Reception is impossible after any transmission in ISO7816 mode T1.

Problem/Fix Workaround

Configure USART in ISO7816 Mode T0 + INACK = 1 in US_MR during the reception. Once reception is done, i.e. when the PDC Interruption ENDRX is received, reconfigure the USART in Mode T1 in US_MR prior to transmitting.

2.12.2 USART: Bad value in Number of Errors Register

The Number of Errors Register (US_NER) always returns 0 instead of the ISO7816 error number.

Problem/Fix Workaround

None

Revision History

Doc. Rev	Comments	Change Request Ref.
6485A	First issue	

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