8-bit MCU & LCD Dot Matrix Controller

1. Features

- 8-bit MCU C51 core based (See TEMIC 8-bit Microcontrollers Databook)
- 512 bytes of internal RAM
- 32K bytes of internal ROM/OTP
- Four 8-bit I/O Ports
  - Two General Purpose Ports (P0 and P2)
  - P0, P1, P2 and P3 can drive LEDs (but 24 max can be used simultaneously)
- Three specific 8-bit Ports
  - Two 8-bit Keyboard scan Ports (P5 and P6)
  - One specific port (P4)
    - 4-bit Keyboard read Port (p4.0 to P4.3)
    - 2 comparator input (P4.4 and P4.5)
    - 2 general purpose bit (P4.6 and P4.7) which can drive LEDs
- Three 16-bit Timers/Counters
  - Timer 0, 1 and 2 of the standard 80C51
- Serial I/O Port (UART)
  - Internal Baud Rate Generator
- Power Monitoring and Management
  - Double Crystal inputs for speed and low current application
- Dual Data Pointer
- Watchdog Timer
- PCA (2 channels)
- I2C
- SPI
  - Master/Slave mode
- LCD Display Controller Driver
  - Capable of displaying 1 line or 2 lines of up to 24 characters, or 2 or 4 lines of up to 12 characters
    - 5x7 character format plus cursor; 5x8 for kana and user defined symbols
    - 60 segments, 34 commons and 60 icons
  - Direct programming of the special character patterns by Character Generator RAM
    - Character Generator RAM : 1024 bits (16 characters)
    - Character Generator ROM : 9600 bits (240 characters)
    - Display Data RAM : 640 bits (80 characters)
    - Segment Data RAM : 128 bits (60 icons max)
  - Mux rate 1:17 and 1:33
  - Programmable LCD voltage
  - 2 Voltage comparators e.g. for LCD voltage adaption to temperature variations
  - LCD active in power save mode
- Power fail management
- Up to 33MHz at 5V±10% and
  Up to 12MHz at 3V ±10%
- Die form and TQFP176 package
- Power supply V_{DD} : 3V±10% to 5V ±10%
- Temperature range: commercial (0 to 70 ^{o}C)

2. Description

The PAROS is a display oriented microcontroller based on a C51 compatible core including a LCD display controller/driver, keyboard control and LED drivers.
The PAROS provides all features for most embedded applications needing low-power LCD controller and driver designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters, or 2 or 4 lines by 12 characters with 5x8 dot format. All necessary functions for the LCD display are provided by this component with a combined LCD/Keyboard scan port and up to 34 LED drives. For acoustical signals, the buzzer function is programmable in a wide frequency range. All LED drives support 10mA sink current.

Large applications can also be designed with Paros like portable equipments thanks to its low power consumption capability and its “on-board” features like timers and general purpose I/Os. A Clock switching mechanism to the second low frequency oscillator e.g. 32KHz during idle mode permits to minimize current consumption while the MCU is running. To save more power, the Power-down mode can be also selected i.e. in this

configuration the clock is only provided to the LCD controller. It is possible to stop the Power-down mode by an external interrupt or by a keyboard interrupt.
Three serial interfaces are available to communicate with other applications: the standard USART which can handle a large panel of baud rates with its own baud rate generator and the SPI and I2C able to act as slave or master.

3. alias SFR Mapping

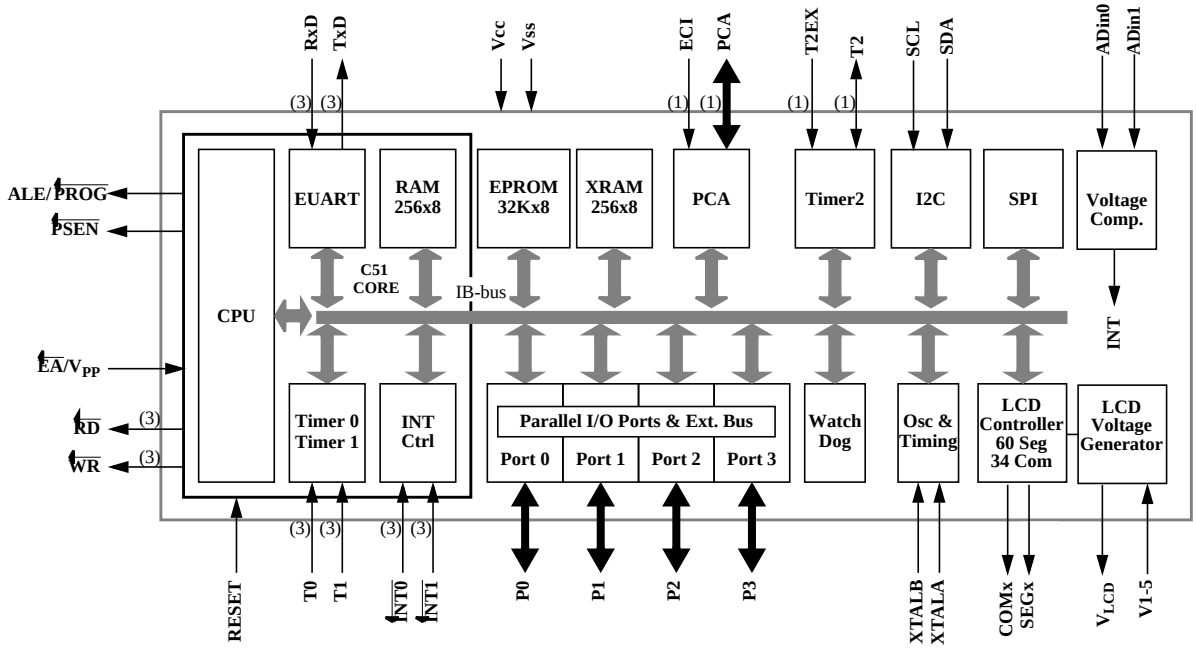
The Special Function Registers (SFRs) of the PAROS belongs to the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3, P4, KB0, KB1
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON, BRL, BDRCON
- Power and clock control registers: CKSEL, OSCCON, PCON, CKRL
- Interrupt system registers: IE, IE1, IPL0, IPL1, IPH0, IPH1, P4F, P4IE
- WatchDog Timer: WDTRST, WDTPRG
- LCD Controller: LCDCON, LCDAC, LCDIR, LCDDR, LCDPS
- I2C: SSCON, SSCS, SSDAT, SSADR
- SPI: SPCR, SPSCR, SPDR
- PCA: CCAP0L, CCAP1L, CCAP0H, CCAP1H, CCAPM0, CCAPM1, CL, CH, CMOD, CCON
- Others: AUXR, AUXR1, COMCON

Table 1. SFR Addresses and Reset Values

	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8h	*KB1/P6* *1111 1111*	*CH* *0000 0000*	*CCAP0H* *XXXX XXXX*	*CCAP1H* *XXXX XXXX*					*FFh*
F0h	*B* *0000 0000*								*F7h*
E8h	*KB0/P5* *1111 1111*	*CL* *0000 0000*	*CCAP0L* *XXXX XXXX*	*CCAP1L* *XXXX XXXX*					*EFh*
E0h	*ACC* *0000 0000*			*LCDCON* *0000 0000*	*LCDPS* *0000 0000*	*LCDAC* *0000 0000*	*LCDIR* *0000 0000*	*LCDDR* *0000 0000*	*E7h*
D8h	*CCON* *00XX XX00*	*CMOD* *0XXX X000*	*CCAPM0* *0000 0000*	*CCAPM1* *0000 0000*					*DFh*
D0h	*PSW* *0000 0000*								*D7h*
C8h	*T2CON* *0000 0000*	*T2MOD* *XXXX XX00*	*RCAP2L* *0000 0000*	*RCAP2H* *0000 0000*	*TL2* *0000 0000*	*TH2* *0000 0000*			*CFh*
C0h	*IE1* *XXXX X000*			*SPCR* *0001 0100*	*SPSCR* *0000 0000*	*SPDR* *XXXX XXXX*			*C7h*
B8h	*IPL0* *X000 000*	*SADEN* *0000 0000*							*BFh*
B0h	*P3* *1111 1111*	*P4* *1111 111*	*IPL1* *XXXX X000*	*IPH1* *XXXX X000*				*IPH0* *X000 0000*	*B7h*
A8h	*IE* *0000 0000*	*SADDR* *0000 0000*							*AFh*
A0h	*P2* *1111 1111*		AUXR1 XXXX XXX0	COMCON 0100 0100			*WDRST* *0000 0000*	*WDTPRG* *0000 0000*	*A7h*
98h	*SCON* *0000 0000*	*SBUF* *XXXX XXXX*	*BRL* *0000 0000*	*BDRCON* *0XXX 0000*		*P4IE* *XXXX 0000*	*P4F* *XXXX 0000*		*9Fh*
90h	*P1* *1111 1111*			*SSCON* *0000 0000*	*SSCS* *1111 1000*	*SSDAT* *1111 1111*	*SSADR* *1111 1110*	*CKRL* *1111 1111*	*97h*
88h	*TCON* *0000 0000*	*TMOD* *0000 0000*	*TL0* *0000 0000*	*TL1* *0000 0000*	*TH0* *0000 0000*	*TH1* *0000 0000*	*AUXR* *XXXX XXX0*		*8Fh*
80h	*P0* *1111 1111*	*SP* *0000 0111*	*DPL* *0000 0000*	*DPH* *0000 0000*		*CKSEL* *XXXX X000*	*OSCCON* *XXXX X001*	*PCON* *00X1 0000*	*87h*
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

4. Block Diagram



(1): Alternate function of Port 1

(3): Alternate function of Port 3

Figure 1. Paros Block Diagram

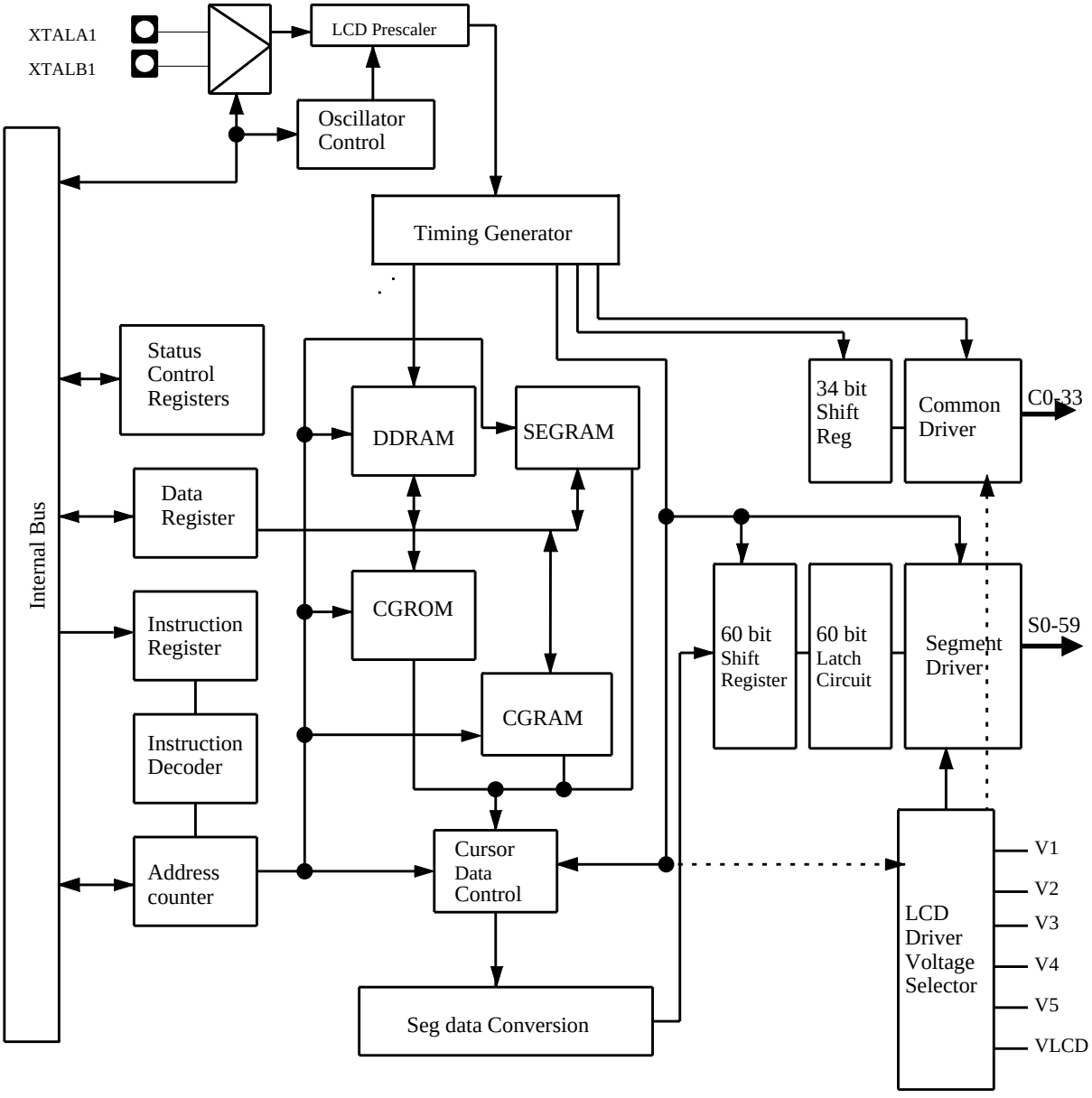


Figure 2. LCD Controller Driver Diagram

5. Pin Configuration

Table 2. Pin Description

Pin Name	Type	Description
VSS	GND	Circuit ground potential. (4 Vss buffers)
VCC		Supply voltage during normal, idle, and power-down operation. (4 Vcc buffers)
V1:5/Vlcd		LCD Voltage Generator and Bias Voltage Inputs.
P0.0:7	I/O	Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the data bus during accesses to external Data Memory. In this application it uses strong internal pull-ups when emitting 1's. Each Port 0 pin can sink 10 mA* for direct drive of LEDs. Port 0 is used as data bus during EPROM programming and program verification.
P1.0:7	I/O	Port 1 is an 8 bit bi-directional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, in the DC section) because of the internal pull-ups. Port 1 can sink /source 3 LS TTL inputs. It can drive CMOS inputs without external pull-ups. Port 1 can sink 10 mA* on each pin for direct drive of LED. Port1 also serves the functions of the following special features of Paros as listed below: Port Pin Alternate Function P1.0 T2 Timer/Counter 2 external count input/clockout P1.1 T2EX/$\overline{SS}$ Timer/Counter 2 reload/capture/direction control/ SPI Slave Selection. $\overline{SS}$ = 0 slave, $\overline{SS}$ = 1 master P1.2 ECI External Counter Input for PCA module P1.3 CEX0 Compare/Capture Input for module 0 P1.4 CEX1/ Compare/Capture Input for module 1 P1.5 MISO SPI master input Slave output P1.6 SPSCK clock/SPI & serial clock, output for master, input for slave. P1.7 MOSI synchronous serial link data & SPI master output, Slave Input Port 1 receives the low-order address byte during EPROM programming and program verification.
P2.0:7	I/O	Port 2 is an 8 bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, in the DC section) because of the internal pull-ups. Port 2 can sink 10 mA* on each pin for direct drive of LED. It can drive CMOS inputs without external pull-ups. Some Port 2 pins receive the high-order address bits and control signals during EPROM programming and program verification.
P3.0:7	I/O	Port 3 is an 8 bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, in the DC section) because of the pull-ups. Port 3 can sink 10 mA* on each pin for direct drive of LED. Port 3 also serves the functions of various special features of the TEMIC's C51 Family, as listed below: Port Pin Alternate Function P3.0 RxD Serial port input P3.1 TxD Serial port output P3.2 $\overline{INT0}$ (external interrupt 0) P3.3 $\overline{INT1}$ (external interrupt 1) P3.4 T0 timer 0 external input P3.5 T1 timer 1external input P3.6 $\overline{WR}$ external Data Memory write strobe P3.7 $\overline{RD}$ external Data Memory read strobe Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pull-ups. Some Port 3 pins receive control signals during EPROM programming and program verification.
P4.0:7	I/O	Port 4 is a specific port. P4.0 to 4.3: Keyboard controller with interrupt capability P4.4 and P4.5: comparator input P4.6 and P4.7: 2 general purpose specially designed to strongly drive important loads and to be able to provide up to 10mA* per port bit line. The pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (IIL, in the DC section) because of the pull-ups.
P5.0:7/S0:7	O	Port 5 is an 8 bit Output port dedicated for Keyboard scan. Port 5 is also multiplexed with the LCD Segment control S0-S7.

Table 2. Pin Description

Pin Name	Type	Description
P6.0:7/S8:15	O	Port 6 is an 8 bit Output port dedicated for Keyboard scan. Port 6 is also multiplexed with the LCD Segment control S8-S15.
S16:S59	O	Dedicated LCD Segment driver for Segments S16 to S59.
C0:33	O	Dedicated LCD Common driver for Commons C0:33.
SCL	I/O	I2C Serial Clock
SDA	I/O	I2C Serial Data
RST	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-on reset using only a capacitor connected to V_{CC}. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is started or not (asynchronous reset).
ALE/$\overline{PROG}$	I/O	Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without external pull-up. If desired, to reduce EMI, ALE operation can be disabled by setting bit 0 of SFR location 8Eh (AUXR). With this bit set, the pin is weakly pulled high. However, ALE remains active during MOVX, MOVC instructions and external fetches. Setting the ALE disable bit has no effect if the microcontroller is in external execution mode ($\overline{EA}$=0).
PSEN	O	Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of $\overline{PSEN}$ are skipped during each access to external Data Memory). $\overline{PSEN}$ is not activated during fetches from internal Program Memory. $\overline{PSEN}$ can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pull-up.
$\overline{EA}$/VPP	I/O	External Access enable. EA must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000h to FFFFh. Note however, that if any of the Security bits are programmed, $\overline{EA}$ will be internally latched on reset. $\overline{EA}$ should be strapped to V_{CC} for internal program execution. This pin also receives the programming supply voltage (VPP) during EPROM programming.
XTALA1	I	Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.
XTALA2	O	Output from the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.
XTALB1	I	Input to the inverting amplifier that forms the oscillator. Receives the second external oscillator signal when a second external oscillator is used to minimize consumption in Idle mode.
XTALB2	O	Output from the inverting amplifier that forms the second oscillator. This pin should be floated when an external oscillator is used.

* Maximal 24 LEDs are permitted and max. 4 can be switched by the same instruction.

6. CLOCK

6.1 Overview

This core is monophase, edge sensitive .
Two oscillators are available for CPU :

- OSCA used for high frequency : Upto 33MHZ @5V +/- 10%
- OSCB used for slow frequency : 32.768KHZ

Several operating modes are available and programmable by software :

- to switch for OSCA to OSCB and vice-versa
- to stop OSCA and/or OSCB to reduce consumption

In order to optimize the power consumption and the execution time needed for a specific task, an internal prescaler feature has been implemented between the selected oscillator and the CPU .

A third oscillator OSCC (internal) is dedicated for display controller only and can be switched off by software too.

6.2 Registers :

Table 3. CKSEL (85h)
Reset value : XXXXX100b
Located in MISC block

7	6	5	4	3	2	1	0
-	-	-	-	-	**RSTD**	**CKS1**	**CKS0**

Bit Number	Mnemonic	Description
7		**Reserved**
6		**Reserved**
5		**Reserved**
4		**Reserved**
3		**Reserved**
2	RSTD	Reset Detector Disable Bit
1	CKS1	**Cpu Ocillator Select Bit : (CkCpuBAb)** When cleared, Cpu and peripherals connected to OSCA When set, Cpu and peripherals connected to OSCB Cleared by hardware after a Power-up (OSCA selected by default)
0	CKS0	**Cpu Ocillator Select Bit : (CkCpuBCb)** When cleared, LCD controller connected to OSCC When set, LCD controller connected to OSCB Cleared by hardware after a Power-up (OSCC selected by default)

Table 4. OSCCON (86h):
Reset value : XXXXX001b

7	6	5	4	3	2	1	0
-	-	-	-	-	OscCEn	OscBEn	OscAEn

Bit Number	Mnemonic	Description
7		**Reserved**
6		**Reserved**
5		**Reserved**
4		**Reserved**
3		**Reserved**
2	OscCEn	**OscC enable bit** Set by software to run OscC Cleared by software to stop OscC Cleared by hardware after a Power-up
1	OscBEn	**OscB enable bit** Set by software to run OscB Cleared by software to stop OscB Cleared by hardware after a Power-up
0	OscAEn	**OscA enable bit** Set by software to run OscA Cleared by software to stop OscA Set by hardware after a Power-up

Table 5. CKRL (97h)
Reset value : 11111111b

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Mnemonic	Description
7:0	CKRL	**Clock Reload Register :** Prescaler value

Table 6. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

6.3 Functional Block diagram

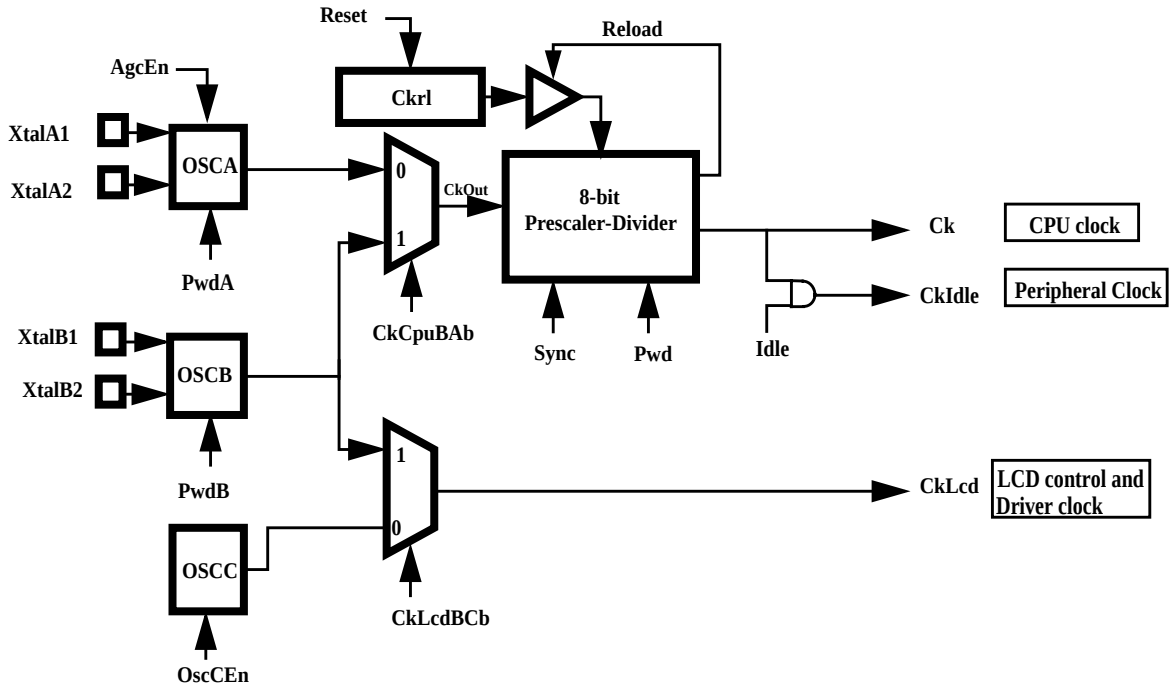


Figure 3. Functional block diagram

6.4 Operating modes

6.4.1 Reset

- An hardware RESET put the Clock generator in the following state :
  - OscAEn = 1 & OscBEn = 0: OscA is running, OSCB is stopped .
  - OscCEn = 1: OSCC is stopped .
  - CkCpuBAb = 0 : OSCA is selected for CPU .
  - CkLcdBCb = 0: OSCC is selected for LCD controller .
- Sync signal is used for tester synchronization and provided by the dedicated test mode .

6.4.2 Functional modes :

6.4.2.1 NORMAL MODES :

- CPU and Peripherics clock depend on the software selection using CKCON and CKRL registers
  - CkCpuBAb bit selects either OSCA or OSCB
  - CKRL register determines the frequency of the selected clock
  - It is always possible to switch dynamicly by software from OSCA to OSCB , and vice versa by changing CkCpuBAb bit, a synchronization cell allowing to avoid any spike during transition .

6.4.2.2 IDLE MODES :

- IDLE modes are achieved by using any instruction that writes into PCON.0 sfr
- IDLE modes A and B depend on previous software sequence, prior to writing into PCON.0 register :

- IDLE MODE A : OSCA is running (OscAEn = 1) and selected (CkCpuBAb = 0)
- IDLE MODE B: OSCB is running (OscBEn = 1) and selected (CkCpuBAb = 1)
- The unused oscillator OSCA or OSCB can be stopped by software by clearing OscAEn or OscBEn respectively .

- IDLE mode can be canceled either by Reset , or by activation of any enabled interruption
  - In both case, PCON.0 is cleared by hardware
  - Exit from IDLE modes will leave Ocillators control bits inchanged (OscEnA,OscEnB,CkCpuBAb)

6.4.2.3 POWER DOWN MODES :

- POWER DOWN modes are achieved by using any instruction that writes into PCON.1 sfr
- POWER DOWN modes A and B depend on previous software sequence, prior to writing into PCON.1 register :
  - If CkLcdBCb = 1, then only OSCA will be stopped , OSCB can be used by Lcd
  - If CkLcdBCb = 0, then both OSCA and OSCB will be stopped, OSCC can be used by Lcd
- POWER DOWN mode can be cancelled either by an harware Reset, by an external interruption, or by the keyboard .
  - By ResetB signal : The CPU will restart in NORMAL mode A .
  - By interruptions INT0 or INT1 interruptions , if enabled : standard behavorial, request on Pads must be driven low enough to ensure correct restart of the oscillator which was selected when entering in Power down .
  - By keyboard in enabled : a hardware clear of the PCON.1 flag ensure the restart of the oscillator which was selected when entering in Power down .

6.4.2.4 Overview :

Table 7. Control clocks configurations

PCON.1	PCON.0	OscCEn	OscBEn	OscAEn	CkLcdBbC	CkCpuBAb	Selected Mode	Comment
0	0	X	0	1	X	0	NORMAL MODE A, OSCB stopped	Default mode after power-up or Warm Reset
0	0	X	1	1	X	0	NORMAL MODE A, OSCB running	Same + OSCB running
0	0	X	1	0	X	1	NORMAL MODE B, OSCA stopped	OSCB running and selected
0	0	X	1	1	X	1	NORMAL MODE B, OSCA running	Same + OSCA running
X	X	X	0	0	X	X	INVALID	OSCA & OSCB cannot be stopped at the same time
X	X	X	X	0	X	0	INVALID	OSCA must not be stopped , as used for CPU and peripherics
X	X	X	0	X	X	1	INVALID	OSCB must not be stopped as used for CPU and peripherics
0	1	X	X	1	X	0	IDLE MODE A	The CPU is off, OSCA supplies the peripherics OSCB can be disabled (OscBEn = 0)
0	1	X	1	X	X	1	IDLE MODE B	The CPU is off, OSCB supplies the peripherics, OSCA can be disabled (OscAEn = 0)
1	X	X	X	1	0	X	POWER DOWN MODE A	The CPU and peripherics are off, but OSCB is still running for Lcd
1	X	0	X	X	1	X	TOTAL POWER DOWN	The CPU is off, OSCA and OSCB are stopped OSCC in stopped
1	X	1	X	X	1	X	PAUSE	The CPU is off, OSCA and OSCB are stopped Lcd is supplied by OSCC
X	X	X	0	X	0	X	INVALID	OSCB must not be stopped as used by Lcd

6.5 Design considerations

6.5.1 Oscillators control :

- PwdOscA and PwdOscB signals are generated in the Clock generator and used to control the hard blocks of oscillators A and B .
- PwdOscA = ’1’ stops OSCA
- PwdOscB = ’1’ stops OSCB
- The following tables summarize the 1.6 paragraph concerning Operating modes :

Table 8. OSCA control

PCON.1	OscAEn	PwdOscA	Comments
0	1	0	OSCA running
1	X	1	OSCA stopped by Power-down mode
0	0	1	OSCA stopped by clearing OscAEn

Table 9. OSCB control

PCON.1	OscBEn	CkLcdBCb	PwdOscB	Comments
0	1	X	0	OSCB running
1	1	0	0	Although PCON.1 is set, OSCB cannot be stopped , as used by Lcd
1	X	1	1	OSCB stopped by Power-down mode
0	0	X	1	OSCB stopped by clearing OscBEn

Table 10. OSCC control

OscCEn	PwdOscC	Comments
1	0	OSCC running
0	1	OSCC stopped by clearing OscCEn

6.5.2 Prescaler Divider :

- An hardware RESET put the precaler divider in the following state :
  - CKRL = FFh : internal clock = FoscA/2 (Standard C51 feature)
- CkCpuBAb signal selects OSCA or OSCB : Fosc = FoscA or FoscB
- Any value between FFh downto 00h can be written by software into CKRL sfr in order to divide frequency of the selected oscillator :
  - CKRL = 00h : minimum frequency = Fosc/512
  - CKRL = FFh : maximum frequency= Fosc/2 (Standard C51 feature)

7. Timer 2

The timer 2 in the PAROS is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 11.) and T2MOD register (See Table 12.). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/6$ (timer operation) or external pin T2 (counter operation) as the timer register input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 includes the following enhancements:

- Auto-reload mode (up or down counter)
- Programmable clock-output

7.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. This feature is controlled by the DCEN bit in T2MOD register (See Table 12.). Setting the DCEN bit enables timer 2 to count up or down as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

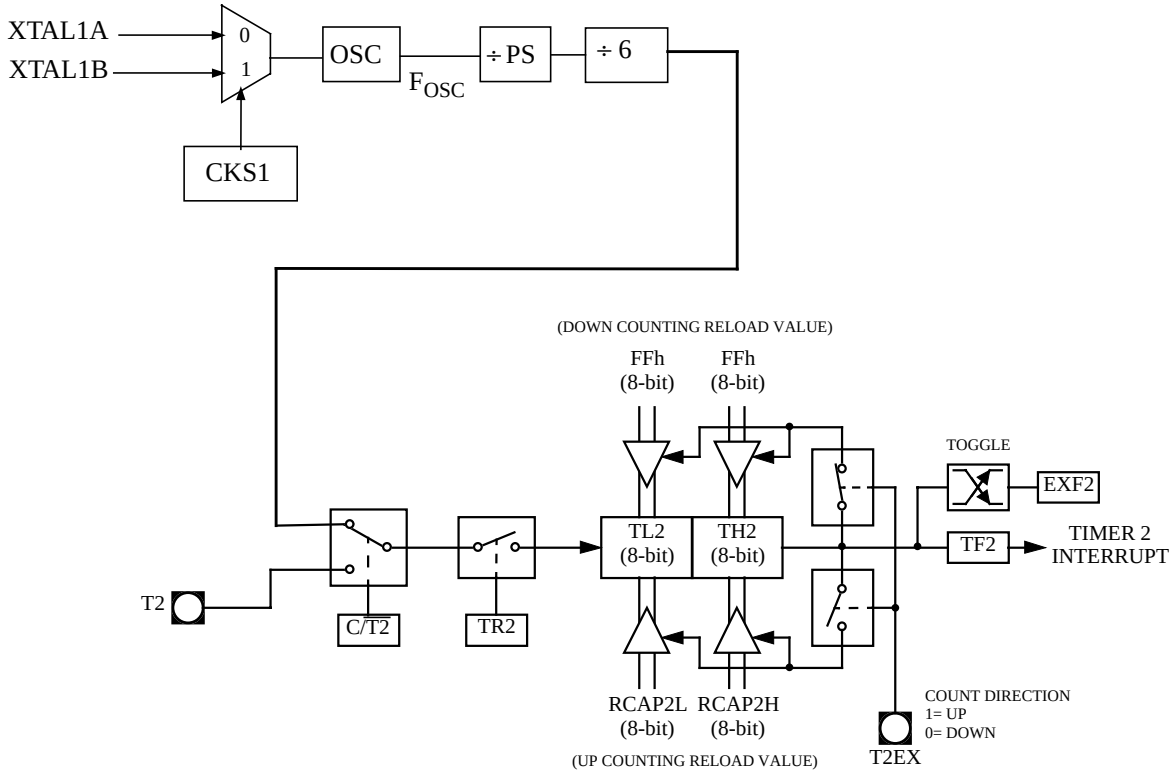


Figure 4. Auto-Reload Mode Up/Down Counter

7.2 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5.) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

$$Clock-OutFrequency = \frac{F_{OSC}}{4 \times (65536 - RCAP2H/(RCAP2L)} \times \frac{1}{(256 - PS)}$$

PS is the oscillator prescalar

For a 16 MHz system clock with Prescalar value PS=255, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{18)}$ to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

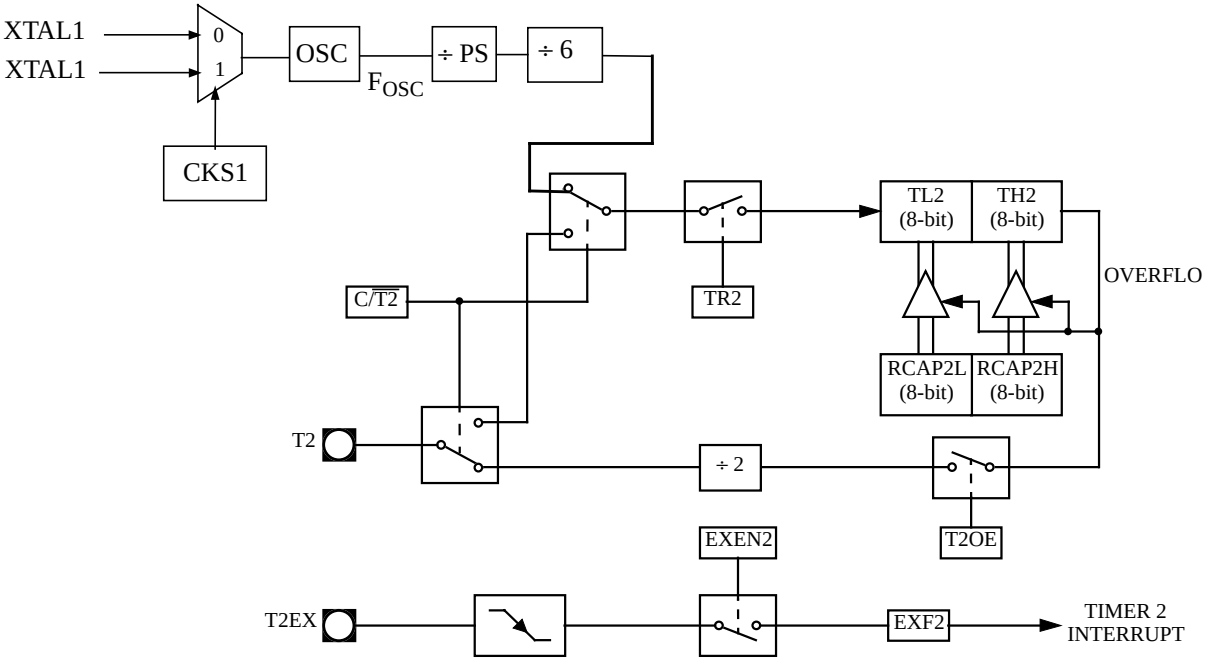


Figure 5. Clock-Out Mode

Table 11. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer 2 overflow.
6	EXF2	**Timer 2 External Flag** Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. Set to cause the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software.
5	RCLK	**Receive Clock bit** Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	**Transmit Clock bit** Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	**Timer 2 External Enable bit** Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	**Timer 2 Run control bit** Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	**Timer/Counter 2 select bit** Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T2 input pin).
0	CP/RL2#	**Timer 2 Capture/Reload bit** If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b
Bit addressable

Table 12. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b
Not bit addressable

8. Serial I/O Port

The serial I/O ports in the PAROS is entirely compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection and Automatic Address Recognition
- Internal Baud Rate Generator

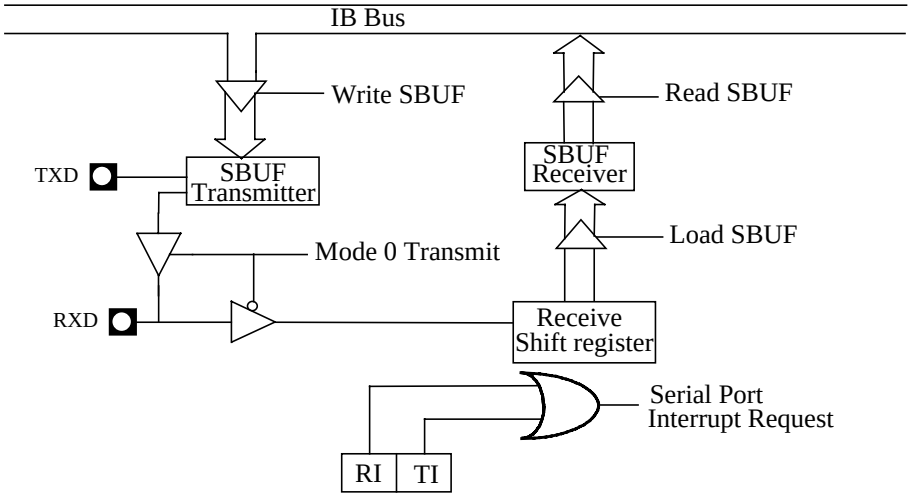


Figure 6. Serial I/O UART Port Block Diagram

8.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Table 19.).

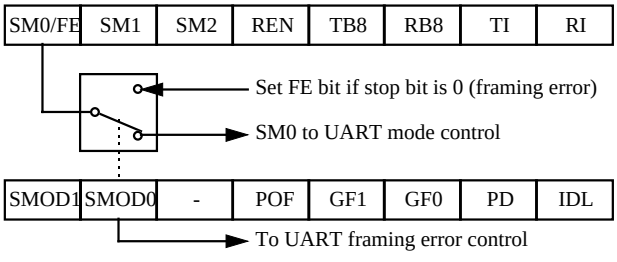


Figure 7. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 8. and Figure 9.).

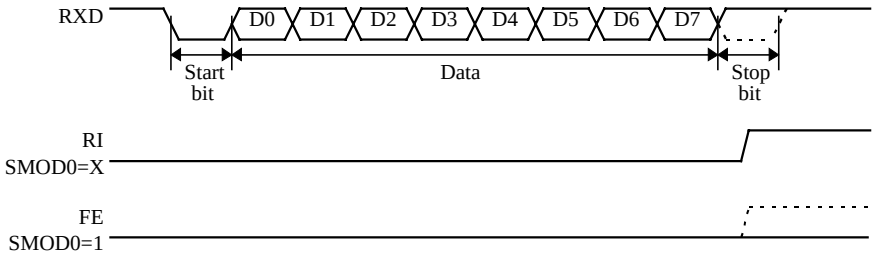


Figure 8. UART Timings in Mode 1

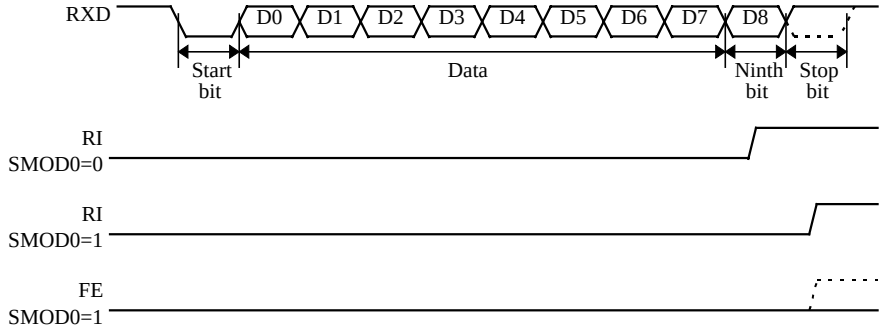


Figure 9. UART Timings in Modes 2 and 3

8.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).
Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.
If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.
To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

8.2.1 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b.
For example:

```
SADDR 0101 0110b
SADEN 1111 1100b
Given 0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A: SADDR 1111 0001b
       SADEN 1111 1010b
       Given 1111 0X0Xb

Slave B: SADDR 1111 0011b
       SADEN 1111 1001b
       Given 1111 0XX1b

Slave C: SADDR 1111 0010b
       SADEN 1111 1101b
       Given 1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed seFG_Lefttely.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).
For slave A, bit 1 is a 0; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves A and B, but not slave C, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

8.2.2 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR       0101 0110b
SADEN       1111 1100b
SADDR OR SADEN 1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A: SADDR 1111 0001b
       SADEN 1111 1010b
       Given 1111 1X11b,

Slave B: SADDR 1111 0011b
       SADEN 1111 1001b
       Given 1111 1X11B,

Slave C: SADDR=1111 0010b
       SADEN 1111 1101b
       Given 1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

8.2.3 Reset Addresses

On reset, the SADDR, SADEN register are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

8.3 Baud Rate Selection for UART

The Baud Rate Generator for transmit and receive clocks can be selected separately via the BDRCON register.

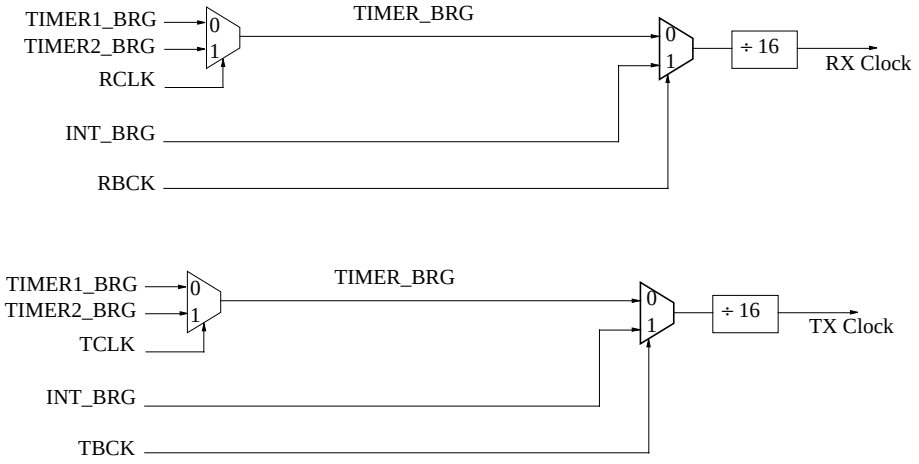


Figure 10.

8.4 Internal Baud Rate Generator (BRG)

When the internal Baud Rate Generator is used, the Baud Rates are determined by the BRG overflow, the value of SPD bit (Speed Mode) in BRCON register and the value of the SMOD1 bit in PCON register:

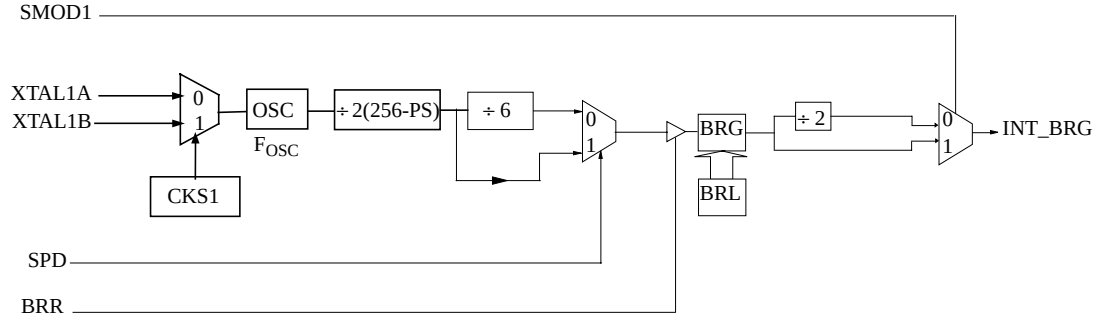


Figure 11. Internal Baud Rate

PS is the oscillator prescalar

- SPD = 1

$$BaudRate = \frac{2^{SMOD1} \times F_{XTAL}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times [256-(BRL)]} \times \frac{1}{(256-PS)}$$

$$BRL = 256 - \frac{2^{SMOD1} \times F_{XTAL}}{64 \times BaudRate} \times \frac{1}{(256-PS)}$$

PS is the oscillator prescalar

- SPD = 0 (Default Mode)

$$BaudRate = \frac{2^{SMOD1} \times F_{XTAL}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times [256-(BRL)]} \times \frac{1}{(256-PS)}$$

$$BRL = 256 - \frac{2^{SMOD1} \times F_{XTAL}}{384 \times BaudRate} \times \frac{1}{(256-PS)}$$

Table 13. Example of computed value when PS=FFh, SMOD1=0, SPD=0

Baud Rates	F_{XTAL} = 16.384 MHz		F_{XTAL} = 24MHz	
	BRL	Error (%)	BRL	Error (%)
4800	247	1.25	243	0.16
2400	238	1.25	230	0.16
1200	220	1.25	202	0.37
600	185	0.16	152	0.16

PS is the oscillator prescalar

Table 14.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 15.

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 16.

SBUF - Serial Buffer Register (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

Table 17.

BRL - Baud Rate Reload Register (9Ah) for UART

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 18. SCON Register

SCON (S:98h)
Serial Control Register

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit**. To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.
	SM0	**Serial Port Mode bit 0**. To select this function, clear SMOD0 bit in PCON register. Software writes to bits SM0 and SM1 to select the Serial Port operating mode. Refer to SM1 bit for the mode selections.
6	SM1	**Serial Port Mode bit 1.** To select this function, set SMOD0 bit in PCON register. Software writes to bits SM1 and SM0 to select the Serial Port operating mode. SM0SM1 Mode DescriptionBaud Rate 0 0 0Shift RegisterF_{OSC}/12 or variable if SRC bit in BDRCON is set 0 1 18-bit UARTVariable 1 0 29-bit UARTF_{OSC}/32 or F_{OSC}/64 1 1 39-bit UARTVariable
5	SM2	**Serial Port Mode bit 2** Software writes to bit SM2 to enable and disable the multiprocessor communication and automatic address recognition features. This allows the Serial Port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN	**Receiver Enable bit** Clear to disable reception in mode 1, 2 and 3, and to enable transmission in mode 0. Set to enable reception in all modes.
3	TB8	**Transmit bit 8** Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.
2	RB8	**Receiver bit 8** Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.
1	TI	**Transmit Interrupt flag** Set by the transmitter after the last data bit is transmitted. Must be cleared by software.
0	RI	**Receive Interrupt flag** Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.

Reset Value= 0000 0000b

Table 19. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X0 0000b
Not bit addressable

Table 20. BDRCON Register

BDRCON - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	**BRR**	**TBCK**	**RBCK**	**SPD**	**SRC**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	BRR	**Baud Rate Run Control bit** Clear to stop the Baud Rate. Set to start the Baud Rate.
3	TBCK	**Transmission Baud rate Generator Selection bit for first UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for first UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for first UART** Clear to select the SLOW Baud Rate Generator when SRC=1. Set to select the FAST Baud Rate Generator when SRC=1.
0	SRC	**Baud Rate Source select bit in Mode 0 for first UART** Clear to select $F_{OSC}/12$ as the Baud Rate Generator. Set to select the internal Baud Rate Generator.

Reset Value = XXX0 0000b

9. Interrupt System

The PAROS has a total of 10 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), serial port interrupt, PCA, keyboard interrupt (P4.x), SPI and I2C. These interrupts are shown in Figure 12..

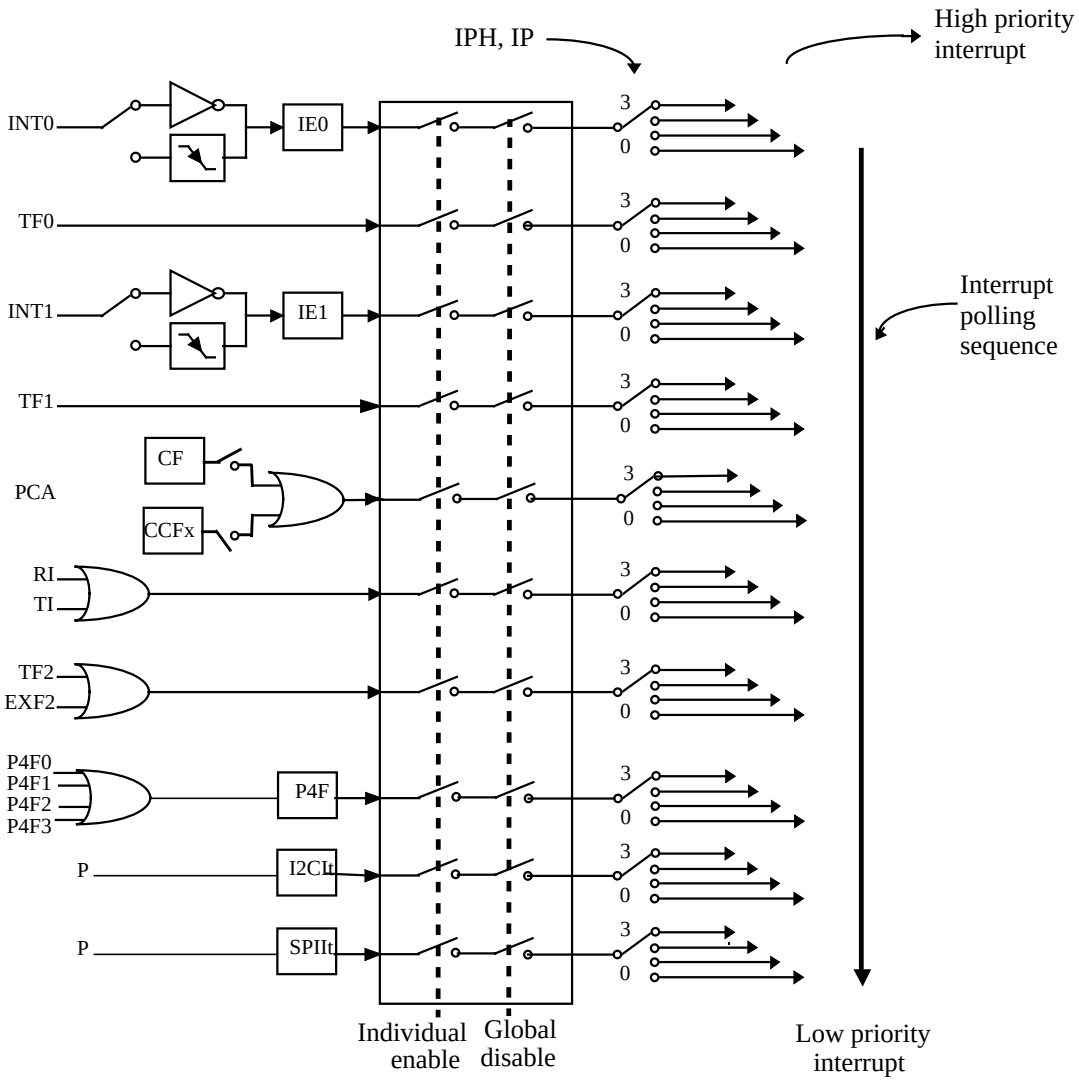


Figure 12. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 22.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 24.) and in the Interrupt Priority High register (See Table 26.). Table 21. shows the bit values and priority levels associated with each combination.

Table 21. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 22. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**EC**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	EC	**PCA Interrupt Enable** Clear to disable the the PCA interrupt. Set to enable the the PCA interrupt.
5	ET2	**Timer 2 overflow interrupt Enable bit** Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b
Bit addressable

Table 23. IE1 Register

IE1 (S:C0h)
Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	-	-	-	**SPI**	**I2C**	**KBIE**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	SPI	**SPI Interrupt Enable bit** Clear to disable the SPI interrupt. Set to enable the SPI interrupt.
1	I2C	**I2C Interrupt Enable bit** Clear to disable the I2C interrupt. Set to enable the I2C interrupt.
0	KBIE	**Keyboard Interrupt Enable bit** Clear to disable the Keyboard interrupt. Set to enable the Keyboard interrupt.

Reset Value = XXXX X000b
No Bit addressable

Table 24. IPL0 Register

IPL0 - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPC	**EWC Counter Interrupt Priority bit** Refer to PPCH for priority level
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X000 0000b
Bit addressable.

Table 25. IPL1 Register

IPL1 - Interrupt Priority Low Register 1 (S:B2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	**PSPI**	**PI2C**	**PKB**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPI	**SPI Interrupt Priority level less significant bit.** Refer to PSPIH for priority level.
1	PI2C	**I2C Interrupt Priority level less significant bit.** Refer to PI2CH for priority level.
0	PKB	**Keyboard Interrupt Priority level less significant bit.** Refer to PKBH for priority level.

Reset Value = XXXX XXX0b
Not Bit addressable.

Table 26. IPH0 Register

IPH0 - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**EWC-PCA Counter Interrupt Priority level most significant bit** PPCH PPC Priority level 0 0 Lowest 0 1 1 0 1 1 Highest priority
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X000 0000b
Not bit addressable

Table 27. IPH1 Register

IPH1 - Interrupt Priority High Register 1 (B3h)

7	6	5	4	3	2	1	0
-	-	-	-	-	**PSPIH**	**PI2CH**	**PKBH**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIH	**SPI Interrupt Priority level most significant bit** PSPIH PSPI Priority level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PI2CH	**I2C Interrupt Priority level most significant bit** PI2CH PI2C Priority level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PKBH	**Keyboard Interrupt Priority level most significant bit** PKBH PKB Priority level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XXXX X000b
Not bit addressable

Table 28. P4IE Register

P4IE - Port 4 Interrupt Enable Register (S:9Dh)

7	6	5	4	3	2	1	0
-	-	-	-	P4IE.3	P4IE.2	P4IE.1	P4IE.0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	P4IE.3	**Port 4 line 3 Interrupt Enable bit** Clear to disable P4F.3 bit in P4F register to generate an interrupt request. Set to enable P4F.3 bit in P4F register to generate an interrupt request.
2	P4IE.2	**Port 4 line 2 Interrupt Enable bit** Clear to disable P4F.2 bit in P4F register to generate an interrupt request. Set to enable P4F.2 bit in P4F register to generate an interrupt request.
1	P4IE.1	**Port 4 line 1 Interrupt Enable bit** Clear to disable P4F.1 bit in P4F register to generate an interrupt request. Set to enable P4F.1 bit in P4F register to generate an interrupt request.
0	P4IE.0	**Port 4 line 0 Interrupt Enable bit** Clear to disable P4F.0 bit in P4F register to generate an interrupt request. Set to enable P4F.0 bit in P4F register to generate an interrupt request.

Reset Value = XXXX 0000b
Not Bit addressable

Table 29. P4F Register

P4F - Port 4 Flag Register (9Eh)

7	6	5	4	3	2	1	0
-	-	-	-	P4F.3	P4F.2	P4F.1	P4F.0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	P4F.3	**Port 4 line 3 flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.3 bit in P4IE register is set. Must be cleared by software.
2	P4F.2	**Port 4 line 2 flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.2 bit in P4IE register is set. Must be cleared by software.
1	P4F.1	**Port 4 line 1 flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.1 bit in P4IE register is set. Must be cleared by software.
0	P4F.0	**Port 4 line 0 flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.0 bit in P4IE register is set. Must be cleared by software.

Reset Value = XXXX 0000b
Not bit addressable.

10. Power Monitoring and Management

10.1 Introduction

The power monitoring and management can be used to supervise the Power Supply (VDD) and to start up properly when PAROS is powered up.

It consists of the features listed below and explained hereafter:

- Power-Fail reset
- Power-Off flag
- Clock prescaler
- Idle mode
- Power-Down mode

All these features are controlled by four 8-bit registers, the Power Management register (POWM), the Power Filter register (PFILT), the Power Control register (PCON) and the Clock Reload register (CKRL) detailed at the end of this chapter.

10.2 Power-On Reset

Table 30. Pin Conditions in Special Operating Modes

Mode	Program Memory	ALE pin	PSEN# pin	Port 0 pins	Port 1 pins	Port 2 pins	Port 3 pins
Reset	Don’t care	Weak High	Weak High	Floating	Weak High	Weak High	Weak High
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Floating	Data	Data	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Floating	Data	Data	Data

10.3 Power-Fail Detector

The Power-Fail detector is controlled by RSTD bit in CKSEL register (85h). When enabled, the power supply is continuously monitored and an internal reset is generated(1) if VDD goes below V_{RST} for at least TMS.

If the power supply rises again over V_{RST+}(2), the internal reset completes after 64 oscillator clock periods.

If RSTD is set, the power supply monitoring is disabled. To avoid extra consumption and allows VDD reduction to V_{RET} in Power-Down mode, the power supply monitoring is also disabled in this mode (PD= 1).

Note:
1. The internal reset is not propagated on the RST pin.

Caution:
When VDD is reduced to V_{RET} in Power-Down mode the VDD voltage is no more monitored. In this case, RAM content may be damage if VDD goes below V_{RET} and circuit behavior is unpredictable unless an external reset is applied.

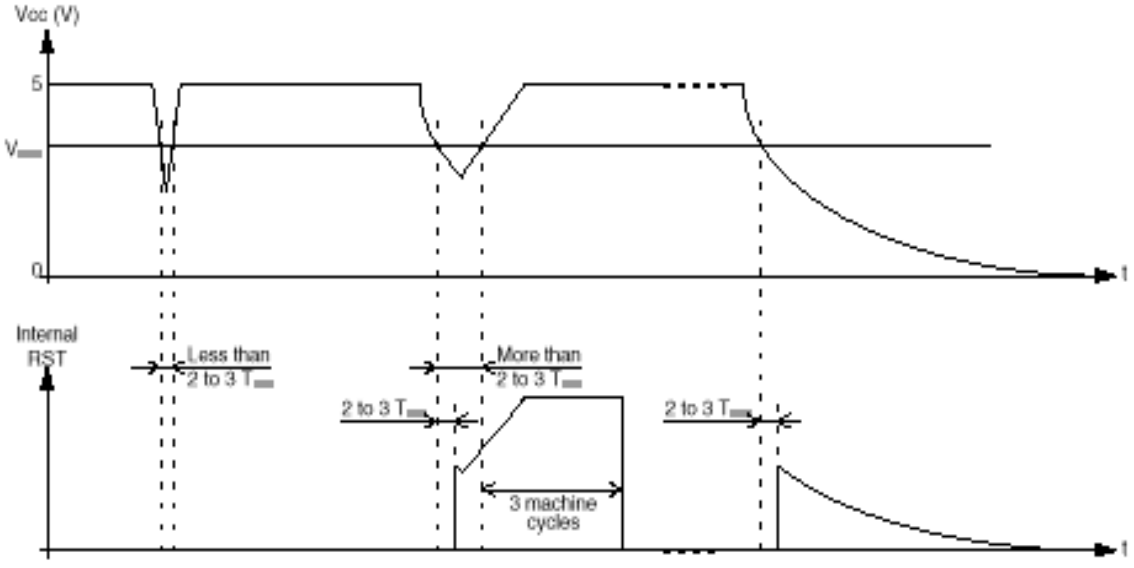


Figure 13. Power Fail Reset timing diagram

10.4 Power-Off Flag

When the power is turned off or fails, the data retention is not guaranteed. A Power-Off Flag (POF, see Table 32.) allows to detect this condition. POF is set by hardware during a reset which follows a power-up or a power-fail. This is a cold reset. A warm reset is an external or a watchdog reset without power failure, hence which preserves the internal memory content and POF. To use POF, test and clear this bit just after reset. Then it will be set only after a cold reset.

Note:
When power supply monitoring is disabled (RSTD= 1 or in Power-Down mode), POF information is not delivered with the same accuracy. It is recommended to clear and not to take in account the POF value after exit from a power down mode with VDD reduction.

10.5 Registers

Table 31. CKRL Register

CKRL (S:97h)
Clock Reload Register

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**Prescaler Value.**

Reset Value= 1111 1111b

Table 32. PCON Register

PCON (S:87h)
Power configuration Register

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**RPD**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Double Baud Rate bit** Set to double the Baud Rate when Timer 1 is used and mode 1, 2 or 3 is selected in SCON register.
6	SMOD0	**SCON Select bit** When cleared, read/write accesses to SCON.7 are to SM0 bit and read/write accesses to SCON.6 are to SM1 bit. When set, read/write accesses to SCON.7 are to FE bit and read/write accesses to SCON.6 are to OVR bit. SCON is Serial Port Control register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off flag** Set by hardware when VDD rises above V_{RET+} to indicate that the Power Supply has been set off. Must be cleared by software.
3	GF1	**General Purpose flag 1** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
2	GF0	**General Purpose flag 0** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
1	PD	**Power-Down Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-Down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	**Idle Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value= 0000 0000b

11. ONCE Mode

The ONCE mode facilitates testing and debugging of systems using Product Name without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of PAROS; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While PAROS is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 33. shows the status of the port pins during ONCE mode.

Table 33. External Pin Status during ONCE Mode

ALE	$\overline{\text{PSEN}}$	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

12. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0 (See Table 34.). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 34. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**AO**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b
Not bit addressable

13. Keyboard Interface

13.1 Introduction

The keyboard interface allows to connect a keypad upto sixteen columns and four lines. The segment and keyboard columns share the same IO pins. The keyboard interface can be managed either by interruption or by polling. The P4F register contains the flags indicating which keys have been pressed. The P4IE register allows to enable the interrupt of the keyboard inputs. IE1 register enables the global interrupt request of the keyboard.

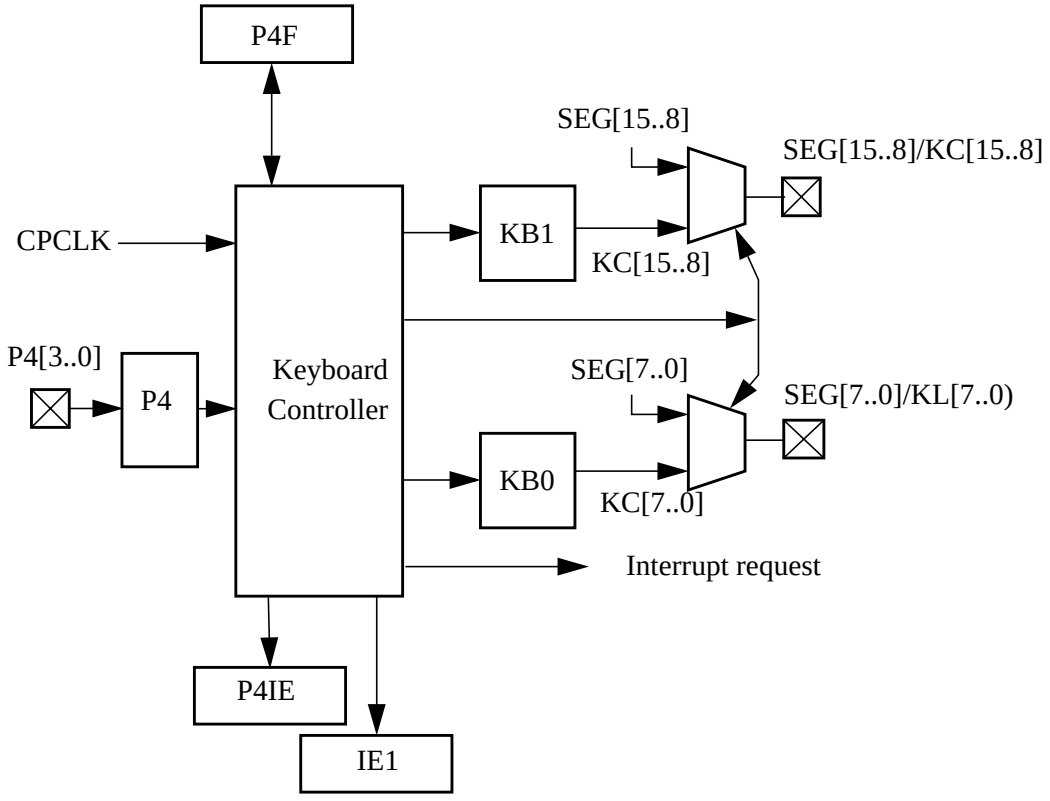


Figure 14. Block diagram of the keyboard interface

The Figure 25. shows the behavior of the scanning process. When a key is pressed the scanning pulse is transmitted to one line of PORT4, an interruption is generated and the number of the line is latched into the P4F register. The scanning process is stopped. It will be restarted when the P4Fn bit which requests the interrupt is cleared by software.

13.1.1 Keybaord IOs implementation

The scanning lines are mapped on the same outputs than the LCD drivers (SEGn) and the implementation is given on the Table 35.

Table 35. Implementation of the scanning lines

SEG0/KC0	SEG4/KC4	SEG8/KC8	SEG12/KC12
SEG1/KC1	SEG5/KC5	SEG9/KC9	SEG13/KC13
SEG2/KC2	SEG6/KC6	SEG10/KC10	SEG14/KC14
SEG3/KC3	SEG7/KC7	SEG11/KC11	SEG15/KC15

Two extra ports (KB0/P5 and KB1/P6) are added and are implemented as alternate functions of SEG/KC IO pins. These two registers contains the number of the line which is currently scanned.

When the LCD controller is on, KB0 and KB1 registers are time multiplexed with the SEG/KC IO pins (see Table 35). Thus during a fixed time slot the SEG/KC pin generates a positive output signal to the keyboard matrix.

13.1.1.1 Scanning pulse level

The controller support upto six LCD levels. The number of levels used is depending on the LCD display and it has to be selecting by an external resistor ladder (see LCD controller part). When the keyboard is scanned, the segments will use VCC and GND level.

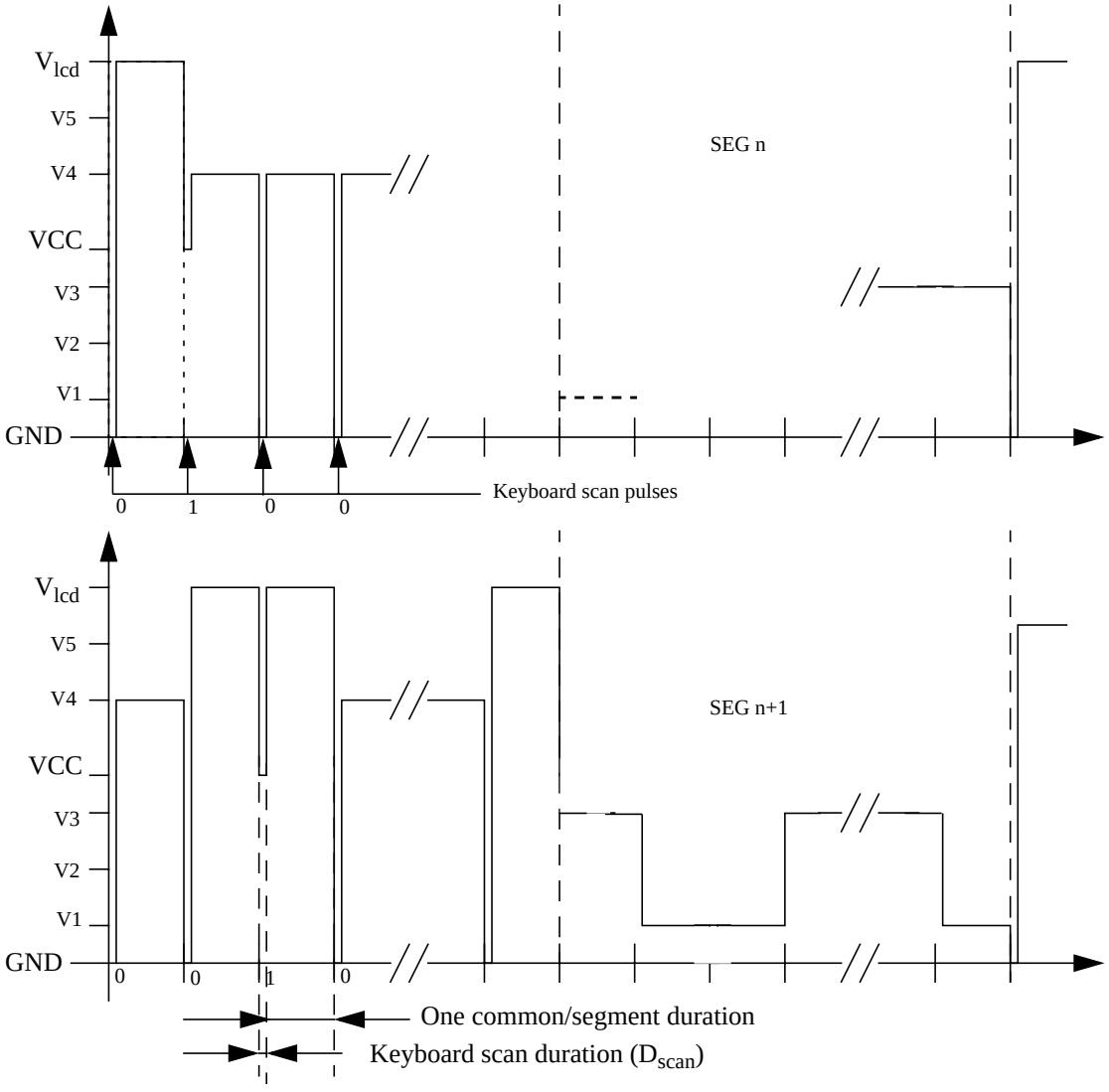


Figure 15. Scanning process

The Figure 15. gives an example for a LCD display running with 6 levels mode. In "normal trame", when the scanning pulse is inactive the level in equal to GND, when the scanning pulse is active the level is equal to VCC. Those levels are inverted during the "inverted trame".

13.1.1.2 Scanning pulse timing and scanning frequency

The Keyboard scan process is performed during the begin of COMn (with $0 < n < 17$). The duration of this pulse is 1/24th of the COMn time.

The duration of COMn is:

$$tCOMn = \frac{72}{CPCK}$$

The scan pulse duration is:

$$tSCAN = \frac{tCOMn}{24} = \frac{3}{CPCK}$$

The scanning frequency is the based on the commons frequency (COMn).

13.1.2 Keyboard input

The keyboard input architecture is shown on the Figure 16. The P4F register allows to identify which key of the keypad has been pressed. The inputs of the keyboard have a schmitt trigger structure to avoid the switching noise of the keypad to generate spurious interruptions. The scanning of the column is done during the COM0. Each bits of the P4F register can be separately reset or set.

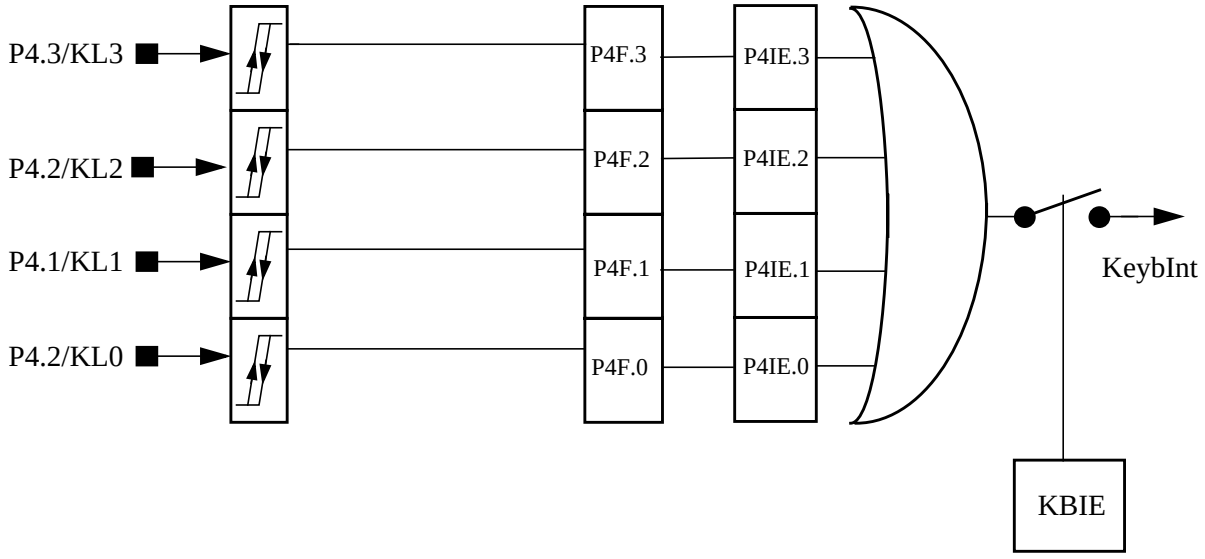


Figure 16. Keyboard input structure

13.2 Interruption

When a key is pressed and when a scan pulse is generated on one of the 16 scanning lines a high level is strobed on one of the four keyboard input lines of P4. So the following processes are executed:

- the scanning process is freezed. The column number is recorded in the KB0 and KB1 registers,
- the corresponding PF4.n flag in the P4F register is set to one. If more than one keys are pressed during the same scanning column each PF4.n flags are set to one,
- an interrupt request is sent to the interrupt controller.

After the interrupt sequence is processed the interrupt request flag P4F.n has to be reset by software. This action restarts the scanning column operation.

Table 36. Output for Keyboard Register

KB0 - Ouput for Keyboard Register 0 (E8h) or Specific P5 (E8h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b

Recording of keyboard scan pulses for column determination.

Table 37. Output for Keyboard Register

KB1 - Ouput for Keyboard Register 1 (F8h) or Specific P6 (F8h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b

Recording of keyboard scan pulses for column determination.

14. Voltage Comparator

14.1 Overview

The comparator feature can be used at each time a level supplied to the P4.5 and P4.4 inputs have to be compared with a reference level. Coupled to a time bas it can be used as a analog voltage converter.

14.2 Description

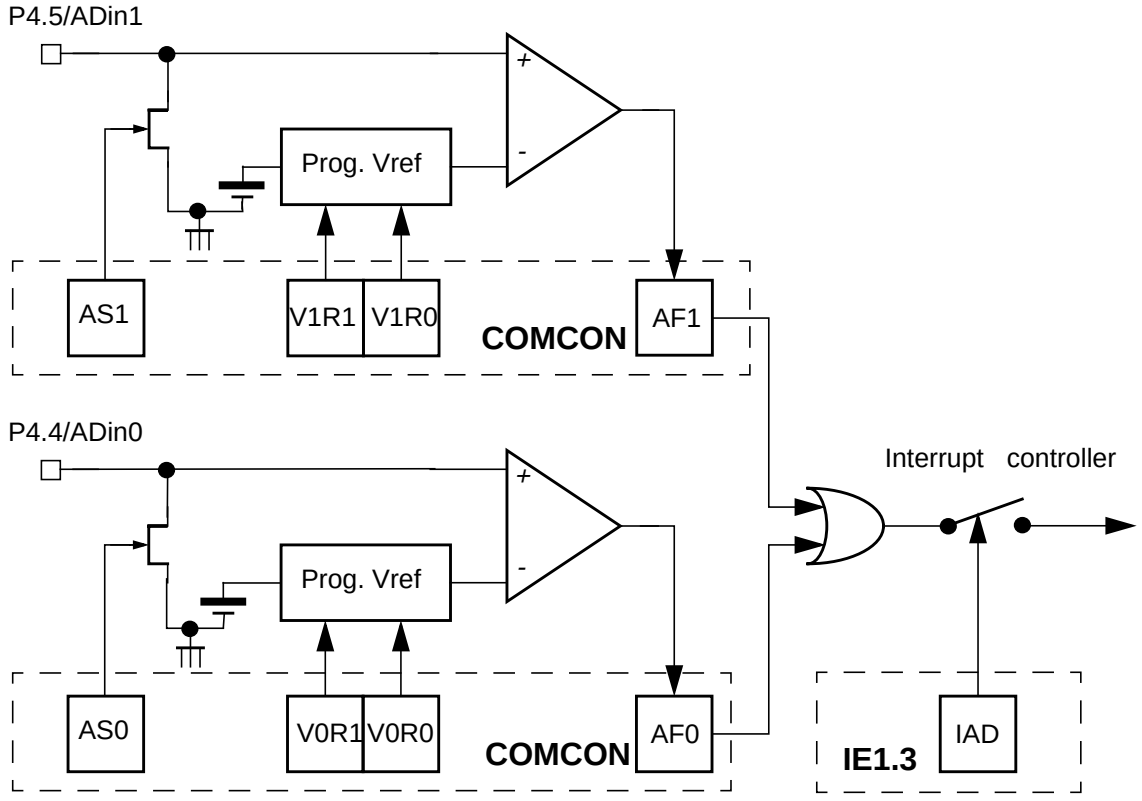


Figure 17. Block diagram of the volatge comparator

The voltage comparator is built around a four level programmable voltage reference through the VRn control bits in the COMCON register. The AS1 and AS0 control bits in the COMCON are cleared by default to force the input level to zero before starting the conversion. The AS1 and AS0 control bits has to set to one to start the voltage comparaison process. When the comparaion is achieved the AF1 and AF0 status bits in the COMCON register are set to one and an interrupt request is sent to the interrupt controller. If the IAD control bit in the IE1 is set to one this ineterrupt will be processed. To complete the interrupt process the AF1/AF0 status bits have to be cleared by software to reset the interrupt request.

Table 38. COMCON Register

COMCON - (A3h)

7	6	5	4	3	2	1	0
AF1	**AS1**	**V1R1**	**V1R0**	**AF0**	**AS0**	**V0R1**	**V0R0**

Bit Number	Bit Mnemonic	Description
7/3	AF1/AF0	= 1, indicates the input level (P4.5/P4.4) has matched the reference level. = 0, the input is less than the reference level.
6/2	AS1/AS0	= 1, start the voltage comparison process = 0, stop the voltage comparaison process
5/1	V1R1/V0R1	Disconnect the voltage reference or select one of three reference value **V1R1/V0R1 Voltage reference** 1 63% x VDD 1 50% x VDD 0 20% x VDD 0 Disconnected
4/0	V1R0/V0R0	Disconnect the voltage reference or select one of three reference value **V1R0/V0R0 Voltage reference** 1 63% x VDD 0 50% x VDD 1 20% x VDD 0 Disconnected

Reset Value = 0100 0100b

AF1, AF0 = 1 , indicates the input level has matched the reference level.

15. WatchDog Timer

PAROS contains a powerfull programmable hardware WatchDog Timer (WDT) that automatically resets the chip if it software fails to reset the WDT before the selected time interval has elapsed. It permits large Time-Out ranking from 16ms to 2s @Fosc = 12MHz.

This WDT consist of a 14-bit counter plus a 7-bit programmable counter, a WatchDog Timer reset register (WDTRST) and a WatchDog Timer programmation (WDTPRG) register. When exiting reset, the WDT is -by default- disable. To enable the WDT, the user has to write the sequence 1EH and E1H into WDRST register. When the WatchDog Timer is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $96xT_{OSC}$, where $T_{OSC}=1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

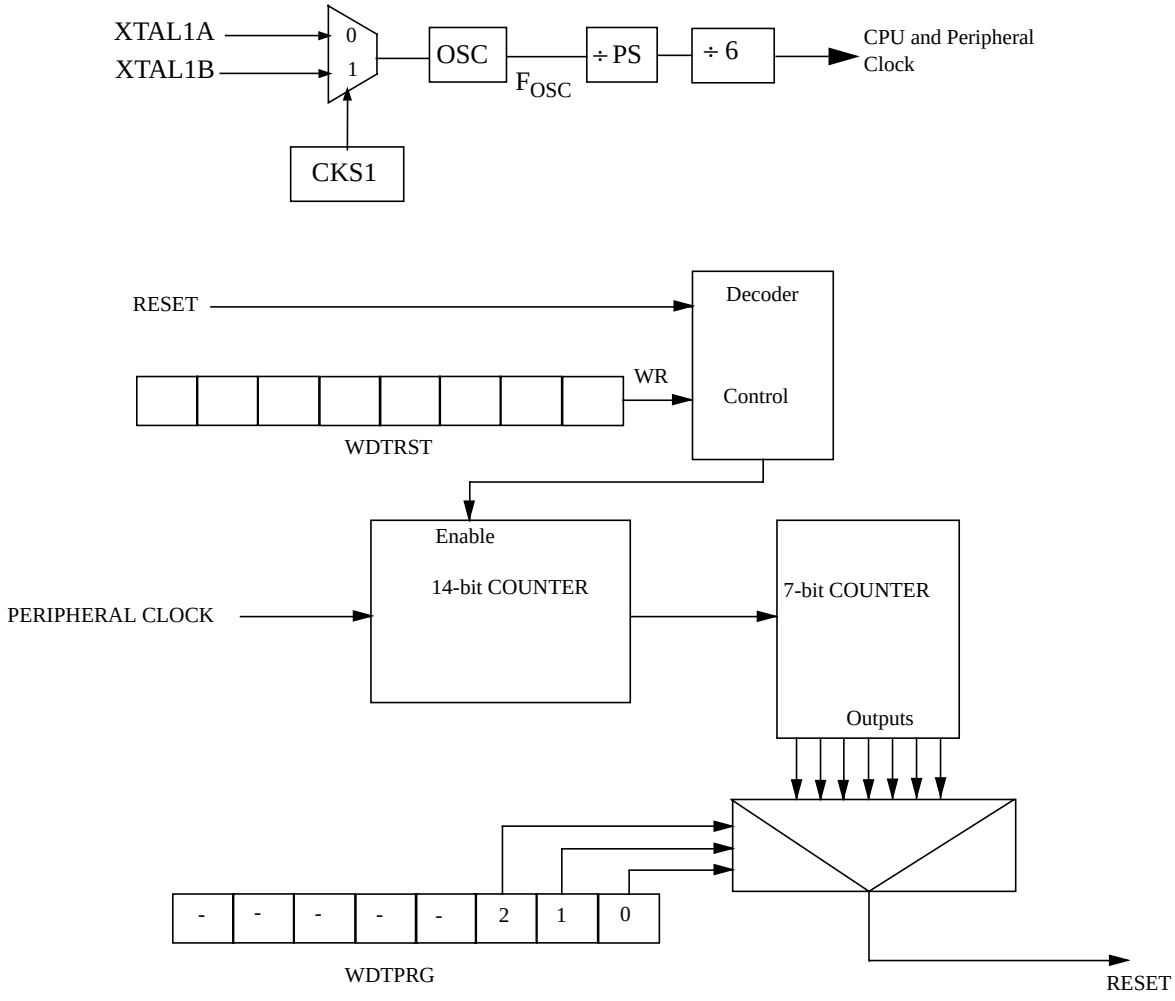


Figure 18. Watchdog Timer

The WDT is controlled by two registers (WDTRST and WDTPRG).

Table 39. WDTPRG Register

WDTPRG - WatchDog Timer Duration Programming register (A7h

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	S2	**WatchDog Timer Duration selection bit 2** Work in conjunction with bit 1 and bit 0.
1	S1	**WatchDog Timer Duration selection bit 1** Work in conjunction with bit 2 and bit 0.
0	S0	**WatchDog Timer Duration selection bit 0** Work in conjunction with bit 1 and bit 2.

Reset Value = XXXX X000b

The three lower bits (S0, S1, S2) located into WDTPRG register permits to program the WDT duration.

Table 40. Machine Cycle Count

S2	S1	S0	Machine Cycle Count
0	0	0	2^{14} - 1
0	0	1	2^{15} - 1
0	1	0	2^{16} - 1
0	1	1	2^{17} - 1
1	0	0	2^{18} - 1
1	0	1	2^{19} - 1
1	1	0	2^{20} - 1
1	1	1	2^{21} - 1

To compute WD Time-Out, the following formula is applied:

$$TimeOut = \frac{F_{XTAL}}{12 \times ((2^{14} \times 2^{Svalue}) - 1) \times (256 - PS)}$$

Note : Svalue represents the decimal value of (S2 S1 S0) / PS represents the Prescalar

Find Hereafter computed Time-Out value for FFosc$_{XTAL}$ = 12MHz

Table 41. Time-Out computation @12MHz

S2	S1	S0	Time-Out for F_{XTAL}osc=12MHz
0	0	0	16.38 ms
0	0	1	32.77 ms
0	1	0	65.54 ms
0	1	1	131.07 ms
1	0	0	262.14 ms
1	0	1	524.29 ms
1	1	0	1.05 s
1	1	1	2.10 s

Table 42. Watchdog Timer Enable Register

WDTRST - WatchDog Timer Enable register (Write Only) (A6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

The WDTRST register is used to reset/enable the WDT by writing 1EH then E1H in sequence.

15.1 WatchDog Timer during Power down mode and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally does whenever PAROS is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power Down.
To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.
In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting PAROS while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

16. DUAL Data Pointer

PAROS contains a Dual Data Pointer accelerating data memory block moves. The Standard 80C52 Data Pointer is a 16-bit value that is used to address off-chip data RAM or peripherals. In PAROS, the standard 16-bit data pointer is called DPTR and located at SFR location 82H and 83H. The second Data Pointer named DPTR1 is located at the same address than the previous one. The DPTR select bit (DPS / bit0) chooses the active pointer and it is located into the AUXR1 register. It should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.
The user switches between data pointers by toggling the LSB of the AUXR1. The increment (INC) is one of the solution to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual Data Pointer saves code and ressources when moves of blocks need to be accomplished.

The second Data Pointer can be used to address the on-chip XRAM.

Table 43. DPL Register

DPL - Low Byte of DPTR1 (82h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 44. DPH Register

DPH - High Byte of DPTR1 (83h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 45. AUXR1 Register

AUXR1 - Dual Pointer Selection Register (A2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**DPS**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer 1** Clear to select DPTR as Data Pointer. Set to select DPTR1 as Data Pointer.

17. Programmable Counter Array (PCA)

The Programmable Counter Array is a special 16-bit Timer that has two 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1.4 (CEX1). In PAROS, only module 0 and module 1 are integrated.

17.1 Operating Mode

The PCA timer is a common time base for all two modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR. as follows :

CPS1	CPS0	PCA timer Count Source
0	0	$F_{OSC}/12$
0	1	$F_{OSC}/4$
1	0	Timer 0
1	1	External ECI pin

In the CMOD SFR are two additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode and ECF which when set allows the PCA overflow flag CF (in the CCON SFR) to generate an interrupt.

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module. To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 1 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Each module in the PCA has a special function register associated with it. These registers are: CCAPMx for module number x. The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

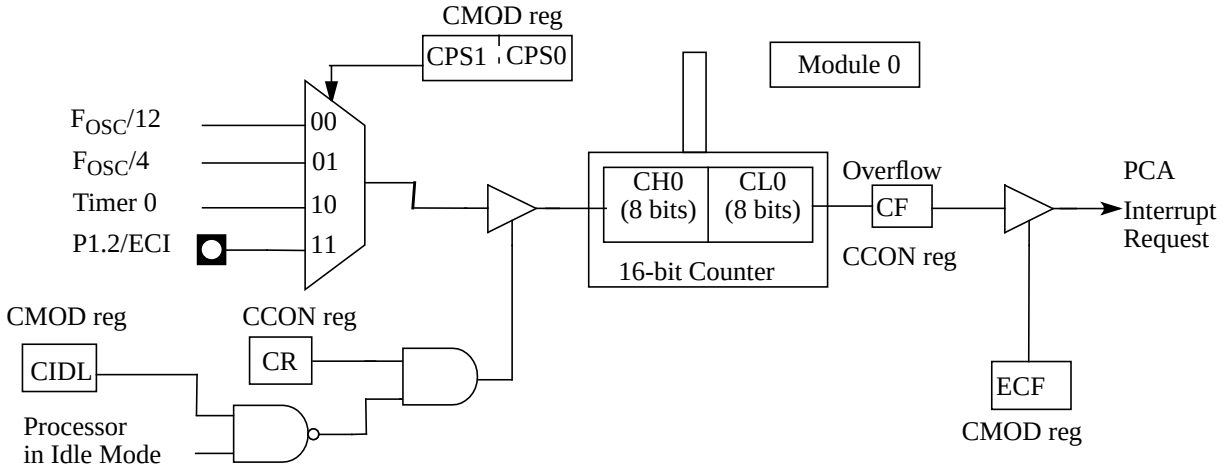


Figure 19. PCA Mode for module 0

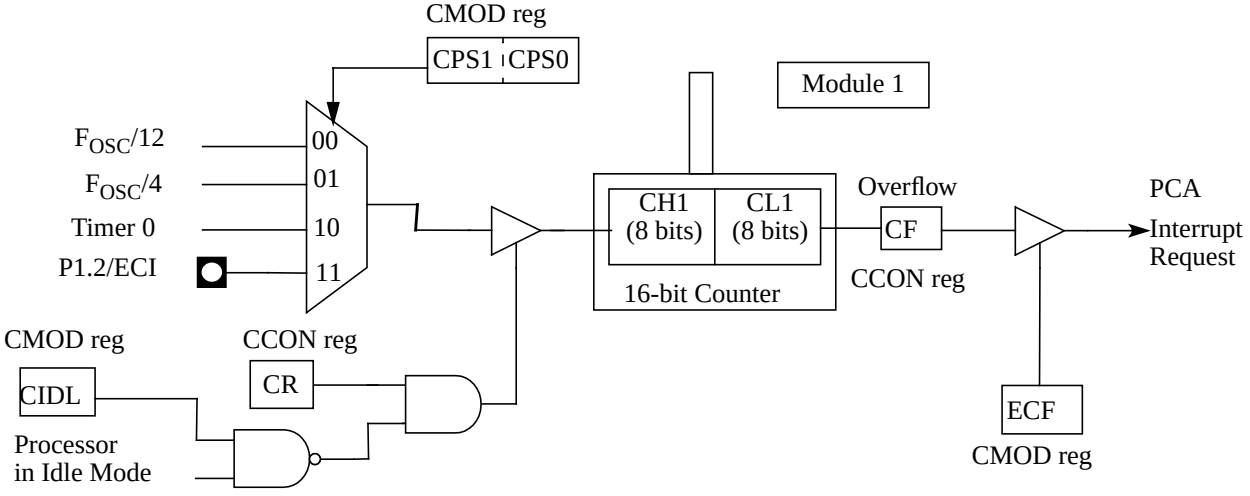


Figure 20. PCA Mode for module 1

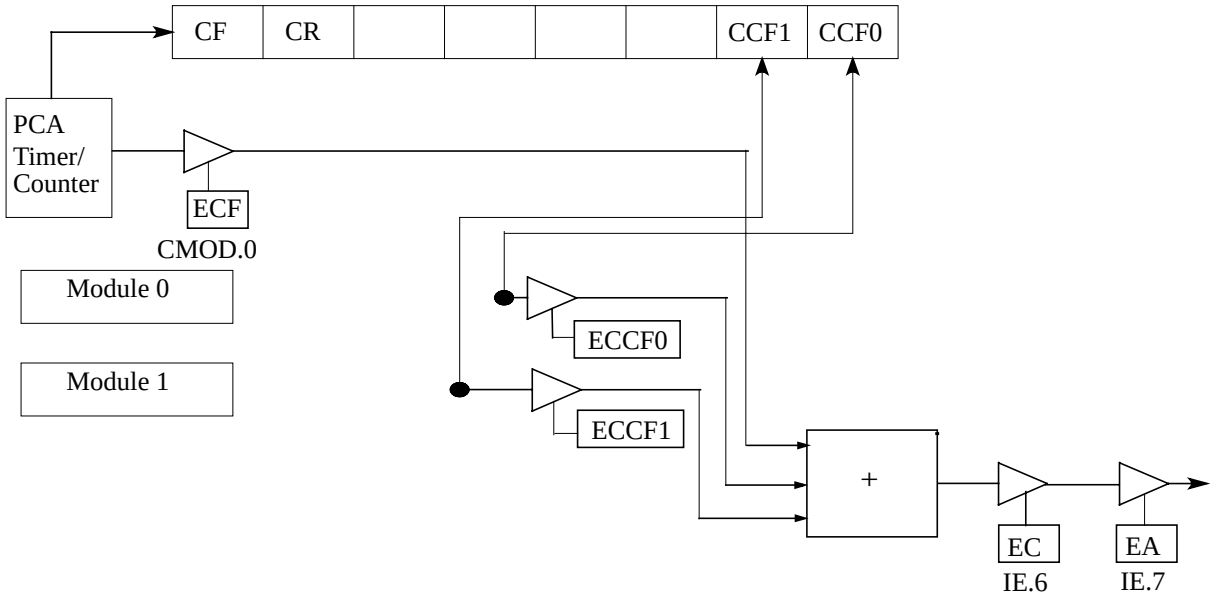


Figure 21. PCA Timer Interrupts

17.2 PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

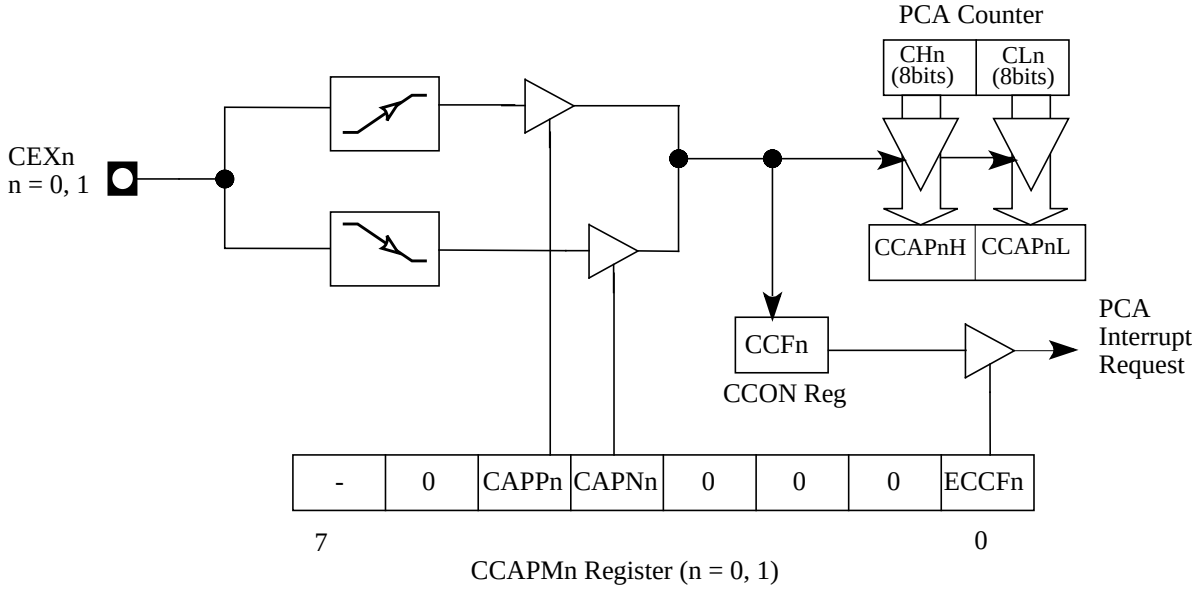


Figure 22. PCA Capture Mode

17.3 16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

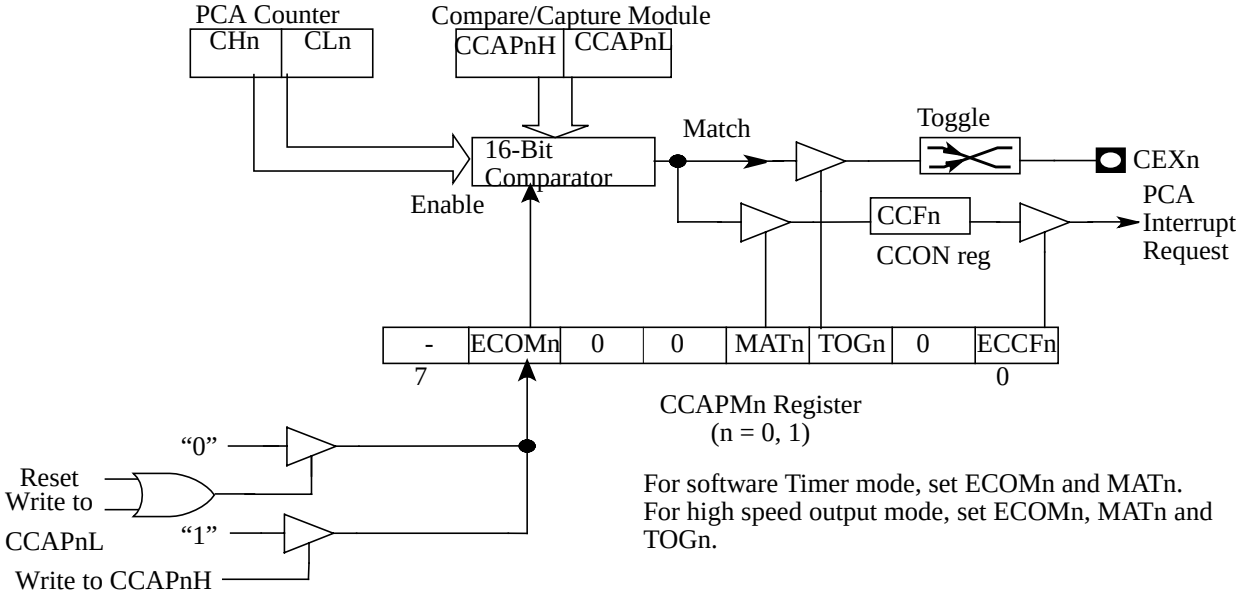


Figure 23. PCA 16-bit Software Timer and Hifh Speed Ouput Mode

17.4 High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set.

17.5 Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

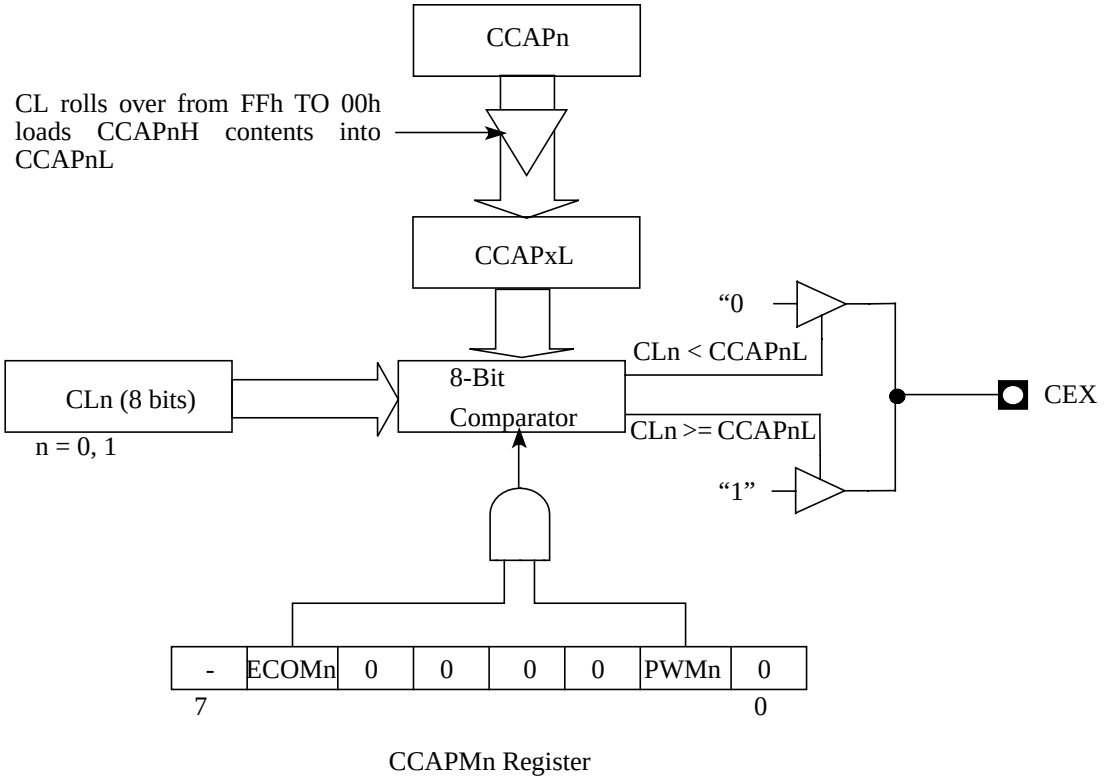


Figure 24. PCA PWM Mode

17.6 PCA Registers

Table 46. PCA Register

PCA High Byte Compare/Capture Module n Registers (n = 0, 1)
CCAP0H (FAh)
CCAP1H (FBh)
High Byte Compare/Capture Module n

7	6	5	4	3	2	1	0
High Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CCAPnH 7:0	**High byte of EWC-PCA comparison or capture values**

Reset Value = XXXX XXXXb

Table 47. PCA Register

PCA Low Byte Compare/Capture Module n Registers (n = 0, 1)
CCAP0L (EAh)
CCAP1L (EBh)
Low Byte Compare/Capture Module n

7	6	5	4	3	2	1	0
Low Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CCAPnL 7:0	**Low byte of EWC-PCA comparison or capture values**

Reset Value = XXXX XXXXb

Table 48. PCA Register

PCA Compare/Capture Module n Mode registers (n = 0, 1)
CCAPM0 (DAh)
CCAPM1 (DBh)

7	6	5	4	3	2	1	0
-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The Value read from this bit is indeterminate. Do not set this bit.
6	ECOMn	**Enable Compare Mode Module x bit** Clear to disable the Compare function. Set to enable the Compare function.. The Compare function is used to implement the software Timer, the high-speed output, the Pulse Width Modulator (PWM) and Watchdog Timer (WDT).
5	CAPPn	**Capture Mode (Positive) Module x bit** Clear to disable the Capture function triggered by a positive edge on CEXx pin. Set to enable the Capture function triggered by a positive edge on CEXx pin
4	CAPNn	**Capture Mode (Negative) Module x bit** Clear to disable the Capture function triggered by a negative edge on CEXx pin. Set to enable the Capture function triggered by a negative edge on CEXx pin.
3	MATn	**Match Module x bit** Set when a match of the PCA Counter with the Compare/Capture register sets CCFx bit in CCON register, flagging an interrupt. Must be cleared by software.
2	TOGn	**Toggle Module x bit** The toggle mode is configured by setting ECOMx, MATx and TOGx bits. Set when a match of the PCA Counter with the Compare/Capture register toggles the CEXx pin. Must be cleared by software.
1	PWMn	**Pulse Width Modulation Module x Mode bit** Set to configure the module x as an 8-bit Pulse Width Modulator with output waveform on CEXx pin . Must be cleared by software.
0	ECCFn	**Enable CCFx Interrupt bit** Clear to disable CCFx bit in CCON register to generate an interrupt request. Set to enable CCFx bit in CCON register to generate an interrupt request.

Reset Value = X000 0000b

Table 49. CCON, Timer/Counter Control Register

Timer/Counter Control Register CCON (D8h)

7	6	5	4	3	2	1	0
CF	**CR**	**-**	**-**	**-**	**-**	**CCF1**	**CCF0**

Bit Number	Bit Mnemonic	Description
7	CF	**PCA Timer/Counter Overflow flag** Set by hardware when the PCA Timer/Counter rolls over. This generates a PCA interrupt request if the ECF bit in CMOD register is set. Must be cleared by software.
6	CR	**PCA Timer/Counter Run Control bit** Clear to turn the PCA Timer/Counter off. Set to turn the PCA Timer/Counter on.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	CCF1	**PCA Module 1 Compare/Capture flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 1 bit in CCAPM 1 register is set. Must be cleared by software.
0	CCF0	**PCA Module 0 Compare/Capture flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 0 bit in CCAPM 0 register is set. Must be cleared by software.

Reset Value = 00XX XX00b

Table 50.

Timer/Counter Registers High value CH0 (F9h)

7	6	5	4	3	2	1	0
High Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CH0 7:0	**High byte of Timer/Counter**

Reset Value = 0000 00000b

Table 51.

Timer/Counter Registers Low value CL0 (S:E9h)

Low Byte of Timer/Counter Register

7	6	5	4	3	2	1	0
Low Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CL0 7:0	**Low byte of Timer/Counter**

Reset Value = 0000 00000b

Table 52.

Timer/Counter Registers High value CH1 (F1h)

7	6	5	4	3	2	1	0
High Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CH1 7:0	**High byte of Timer/Counter**

Reset Value = 0000 00000b

Table 53.

Timer/Counter Registers Low value CL1 (E1h)

Low Byte of Timer/Counter Register

7	6	5	4	3	2	1	0
Low Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CL1 7:0	**Low byte of Timer/Counter**

Reset Value = 0000 00000b)

Table 54.

Timer/Counter Mode Register CMOD (D9h)

7	6	5	4	3	2	1	0
CIDL	**-**	**-**	**-**	**-**	**CPS1**	**CPS0**	**ECF**

Bit Number	Bit Mnemonic	Description
7	CIDL	**PCA Counter Idle Control bit** Clear to let the PCA running during Idle mode. Set to stop the PCA when Idle mode is invoked.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	CPS1	**EWC Count Pulse Select bits** CPS1 CPS0 Clock source 0 0 Internal Clock, Fosc/12 0 1 Internal Clock, Fosc/4 1 0 Timer 0 overflow 1 1 External clock at ECI/P1.2 pin (Max. Rate = Fosc/8)
1	CPS0	
0	ECF	**Enable PCA Counter Overflow Interrupt bit** Clear to disable CF bit in CCON register to generate an interrupt. Set to enable CF bit in CCON register to generate an interrupt.

Reset Value = 00XX X000b

18. Inter-Integrated Circuit Interface (I2C)

Introduction

The Synchronous Serial Link Controller (SSLC) provides the selection of one synchronous serial interface among the three most popular ones:

- Inter-Integrated Circuit (I^2C) interface.
- Serial Peripheral Interface

When an interface is selected, the others are no longer available, their usage is exclusive.

This section describes the I^2C. In the rest of the section SSLC means I^2C. The I^2C bus is a bi-directional two-wire serial communication standard. It is designed primarily for simple but efficient integrated circuit (IC) control. The system is comprised of two lines, SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. The serial data transfer is limited to 100Kbit/s in standard mode. Various communication configuration can be designed using this bus. Figure 25 shows a typical I^2C bus configuration. All the devices connected to the bus can be master and slave.

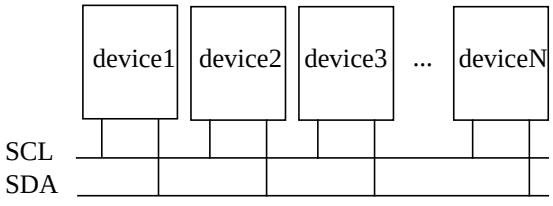


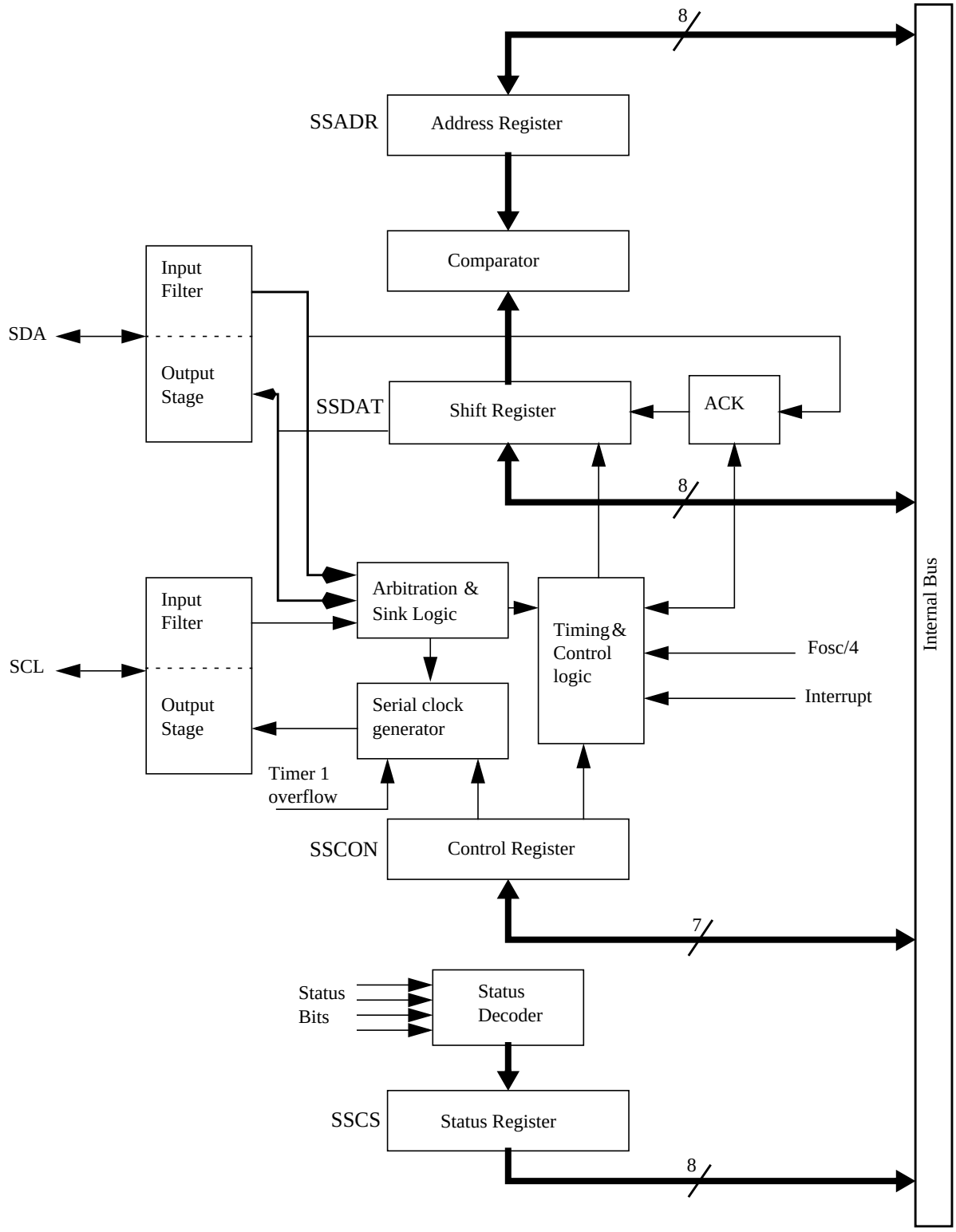
Figure 25. I^2C bus configuration

18.1 Pin Description

OSC : clock of oscillator.
NRESET : reset active on low level.
NRD : read active on low level.
NWR : write active on low level.
ALE : address latch enable active on high level.
DATA_IN : bus of datas.
SDA_IN : value of I^2C line after Wire And.
SCL_IN : value of I^2C clock after Wire And.

ENADATA : direction of the bidirectional buffers for datas.
SERIAL_IT : IT active on high level.
DATA_OUT : bus of datas.
SDA_OUT : value of I^2C line before Wire And.
SCL_OUT : value of I^2C clock before Wire And.

18.2 Block Diagram



18.3 Description

18.3.1 Introduction

The CPU interfaces to the I^2C logic via the following four 8-bit special function registers: the Synchronous Serial Control register (SSCON see Table 63 and Table 64), the Synchronous Serial Data register (SSDAT see Table 65 and Table 66), the Synchronous Serial Control and Status register (SSCS see Table 70 and Table 68) and the Synchronous Serial Address register (SSADR see Table 69 and Table 70).

SSCON is used to enable SSLC, to program the bit rate (see Table 55), to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the I^2C bus, and to acknowledge a serial interrupt. An hardware reset disables SSLC.

In write mode, SSCS is used to select the I^2C interface and to select the bit rate source. In read mode, SSCS contains a status code which reflects the status of the I^2C logic and the I^2C bus. The three least significant bits are always zero. The five most significant bits contains the status code. There are 26 possible status codes. When SSCS contains F8h, no relevant state information is available and no serial interrupt is requested. A valid status code is available in SSCS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. Table 58 to Table 62 give the status for the master modes and miscellaneous states.

SSDAT contains a byte of serial data to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when I^2C logic is in a defined state and the serial interrupt flag is set. Data in SSDAT remains stable as long as SI is set. While data is being shifted out, data on the bus is simultaneously shifted in; SSDAT always contains the last byte present on the bus.

SSADR may be loaded with the 7-bit slave address (7 most significant bits) to which SSLC will respond when programmed as a slave transmitter or receiver. The LSB is used to enable general call address (00h) recognition.

Figure 26 shows how a data transfer is accomplished on the I^2C bus.

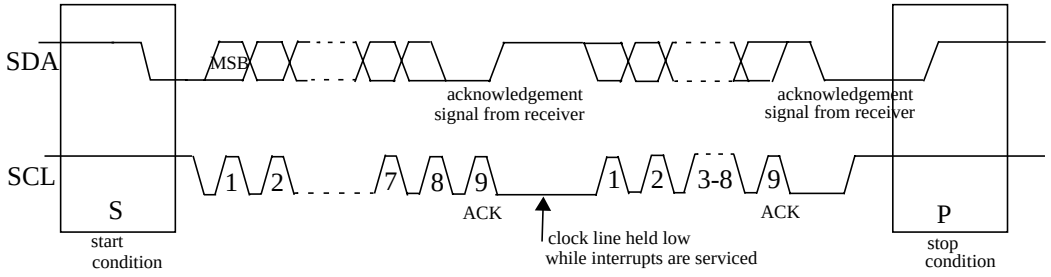


Figure 26. Complete data transfer on I^2C bus

The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave transmitter
- Slave receiver

Data transfer in each mode of operation are shown in Figure 27 to Figure 30. These figures contain the following abbreviations:

S : START condition

R: Read bit (high level at SDA)

W : Write bit (low level at SDA)

A : Acknowledge bit (low level at SDA)

$\overline{A}$: Not acknowledge bit (high level at SDA)

Data : 8-bit data byte

P : STOP condition

In Figure 27 to Figure 30, circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in SSCS. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When the serial interrupt routine is entered, the status code in SSCS is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in Table 58 to Table 61.

18.3.2 Master transmitter mode

In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 27). Before the master transmitter mode can be entered, SSCON must be initialised as follows:

Table 55. SSCON initialization

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	X	bit rate	bit rate

CR0, CR1 and CR2 define the internal serial bit rate if external bit rate generator is not used. SSIE must be set to enable SSLC. STA, STO and SI must be cleared.

The master transmitter mode may now be entered by setting the STA bit. The I^2C logic will now test the I^2C bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SI bit in SSCON) is set, and the status code in SSCS will be 08h. This status must be used to vector to an interrupt routine that loads SSDAT with the slave address and the data direction bit (SLA+W). The must then be reset before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, SI is set again and a number of status code in SSCS are possible. There are 18h, 20h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in . This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are not referred to in Table 58. After a repeated START condition (state 10h) SSLC may switch to the master receiver mode by loading SSDAT with SLA+R.

18.3.3 Master receiver mode

In the master receiver mode, a number of data bytes are received from a slave transmitter (see Figure 28). The transfer is initialised as in the master transmitter mode. When the START condition has been transmitted, the interrupt routine must load SSDAT with the 7-bit slave address and the data direction bit (SLA+R). The serial interrupt flag must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, the serial interrupt flag is set again and a number of status code in SSCS are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in Table 59. This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are not referred to in Table 59. After a repeated START condition (state 10h) SSLC may switch to the master transmitter mode by loading SSDAT with SLA+W.

18.3.4 Slave receiver mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (see Figure 29). To initiate the slave receiver mode, SSADR and SSCON must be loaded as follows :

Table 56. SSADR : slave receiver mode initialization

A6	A5	A4	A3	A2	A1	A0	GC
own slave address							

The upper 7 bits are the address to which SSLC will respond when addressed by a master. If the LSB (GC) is set SSLC will respond to the general call address (00h); otherwise it ignores the general call address :

Table 57. SSCON : slave receiver mode initialization

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	1	bit rate	bit rate

CR0, CR1 and CR2 have no effect in the slave mode (see Table 60). SSIE must be set to enable SSLC. The AA bit must be set to enable the own slave address or the general call address acknowledgement. STA, STO and SI must be cleared.

When SSADR and SSCON have been initialised, SSLC waits until it is addressed by its own slave address followed by the data direction bit which must be logic 0 (W) for SSLC to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag is set and a valid status code can be read from SSCS. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in . The slave receiver mode may also be entered if arbitration is lost while SSLC is in the master mode (see states 68h and 78h).

If the AA bit is reset during a transfer, SSLC will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, SSLC does not respond to its own slave address. However, the I^2C bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate SSLC from the I^2C bus.

18.3.5 Slave transmitter mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see Figure 30). Data transfer is initialised as in the slave receiver mode. When SSADR and SSCON have been initialised, SSLC waits until it is addressed by its own slave address followed by the data direction bit which must be logic 1 (R) for SSLC to operate in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag is set and a valid status code can be read from SSCS. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in Table 61. The slave transmitter mode may also be entered if arbitration is lost while SSLC is in the master mode (see state B0h).

If the AA bit is reset during a transfer, SSLC will transmit the last byte of the transfer and enter state C0h or C8h. SSLC is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all 1's as serial data. While AA is reset, SSLC does not respond to its own slave address. However, the I^2C bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate SSLC from the I^2C bus.

18.3.6 Miscellaneous States

There are two SSCS codes that do not correspond to a define SSLC hardware state (see Table 62). These are discuss hereafter.

Status F8h indicates that no relevant information is available because the serial interrupt flag is not yet set. This occurs between other states and when SSLC is not involved in a serial transfer.

Status 00h indicates that a bus error has occurred during an SSLC serial transfer. A bus error is caused when a START or a STOP condition occurs at an illegal position in the format frame. Examples of such illegal positions are during the serial transfer of an address byte, a data byte, or an acknowledge bit. When a bus error occurs, SI is set. To recover from a bus error, the STO flag must be set and SI must be cleared. This causes SSLC to enter the not addressed slave mode and to clear the STO flag (no other bits in SSCON are affected). The SDA and SCL lines are released and no STOP condition is transmitted.

18.4 Notes

SSLC interfaces to the external I^2C bus via two port pins: SCL (serial clock line) and SDA (serial data line). To avoid low level asserting on these lines when SSLC is enabled, the output latches of SDA and SLC must be set to logic 1.

			Bit Frequency (KHz)		
CR 2	CR 1	CR 0	Fosc = 12 MHz	Fosc = 16 MHz	F_{OSC} divided by
0	0	0	47	62.5	256
0	0	1	53.5	71.5	224
0	1	0	62.5	83	192
0	1	1	75	100	160
1	0	0	12.5	16.5	960
1	0	1	100	-	120
1	1	0	-	-	60
1	1	1	0.5 < . < 62.5	0.67 < . < 83	96 · (256 - reload value Timer 1) (reload value range: 0-254 in mode 2)

Table 58. Status for master transmitter mode

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
08h	A START condition has been transmitted	Load SLA+W	X	0	0	X	SLA+W will be transmitted; ACK will be transmitted
10h	A repeated START condition has been transmitted	Load SLA+W or Load SLA+R	X X	0 0	0 0	X X	SLA+W will be transmitted; ACK will be transmitted SLA+R will be transmitted Logic will switched to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Load data byte or No SSDAT action or No SSDAT action or No SSDAT action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted and ACK will be received Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset STOP condition followed by a START condition will be transmitted and STO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Load data byte or No SSDAT action or No SSDAT action or No SSDAT action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted and ACK will be received Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset STOP condition followed by a START condition will be transmitted and STO flag will be reset
28h	Data byte has been transmitted; ACK has been received	Load data byte or No SSDAT action or No SSDAT action or No SSDAT action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted and ACK will be received Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset STOP condition followed by a START condition will be transmitted and STO flag will be reset
30h	Data byte has been transmitted; NOT ACK has been received	Load data byte or No SSDAT action or No SSDAT action or No SSDAT action	0 1 0 1	0 0 1 1	0 0 0 0	X X X X	Data byte will be transmitted and ACK will be received Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset STOP condition followed by a START condition will be transmitted and STO flag will be reset
38h	Arbitration lost in SLA+W or data bytes	No SSDAT action or No SSDAT action	0 1	0 0	0 0	X X	I^2C bus will be released and not addressed slave mode will be entered A START condition will be transmitted when the bus becomes free

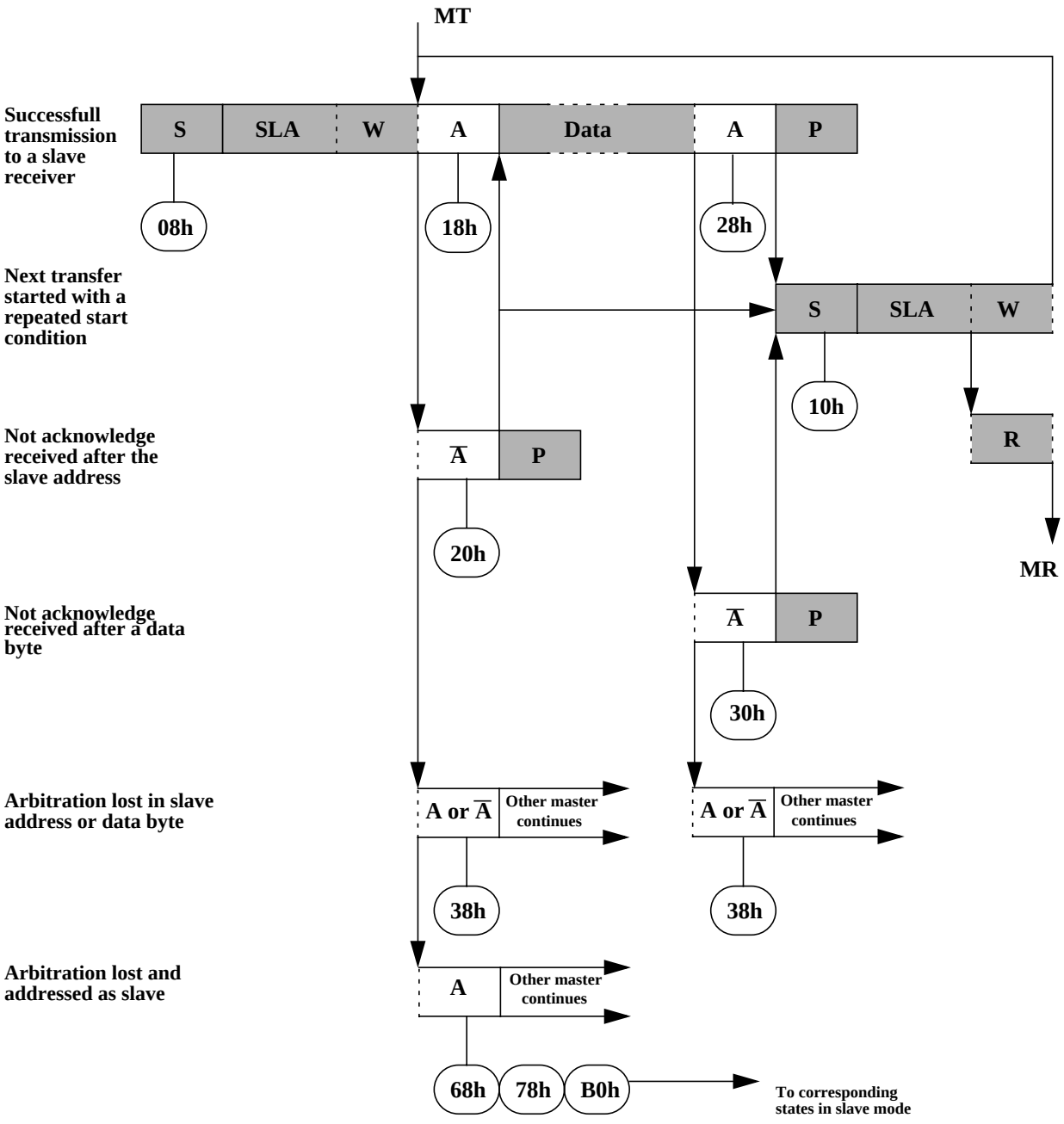


Figure 27. Format and state in the master transmitter mode

Table 59. Status for master receiver mode

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
08h	A START condition has been transmitted	Load SLA+R	X	0	0	X	SLA+W will be transmitted; ACK will be transmitted
10h	A repeated START condition has been transmitted	Load SLA+R or	X	0	0	X	SLA+W will be transmitted; ACK will be transmitted
		Load SLA+W	X	0	0	X	SLA+W will be transmitted Logic will switched to master transmitter mode
38h	Arbitration lost in SLA+R or NOT ACK bit	No SSDAT action or	0	0	0	X	I^2C bus will be released and not addressed slave mode will be entered
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free
40h	SLA+R has been transmitted; ACK has been received	No SSDAT action or	0	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	0	0	0	1	Data byte will be received and ACK will be returned
48h	SLA+R has been transmitted; NOT ACK has been received	No SSDAT action or	1	0	0	X	Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset
		No SSDAT action or	0	1	0	X	
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset
50h	Data byte has been received; ACK has been returned	Read data byte or	0	0	0	0	Data byte will be received and NOT ACK will be returned
		read data byte	0	0	0	1	Data byte will be received and ACK will be returned
58h	Data byte has been received; NOT ACK has been returned	Read data byte or	1	0	0	X	Repeated START will be transmitted STOP condition will be transmitted and STO flag will be reset
		Read data byte or	0	1	0	X	
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted and STO flag will be reset

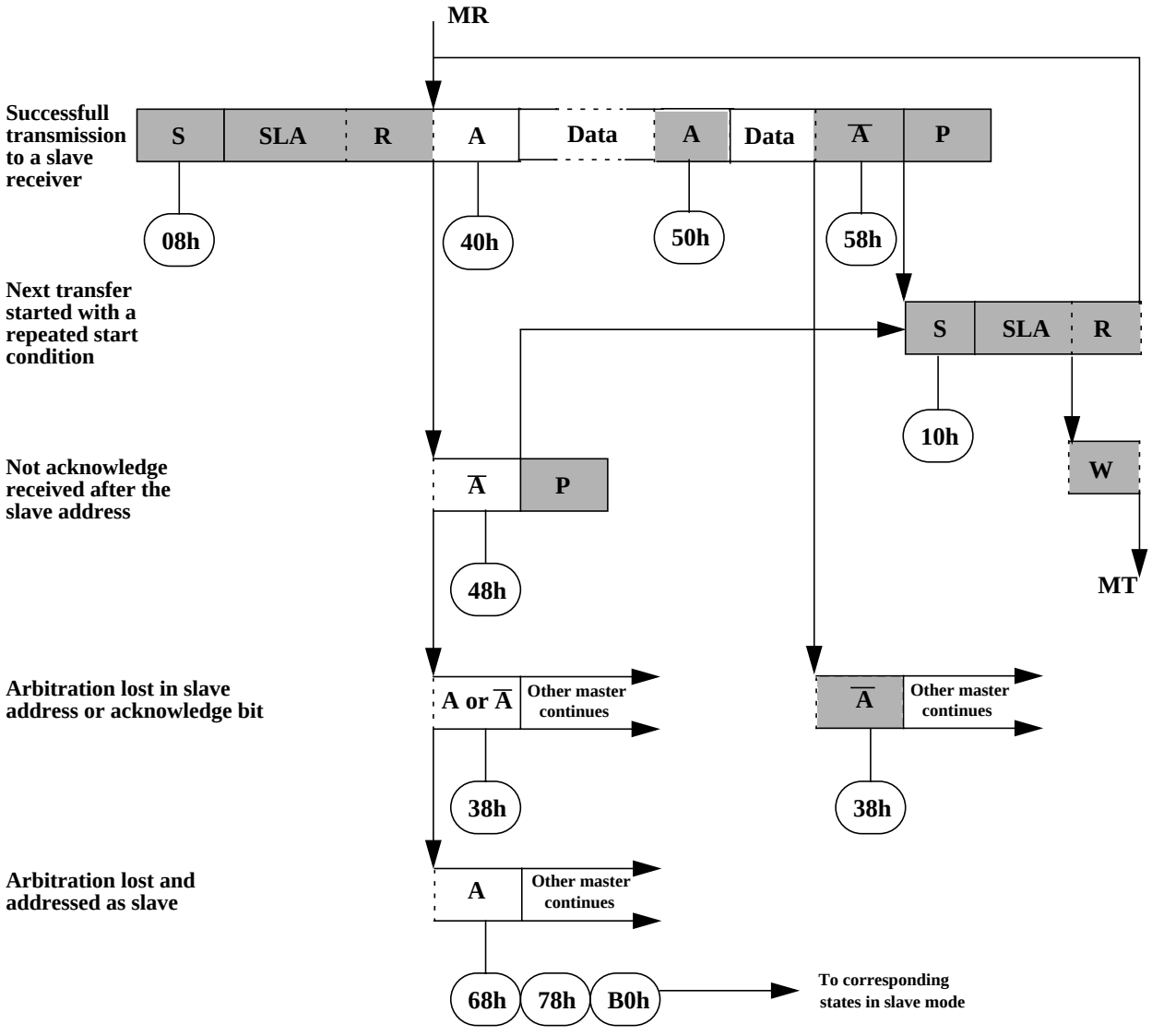


Figure 28. Format and state in the master receiver mode

Table 60. Status for slave receiver mode

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
60h	Own SLA+W has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
68h	Arbitration lost in SLA+R/W as master; own SLA+W has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
70h	General call address has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
78h	Arbitration lost in SLA+R/W as master; general call address has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
80h	Previously addressed with own SLA+W; data has been received; ACK has been returned	No SSDAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned
88h	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		Read data byte or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free
90h	Previously addressed with general call; data has been received; ACK has been returned	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned
98h	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		Read data byte or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		Read data byte or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free

Table 60. Status for slave receiver mode

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free

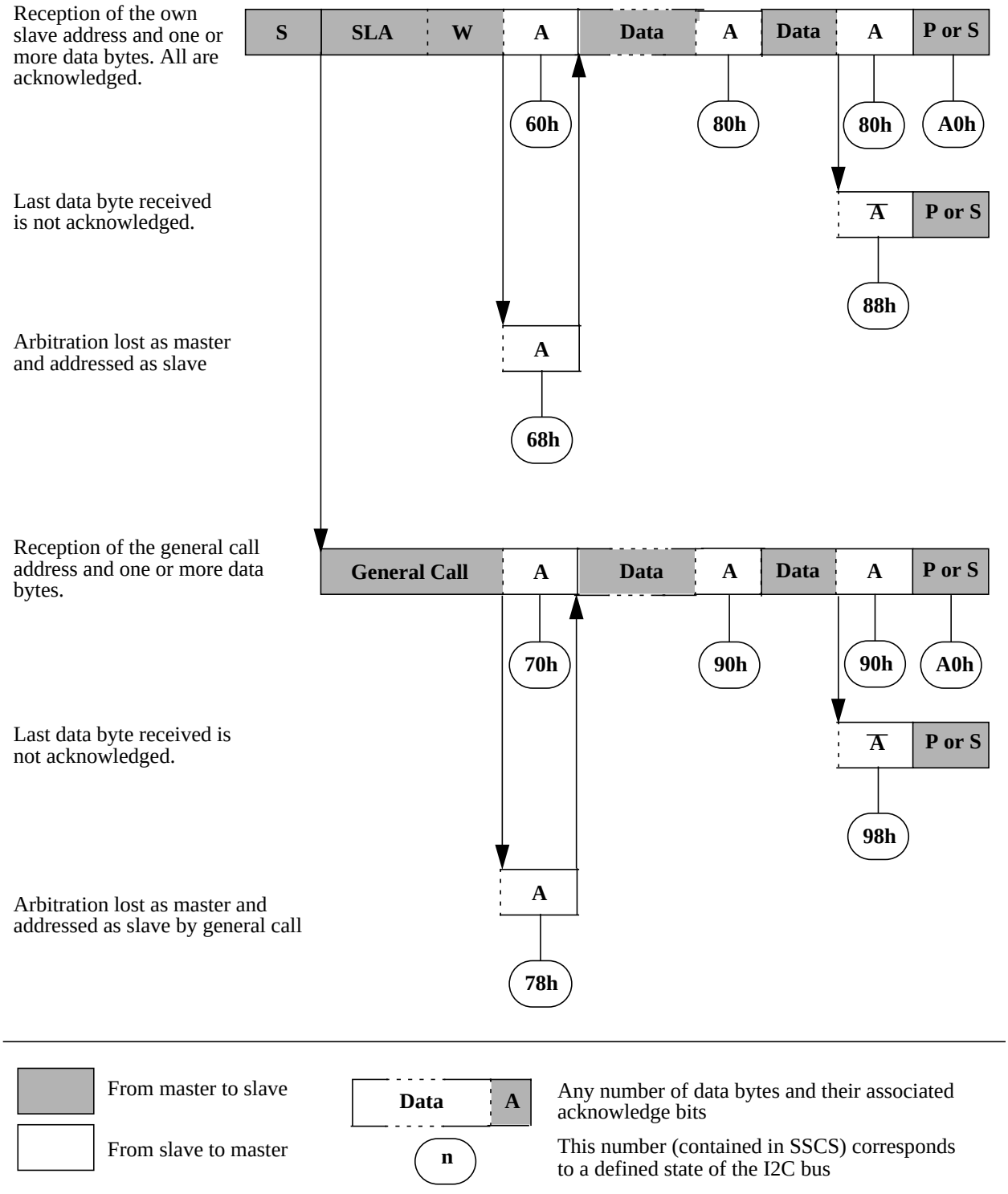


Figure 29. Format and state in the slave receiver mode

Table 61. Status for slave transmitter mode

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
A8h	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received
B0h	Arbitration lost in SLA+R/W as master; own SLA+R has been received; ACK has been returned	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received
B8h	Data byte in SSDAT has been transmitted; NOT ACK has been received	Load data byte or	X	0	0	0	Last data byte will be transmitted and NOT ACK will be received
		Load data byte	X	0	0	1	Data byte will be transmitted and ACK will be received
C0h	Data byte in SSDAT has been transmitted; NOT ACK has been received	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free
C8h	Last data byte in SSDAT has been transmitted (AA=0); ACK has been received	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free

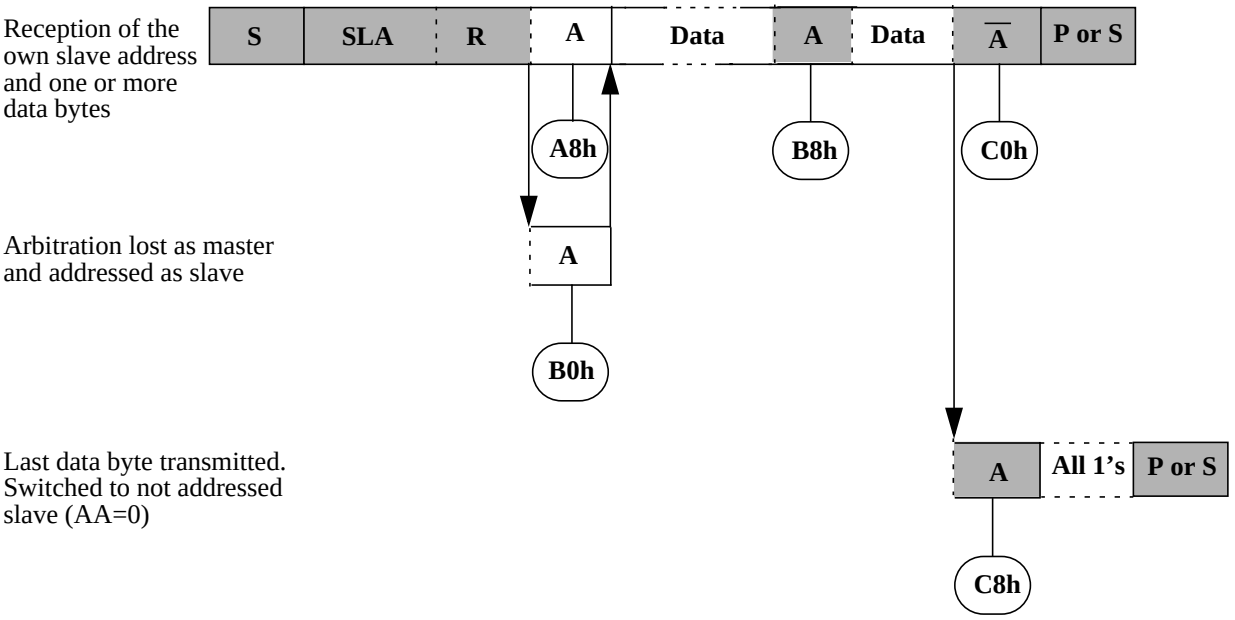


Figure 30. Format & state in the slave transmitter mode

Table 62. Status for miscellaneous states

status code (SSCS)	Status of the I^2C bus and I^2C hardware	Application software response					Next action taken by I^2C software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
F8h	No relevant state information available; SI= 0	No SSDAT action	No SSCON action				Wait or proceed current transfer
00h	Bus error due to an illegal START or STOP condition	No SSDAT action	0	1	0	X	Only the internal hardware is affected, no STOP condition is sent on the bus. In all cases, the bus is released and STO is reset

18.5 Registers

Table 63. SSCON (093h) - Synchronous Serial Control register (read/write)

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
7	6	5	4	3	2	1	0

Table 64. SSCON register - Reset value = 0000 0000b

Bit Number	Bit Mnemonic	Description
7	CR2	**Control Rate bit 2** See Table 55.
6	SSIE	**Synchronous Serial Interface Enable bit** Clear to disable SSLC. Set to enable SSLC.
5	STA	**Start flag** Set to send a START condition on the bus.
4	ST0	**Stop flag** Set to send a STOP condition on the bus.
3	SI	**Synchronous Serial Interrupt flag** Set by hardware when a serial interrupt is requested. Must be cleared by software to acknowledge interrupt.
2	AA	**Assert Acknowledge flag** Clear in master and slave receiver modes, to force a not acknowledge (high level on SDA). Clear to disable SLA or GCA recognition. Set to recognise SLA or GCA (if GC set) for entering slave receiver or transmitter modes. Set in master and slave receiver modes, to force an acknowledge (low level on SDA). This bit has no effect when in master transmitter mode.
1	CR1	**Control Rate bit 1** See Table 55
0	CR0	**Control Rate bit 0** See Table 55

Table 65. SSDAT (095h) - Synchronous Serial Data register (read/write)

SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
7	6	5	4	3	2	1	0

Table 66. SSDAT register - Reset value = FFh

Bit Number	Bit Mnemonic	Description
7	SD7	Address bit 7 or Data bit 7.
6	SD6	Address bit 6 or Data bit 6.
5	SD5	Address bit 5 or Data bit 5.
4	SD4	Address bit 4 or Data bit 4.
3	SD3	Address bit 3 or Data bit 3.
2	SD2	Address bit 2 or Data bit 2.
1	SD1	Address bit 1 or Data bit 1.
0	SD0	Address bit 0 (R/W) or Data bit 0.

Table 67. SSCS (094h) read - Synchronous Serial Control and Status register

SC4	SC3	SC2	SC1	SC0	0	0	0
7	6	5	4	3	2	1	0

Table 68. SSCS register : read mode - reset value = F8h

Bit Number	Bit Mnemonic	Description
0	0	Always zero
1	0	Always zero
2	0	Always zero
3	SC0	**Status Code bit 0** See Table 58 to Table 62
4	SC1	Status Code bit 1 See Table 58 to Table 62
5	SC2	**Status Code bit 2** See Table 58 to Table 62
6	SC3	**Status Code bit 3** See Table 58 to Table 62
7	SC4	**Status Code bit 4** See Table 58 to Table 62

Table 69. SSADR (096h) - Synchronous Serial Address register (read/write)

A7	A6	A5	A4	A3	A2	A1	A0
7	6	5	4	3	2	1	0

Table 70. SSADR register - Reset value = FEh

Bit Number	Bit Mnemonic	Description
7	A7	Slave address bit 7.
6	A6	Slave address bit 6.
5	A5	Slave address bit 5.
4	A4	Slave address bit 4.
3	A3	Slave address bit 3.
2	A2	Slave address bit 2.
1	A1	Slave address bit 1.
0	GC	**General call bit** Clear to disable the general call address recognition. Set to enable the general call address recognition.

19. Serial Port Interface (SPI)

19.1 SPI overview

This serial peripheral interface SPI is a high-speed synchronous serial I/O system.
It may be used for simple I/O expansion using external devices like shift registers, display drivers, converters, or in a multimaster configuration in which a controller may act as a master or a slave.

The SPI protocol handles a serial bit stream of eight bits to be shifted in and out at a programmed bit transfer rate (internally or externally).
Clock phase and polarity are software programmable to allow direct compatibility with a large number of peripheral devices.

Four basic signals are associated with this controller.
The data lines (master-out-slave-in or MOSI and master-in-slave-out or MISO) conduct data.
The SCK carries the serial clock information while the $\overline{SS}$ line asserts the Slave Selection.

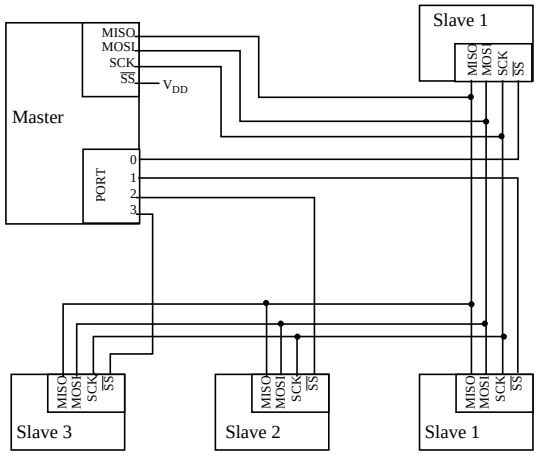


Figure 31. : SPI Master/Slaves connection

19.2 Features

- Full-duplex, three-wire synchronous transfers
- Master or Slave operation
- 4 programmable master bit rates
- Programmable clock polarity and phase
- Write collision flag protection
- Master-Master mode fault protection capabilty

19.3 Signal description

19.3.1 Serial Clock (SCK)

For Serial communications, one controller, the master, initiates data transfer by sending SCK signal. Data is enabled out of both attendee on one edge of the clock, and latched into on the opposite clock edge. Master and slave send and receive data at the same time (full duplex transmission).

19.3.2 Slave Select ($\overline{SS}$)

The $\overline{SS}$ line selects master/slave mode. It must stay low for any message for a slave. It's obvious that only one master ($\overline{SS}$ high level) can drive the network.

When the $\overline{SS}$ line is detected low while the controller is configured as a Master (in SPI mode), the control bits MSTR and SPE are cleared, which causes the SPI to be disabled (MOSI is released) and to reset the current transfer cycle. The MODF flag bit in the SPSR is also set to indicate to the master device that another device is attempting to become a master. In addition, an interruption is generated if the bit SPIE is set.

Two devices attempting to be masters are normally the result of a software error; however, a system could be configured which would contain a default master which would automatically "take-over" and restart the system.

19.3.3 Master In Slave Out (MISO) / Master Out Slave In (MOSI)

The MISO (resp. MOSI) is data input (resp. output) for a master, while the opposite for a slave. A word is transmitted most significant bit first, least significant bit last. When not selected ($\overline{SS}$ high), the MISO pin of a slave device is high-impedance driven.

The SCK line is used to synchronize the exchange of data through the device's MISO and MOSI pins. Since it's driven by the master, it's an input for all slaves.

19.4 Special Function Registers (SFR)

There are three registers in the module that provide control, status and data storage functions. These registers are described in the following paragraphs

19.4.1 Serial Peripheral Control Register (SPCR)

Bit Number	Mnemonic	Description
7	SPIE	Serial Peripheral Interrupt Enable 1 = Generate an interruption if SPIF=1 or MODF=1 0 = Interrupts disabled
6	SPE	Serial Peripheral System Enable 1 = SPI system on (pull-up transistors at SPSCK, MOSI and MISO) 0 = SPI system off
5	DWOM	SPI Wire-Or Mode : This R/W bit disables the pull-up devices on pins SPSCK, MOSI and MISO, so that those pins become open-drain outputs 1 = Open drain for wired-or of SPSCK, MOSI and MISO 0 = Normal push pull SPCK, MOSI and MISO Cleared by Reset signal
4	MSTR	Master Mode Select 1 = Master Mode (defaut after reset) 0 = Slave Mode
3	CPOL	Clock Polarity 1 = SCK line idles high 0 = SCK line idles low
2	CPHA	Clock Phase (set by defaut after reset) This bit selects one of two clock protocol
1	SPR1	SPI Clock Rate Select (See Note) 0 0 : internal clock divided by 2 0 1: internal clock divided by 4 1 0 : internal clock divided by 16 1 1: internal clock divided by 32
0	SPR0	

Table 71. : SPCR SPI Control Register

- SFR address : C3H
- Reset value : 00010100b

Note :

$$Internalclock = \frac{F_{XTAL}}{2 \times (256 - PS)}$$

PS : oscillator prescaler value between 0 and 255

19.4.2 Serial Peripheral Status Register (SPSCR)

Bit Number	Mnemonic	Description
7	SPIF	SPI Transfer Complete Flag 1 = Automatically set when data transfer is complete between processor and external device. An interruption is generated if the bit SPIE is set. 0 = Cleared by a read of SPSR (with SPIF=1), followed by an access (read or write) of the SPDR.
6	WCOL	Write Collision If CPHA=0, transfer begins when SS goes low and ends when SS goes high after eight clock cycles on SCK. If CPHA=1, transfer begins the first time SCK becomes active while SS is low and ends when the SPIF flag gets set. 1 = Automatically set when an attempt is made to write to the SPI data register while data is being transferred. 0 = Cleared by a read of SPSR (with WCOL=1), followed by an access (read or write) of the SPDR
5	-	
4	MODF	Mode Fault This bit indicates the possibility of a multi-master conflict for system control and therefore allows a proper exit from system operation to a reset or a default system state. 1 = Automatically set when a master device has its SS pin pulled low. 0 = Cleared by a read of SPSR (with MODF=1), followed by a write to the SPCR. Setting the MODF bit affects the internal serial peripheral in the following ways: An SPI interrupt is generated if SPIE=1, The SPE bit is cleared. It disables the SPI, The MSTR bit is cleared, thus forcing the device into the slave mode.
3	-	
2	-	
1	-	
0	-	

- SFR address : C4H
- Reset value : 00000000b
- Remark : SPSCR is accessible in Read mode only , so Read-Modify-Write instructions should not be used on SPSCR register .

19.4.3 Serial Peripheral Data Register (SPDR)

Read	R7:0	Receive Data Register
Write	T7:0	Transmit Data register

- SFR address : C5H
- Reset value : XXXXXXXXb

- Remark : Read-Modify-Write instructions should not be used on SPDR register, since the buffer read is not the same as the buffer written .

The Serial Peripheral Data Register is used for transmit or receive data on the serial bus .
In a Master device, only a write to this register will initiate a transmission .
In a Slave device, a write to this register does not initiate a transmission .

At the completion of transmitting a byte of data, the SPIF status bit is set both in the Master and the Slave devices .
During the clock cycle that the SPIF is being set, a copy of the received data byte is moved in a buffer .
When reading the SPDR register, it is actually the buffer which is read .

When writing a data into the SPDR, the data is not buffered, and directly loaded into the shift register for transmission .

The ability to acces the serial data register is limited when a transmission is taking place . See "Error conditions" section for details .

19.5 Operating modes

19.5.1 Master-slave operation :

The SPI module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs .

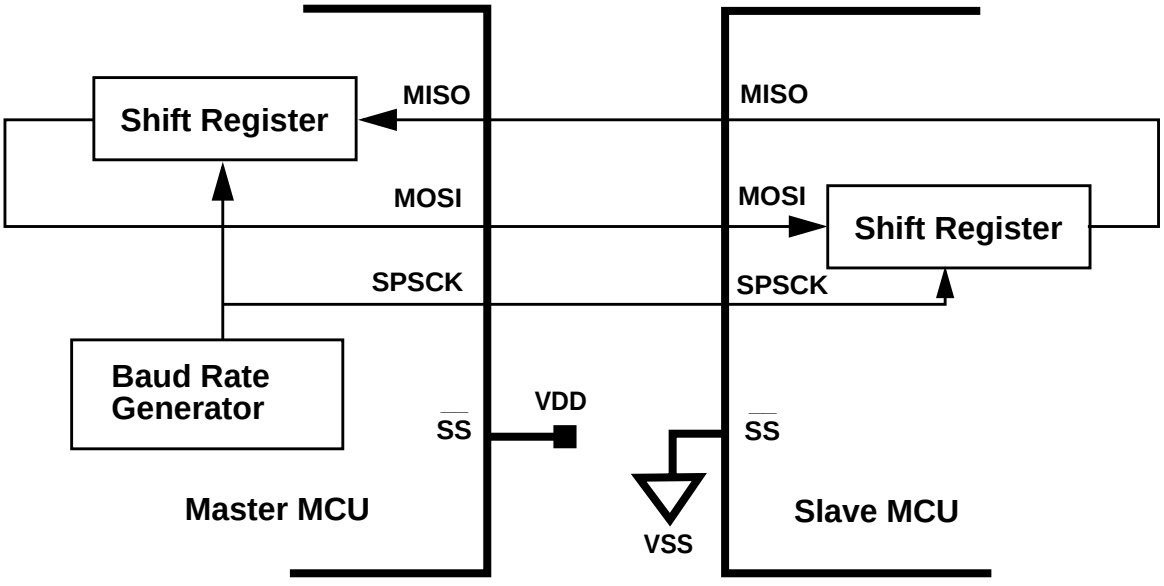


Figure 32. : Full-duplex master-slave connection

19.5.2 Master mode :

The SPI operates in Master mode when the SPI Master bit MSTR is set .
In Master mode, the SPSCK pin is the output of the serial clock for the Slave MCU .
Only one Master SPI module can initiate transmissions. Software begins the transmission from a master SPI module by writing to the SPI data Register .
The byte begins shifting out on the MOSI pin, under the control of the serial clock SPCLK .

Simultanously, another byte shifts in from the slave on the MISO pin.
The transmission ends when SPIF flag becomes set, this operation transfering the received byte into the SPI Data Register SPDR .

19.5.3 Slave mode :

The SPI operates in Slave mode when the SPI Master bit MSTR is clear .
In Slave mode, the SPSCK pin is the input for the serial clock from the Master MCU .
Before a data transmission occurs, the $\overline{SS}$ pin of the slave MCU must be at '0' , and must be remain low until the transmission is complete .
In a salve SPI module, data enters the shift register under the control of the serial clock from the master SPI module .

A slave SPI must complete the write to the data register at least one bus cycle before the master SPI starts a transmission .
When the clock phase bit CPHA is high, the first edge of SPSCK starts a transmission.
When CPHA is low, the falling edge of $\overline{SS}$ starts a transmission .

19.6 Transmission format :

19.6.1 Principle :

During SPI transmission, data is simultaneously shifted out serially, and shifted in serially .
The serial clock SCK from master SPI synchronizes both shifting and sampling on the two lines MOSI and MISO .
Software can select four transmission formats using two bits CPOL and CPHA from SPCR register .
The couple CPOL/CPHA must be identical for the master SPI and the communicating slave SPI , but master can change phase and polarity to communicate with peripheral slaves having different requirements .

19.6.2 Clock polarity :

Clock polarity is specified by the CPOL control bit, and selects that serial clock SCK is active high (CPOL = 0) or low (CPOL = 1)
CPOL has no effect on the transmission format.

19.6.3 Phase control :

When CPHA = 0 , the first SCK edge is the MSB sample strobe .
In this case, the slave must begin to drive its MISO pin before this first SCK edge, so the falling edge of $\overline{SS}$ is used for start the transmission.

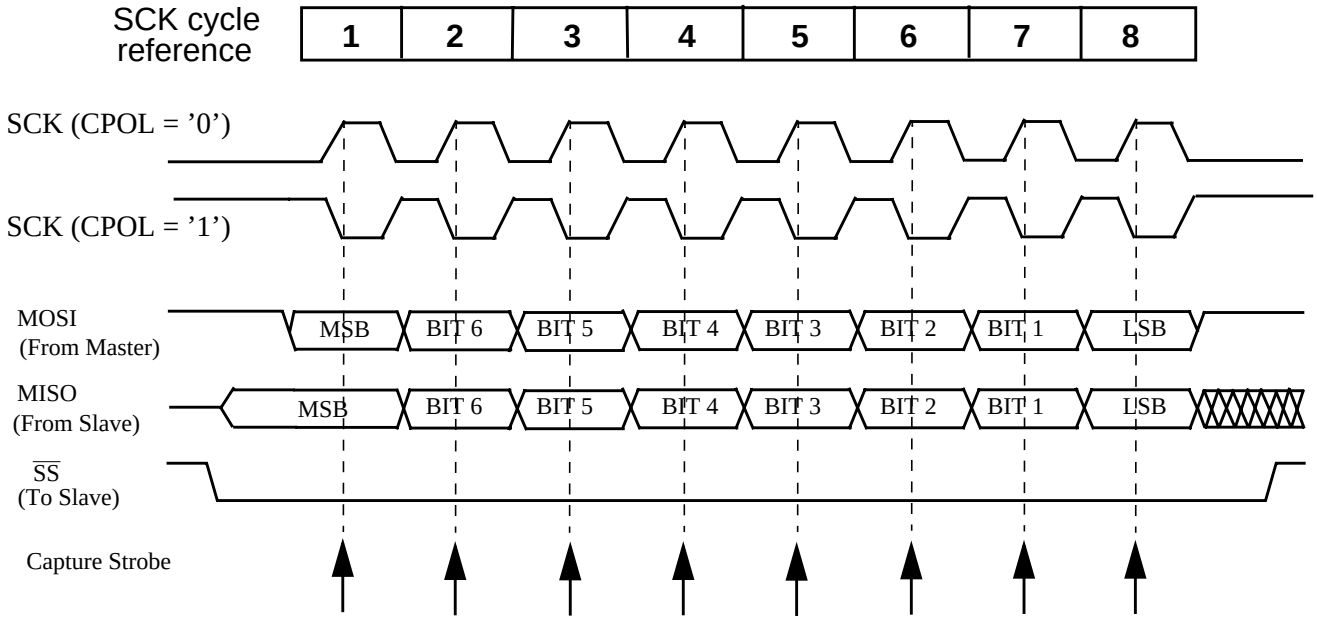


Figure 33. Transmission format with CPHA = 0

The slave must toggle the $\overline{SS}$ pin of the communicating slave between each byte transmitted , otherwise a write collision occurs (see "Error Conditions" section) :

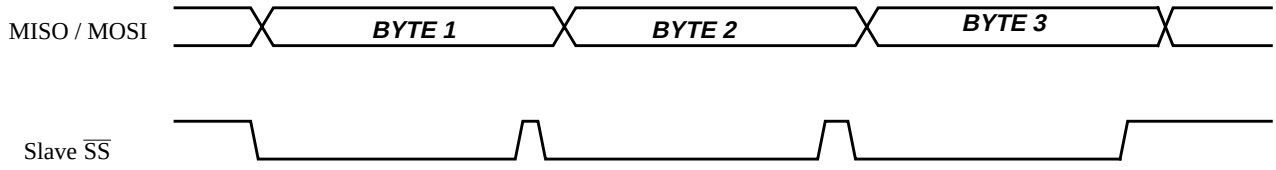


Figure 34. $\overline{SS}$ Timing with CPHA = 0

When CPHA = 1 , the master begins driving the MOSI pin on the first SCK edge .
So the slave uses this first SCK edge as a start transmission signal.

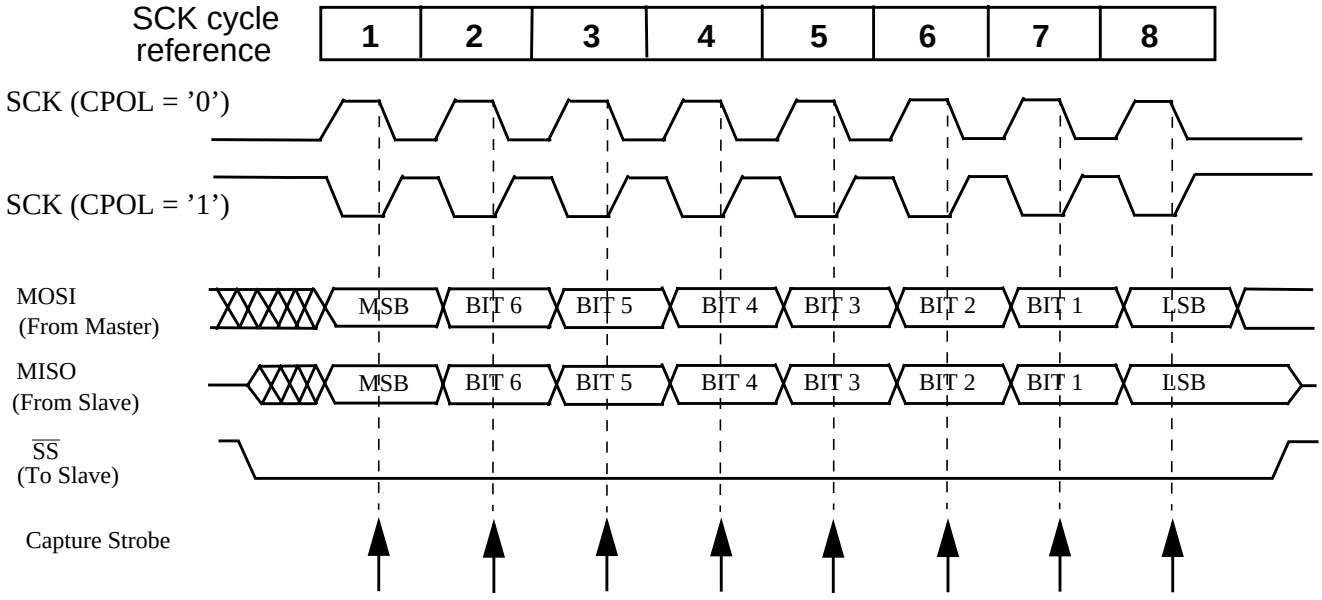


Figure 35. Transmission format with CPHA = 1

The $\overline{SS}$ pin of the slave can remain low between transmissions :

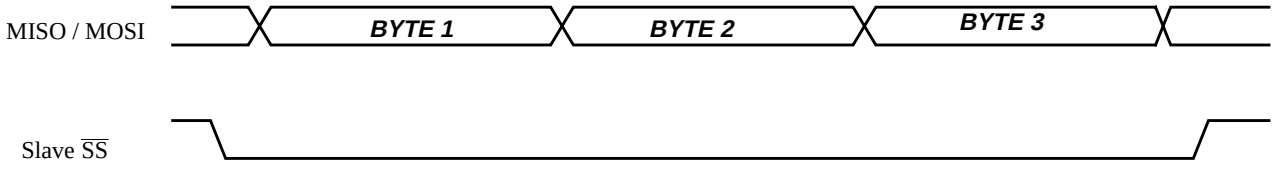


Figure 36. $\overline{SS}$ Timing with CPHA = 1

19.7 Power saving modes :

19.7.1 Idle mode :

Idle mode is achieved by using any instruction that writes into PCON.0 sfr

In this mode, CPU clock (Ck) is stopped, but peripherals like SPI continue to run as CkIdle clock remains active .

19.7.2 Power down mode :

Power down mode is achieved by using any instruction that writes into PCON.1 sfr

In this mode, all internal clock are stopped, so the SPI cannot transmit nor receive any data .

If a transmission was active during instruction that writes into PCON.1, the transmission stops irreparably .

19.8 Error conditions:

19.8.1 Mode fault :

The mode fault error indicates that the level on the Slave Select pin $\overline{SS}$ is inconsistant with the mode of the SPI .

- In a Master SPI, the MODF is set if the $\overline{SS}$ becomes '0' .
  - SPE is cleared (SPI disabled)
  - MSTR is cleared

Clearing the MODF flag is accomplished by a software sequence of reading the status SPSCR ,followed by a write of the SPCR control register .

19.8.2 Write collision :

When a write into the serial data register occurs while a data transfers was taking place, the write collision status bit (WCOL) becomes set .
WCOL bit does not cause an interruption, and the transfer continues uninterrupted.

- A collision in a Master device is defined as a write of the serial data register while the internal clock SCK is in progress .
- A collision in a Slave device is defined in two separate modes :
  - When CPHA = '0', the collision occurs when it attempts to write the serial data register after its $\overline{SS}$ has been pulled low by the Master device .
    When low, $\overline{SS}$ signal freezes the data of its serial data register, and does not allow it to be altered if CPHA = '0' .
    So, when CPHA = '0', the Master device must raise the $\overline{SS}$ pin of the slave devices between each byte it transfers .
  - When CPHA = '1', a collision occurs if the Slave device attempts to write its serial data register after the first clock edge of SCK .

Clearing the WCOL flag is accomplished by a software sequence of accessing the status register SPSCR, followed by an acces (read or write) to the serial data register SPDR .

19.8.3 Overrun :

When a Master device sends several bytes, if the Slave has not responded to its first SPIF, the next received bytes are lost .
When reading the SPDR register, the first byte received is returned .

19.9 Interruptions :

19.9.1 Interrupt requests :

Two SPI interrupt requests can be generated, and share the same CPU interrupt vector, depending on the following conditions :

FLAG	Conditions	Request	SPI Vector Address
SPIF (SPSCR.7) Transfer Completed Flag	SPIE = 1 (see Note)	SPI Transmitter Interrupt request	4BH
MODF (SPSCR.4) Mode Fault	SPIE = 1 (See Note)	SPI Receiver/Error Interrupt request	

Note : Interrupt register IE1 must also be programmed to enable the SPI interrupt

19.10 Resetting the SPI :

An hardware Reset completly resets the SPI by driving low RESETB signal .

The SPI registers are left in the following states :

- SPCR = 00010100B => only MSTR and CPHA are set
- SPSCR = 00000000B

20. On-Chip LCD Controller

PAROS includes a low power CMOS LCD controller and driver designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5x8 dot format and a maximun of 60 icons. The chip contains a character generator and displays alphanumeric and kana characters. The LCD controller is controlled through registers located into the SFR area.

The different blocks which compose the LCD controller are described below.

20.1 Address Counter

The Address Counter assigns addresses to the DDRAM, CGRAM and SEGRAM for reading and writing and is set by writing in the LCDAC register.

20.2 Display data RAM (DDRAM)

The display data RAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown hereafter.

The DDRAM addresses that can display characters are 00h to 4Fh, the DDRAM addresses that can display icons are 50h to 5Bh, the last addresses (5Ch to FFh) can be used by the user.

The address range for 1-line display is 00 to 4Fh. for a 2-line display from 00 to 27h (line 1) and 28 to 4Fh (line 2). For a 4-line display from 00 to 13h, 14h to 27h, 28h to 3Bh and 3Ch to 4Fh for respectively lines 1, 2, 3 and 4. When the display is shifted all the lines are shifted.

When data is written into the DDRAM wrap around occurs from 4Fh to 00 for the displayed DDRAM, from 5Bh to 50h for the SegRAM and from FFh to 5Ch for the user RAM.

Care has to be taken on the fact that the the DDRAM has a greater address range than standard Displays have digits. If one line of DDRAM is written completely, the next line will be addressed by the DDRAM.

20.3 Character Generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5x8 dot format from 8-bit character codes.

20.4 Character Generator RAM (CGRAM)

Up to 16 characters may be stored in the character generator RAM. the and CGRAM use a common address space of which the first column is reserved for CGRAM (see Table 73. and Figure 40.).

20.5 Segment Icon RAM (SEGRAM)

The segment icon RAM is located in the DDRAM at addresses 50h to 5Bh. During 1-line display mode, C0 and C17 makes the data of SEGRAM enable to display icons. When used in 2/4 line display mode C0 and C33 does that. Its higher 2-bits are blinking control data and the lower 5-bits are pattern data (see Table 74. and Table 75.).

20.6 Cursor control Circuit

The cursor control circuit generates the cursor (underline and/or character blink) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address, the cursor will be inhibited.

20.7 Oscillators B and C and Timing generator

The LCD controller time base can be either the external oscillator B, or the internal RC oscillator C (default after a reset).

20.8 LCD Driver Circuit

LCD Driver circuit has 34 commons and 60 segments for LCD driving. Data from SEGRAM/CGRAM/CGROM is transfered to 60 bit segment latch serially, and then it is stored to 60 bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 60-bit segment latch.

In case of 1-line display mode, COM0-COM17 have 1/17 duty, and in 2-line or 4-line mode, COM0-COM33 have 1/33 duty ratio.

Unused output should be left unconnected.

20.9 Programming the LCD controller

The LCD controller is managed through the Instruction register (LCDIR), the Control Register (LCDCON)and the data register (LCDDR). BUSYF bit located into the LCDCON register, is set to one by the LCD controller during the treatment of the instruction posted into the LCDIR or LCDDR register. The CGRAM/DDRAM/SEGRAM are read or written though the Data register (LCDDR). The instruction register stores instruction code from MCU such as ‘Display Clear’ and address information for the DDRAM, CGRAM and SEGRAM. The instruction register can’t be read by the MCU. The Data register temporally stores data to be read in the DDRAM, the CGRAM or the SEGRAM.The address counter register (LCDAC) is directly accessible by the MCU core.

The BUSYF bit indicates the free/busy status of the internal state machine of the LCD controller. If BUSYF is set to one by the LCD Controller, it indicates that no more instructions will be accepted. When a write is performed into LCDIR during BUSYF set to one, the write is not taken into account by the LCD controller. BUSYF is located into LCDCON register.

20.10 Voltage regulator

One of the PCA channel is used as voltage regulator through an integrator connected to V1 input (see typical application diagram). Knowing that each PCA channel located into PAROS has an independent time base, one can be used in PWM mode though a thermic resistor to adjust the LCD voltage for a perfect contrast.

Three bits located in LCDCON (VCP2.VCP1 and VCP0) allow to program the voltage converter in off, V_{CC} and 5V until 9V in 1 volt steps. The needed voltage steps are fixed by a resistor chain connected to V1:V5.

20.11 LCD Controller Register

20.11.1 LCDCON Register

This register allows to know if the controller is writting or reading the common resources (DDRAM, ...).It allows also to setup the voltage converter and the selection of the oscillator A, B and C.

Table 72. LCDCON Register

LCDCON - LCD Control register (E3h)

7	6	5	4	3	2	1	0
BUSYF	**VCP2**	**KEYBONB**	**LCDRST**	**M**	**N**	**VCP1**	**VCP0**

Bit Number	Bit Mnemonic	Description
7	BUSYF	**Busy Flag** Set to one by the LCD controller to signal that the LCD controller is busy. Clear by the LCD controlled to signal that the LCD controller is ready to accept another instruction
6	VCP2	**Voltage Converter Programming bit 2**
5	KEYBONB	**Keyboard on/off** When set to one, the keyboard trame on S0 to S15 is off When cleared, the keyboard trame on S0 to S15 is on
4	LCDRST	**Display controller reset** When clear, the display logic controller is reseted. No operation can be done. When set, the display logic controller is running. It is mandatory that this bit is cleared when the display controller clock is switched (OSCB or OSCC).
3	M	**Display configuration** M N Comments 0 0 1 line x 24, MUX 1:17 0 1 reserved 1 0 2 lines x 24, MUX 1:33 1 1 4 lines x 12 MUX 1:33
2	N	
1	VCP1	**Voltage Converter Programming bit1 and bit0** VCP2 VCP1 VCP0 Comments 0 0 0 Voltage converter off 0 0 1 Voltage V_{CC} (5V or 3V) 0 1 0 Voltage 5V (only if V_{CC} = 3V) 0 1 1 Reserved 1 0 0 Voltage 6V 1 0 1 Voltage 7V 1 1 0 Voltage 8V 1 1 1 Voltage 9V
0	VCP0	

Reset Value = 0X00 0000b

20.11.2 LCDIR Register

This register contains the opcode of the instruction to execute by the LCD controller.

LCDIR - Instruction register for LCD (E6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

20.11.3 LCDDR Register

This register contains the data to write or to read to/from the LCD controller. Before writting or reading to this register, the R/W bit in the LCDIR register has to be setup for the read or write operation.

LCDDR - Data register for LCD (E7h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

20.11.4 LCDAC Register

This register contains the address to access to the DDRAM, CGRAM or SEGRAM. The selection of the RAM is done by setting the AS0 bit in the LCDIR register.

LCDAC - Address Counter register for LCD (E5h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

20.11.5 DDRAM - to Display Mappings

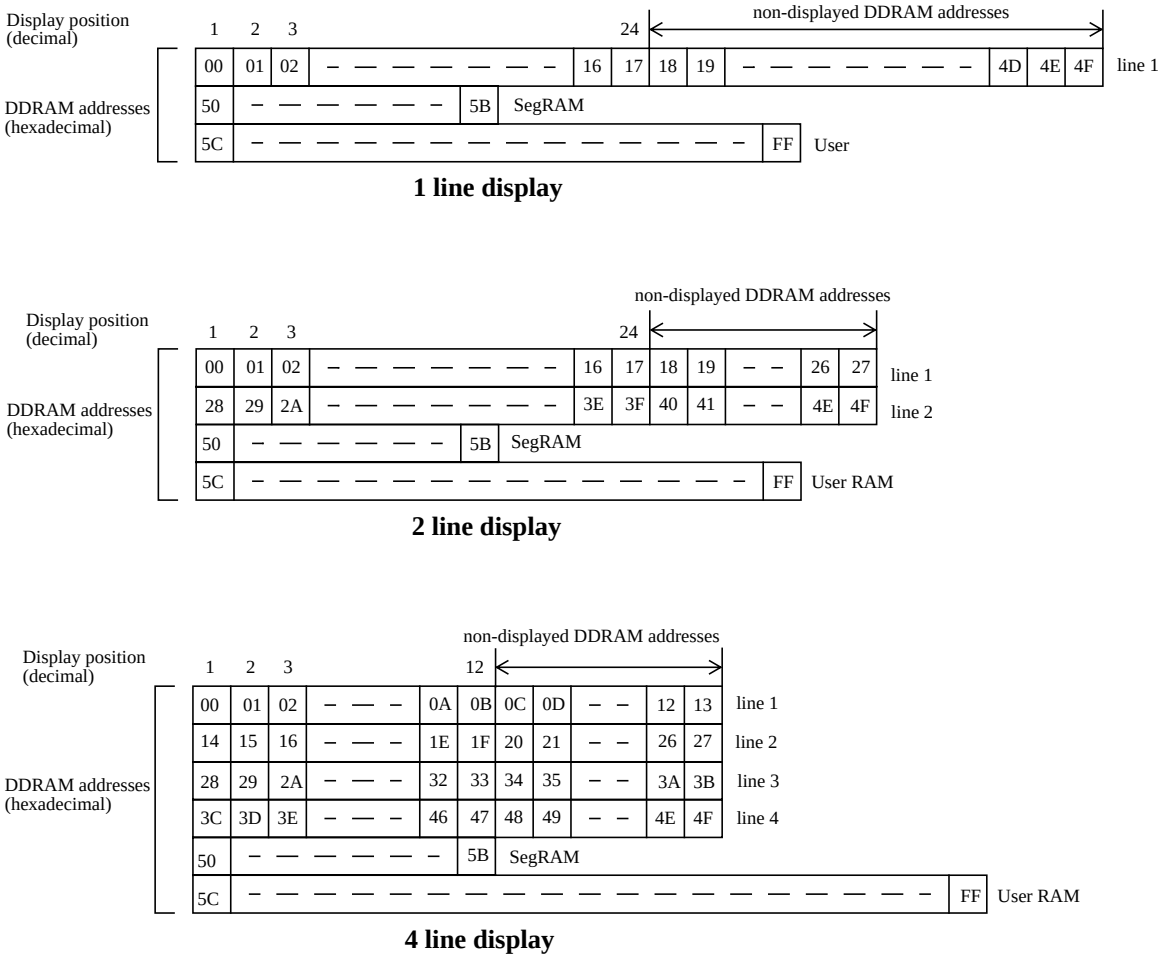


Figure 37. DDRAM-to-display mapping; no shift.

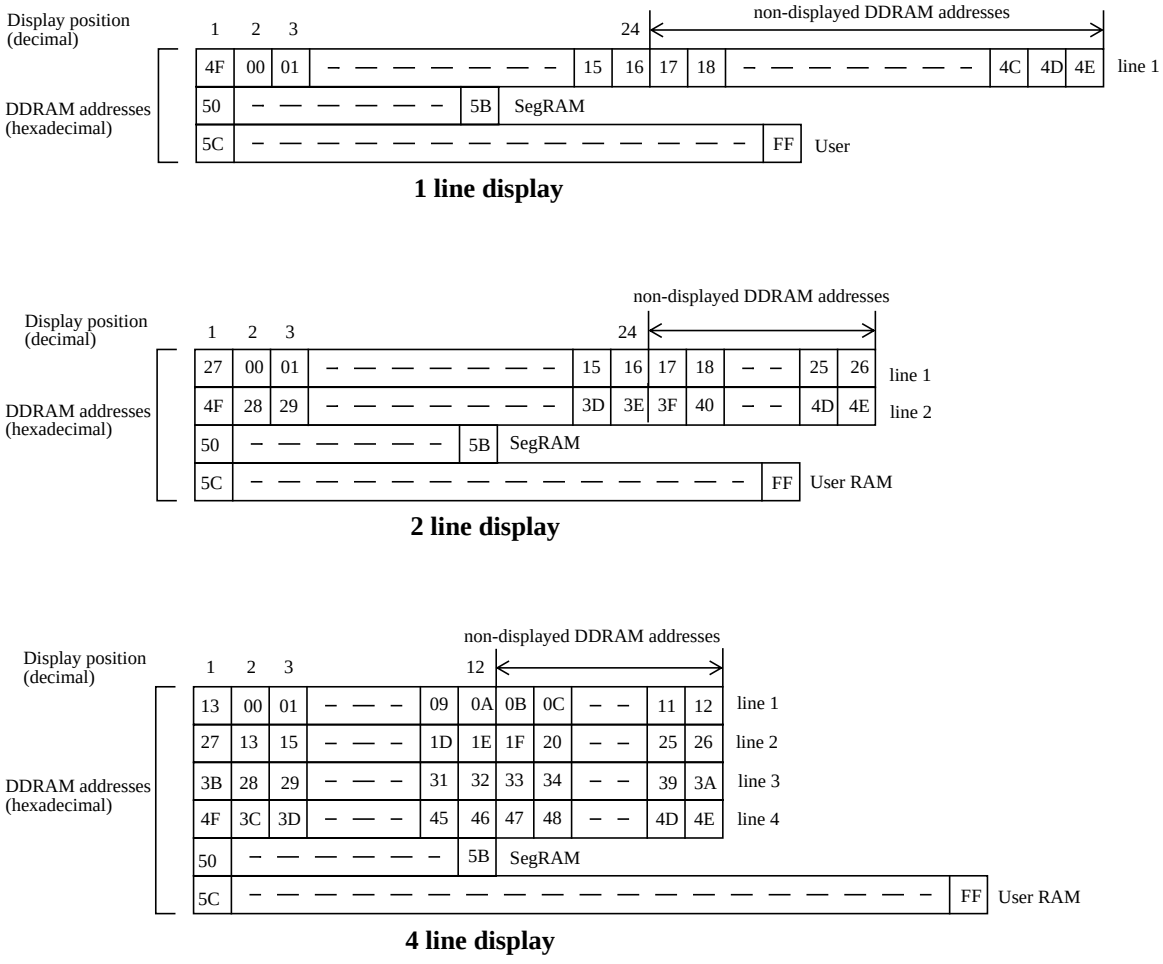


Figure 38. DDRAM-to-display mapping; right shift.

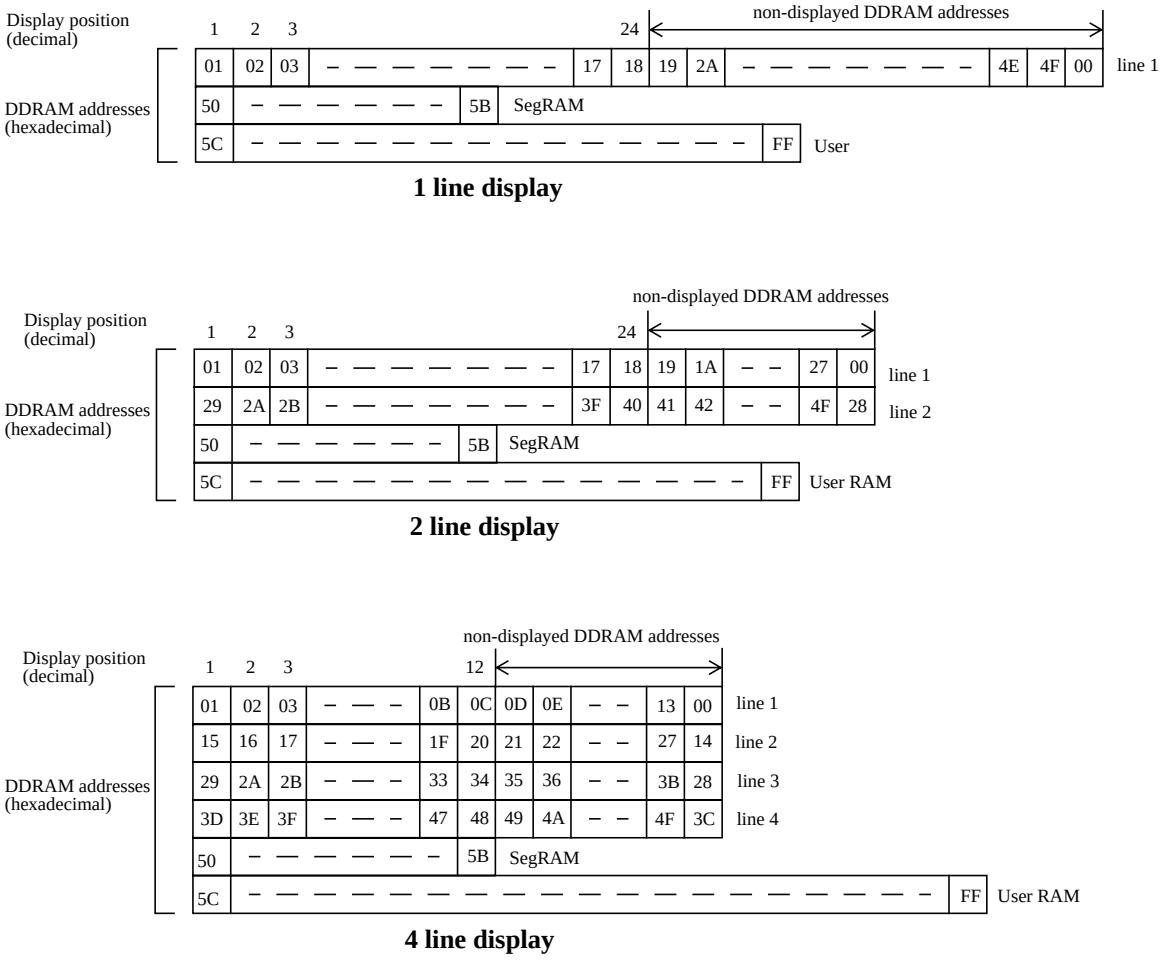


Figure 39. DDRAM-to-display mapping; left shift.

Table 73. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM address (upper 4 bits = 0000)												Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	P4	P3	P2	P1	P0	pattern 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	
			:							:		0	0	1	1	0	0	0	1	
			:							:		0	1	0	1	0	0	0	1	
			:							:		0	1	1	1	1	1	1	1	
			:							:		1	0	0	1	0	0	0	1	
			:							:		1	0	1	1	0	0	0	1	
			:							:		1	1	0	1	0	0	0	1	
			:							:		1	1	1	0	0	0	0	0	
:								:		:		:								:
0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	**pattern 16**
			:							:		0	0	1	1	0	0	0	1	
			:							:		0	1	0	1	0	0	0	1	
			:							:		0	1	1	1	1	1	1	1	
			:							:		1	0	0	1	0	0	0	1	
			:							:		1	0	1	1	0	0	0	1	
			:							:		1	1	0	1	0	0	0	1	
			:							:		1	1	1	0	0	0	0	0	

(5x8 dot Character pattern example)

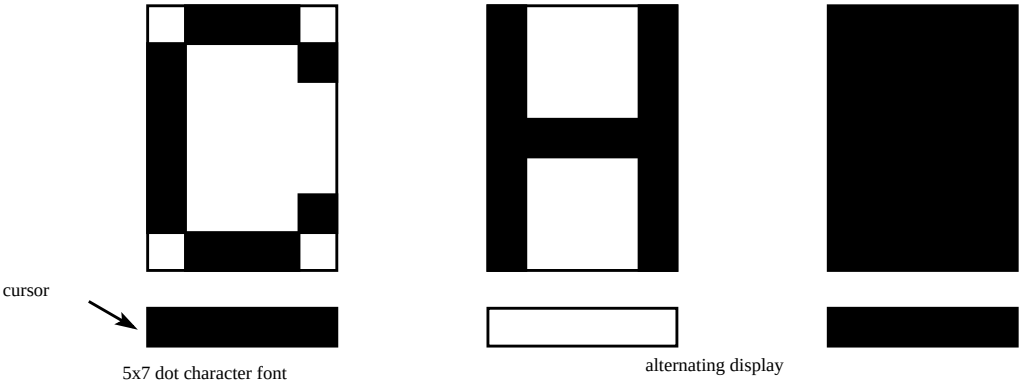


Figure 40. Cursor and blink display examples

Table 74. Relationship between SEGRAM address and display pattern

SEGRAM address				SEGRAM data display pattern							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	x	S0	S1	S2	S3	S4
0	0	0	1	B1	B0	x	S5	S6	S7	S8	S9
0	0	1	0	B1	B0	x	S10	S11	S12	S13	S14
0	0	1	1	B1	B0	x	S15	S16	S17	S18	S19
0	1	0	0	B1	B0	x	S20	S21	S22	S23	S24
0	1	0	1	B1	B0	x	S25	S26	S27	S28	S29
0	1	1	0	B1	B0	x	S30	S31	S32	S33	S34
0	1	1	1	B1	B0	x	S35	S36	S37	S38	S39
1	0	0	0	B1	B0	x	S40	S41	S42	S43	S44
1	0	0	1	B1	B0	x	S45	S46	S47	S48	S49
1	0	1	0	B1	B0	x	S50	S51	S52	S53	S54
1	0	1	1	B1	B0	x	S55	S56	S57	S58	S59

Control Bit			Blinking Port
BE	B1	B0	
0	x	x	No blink
1	0	0	No blink
1	0	1	D4
1	1	x	D4~D0

1. B0, B1: Blinking control bit
2. S0~S59: Icon pattern ON/OFF
3. “X”: Don’t care

Table 75. CGROM Character Code Table

lower 6 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

Characters 1 to 16 (when the upper 4 bits are zero) will be mapped in the CGRAM

20.12 Instructions

The instruction is written into the LCDIR register. The table 1 shows the instruction set supported by the LCD controller. Only two PAROS registers, the instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.

The PAROS operation is controlled by the instructions shown in Table 59. together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

- 1- Designate PAROS functions such as display format, data length, etc...
- 2 -Set internal RAM addresses
- 3- Perform data transfer with internal RAM
- 4- Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than “Read busy flag and address” will be executed. Because the Busy Flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction execution time. An instruction sent while Busy Flag (BF) is HIGH will not be executed.

Table 76. Instruction Description

Instruction									Description
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and set DDRAM address to “00H” from AC
Return Home	0	0	0	0	0	0	1	x	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed
Entry Mode Set	0	0	0	0	0	1	I/D	S	Assign cursor moving direction I/D = “1” : increment, I/D = “0” : decrement and display shift enable bit. S = “1” : make display shift of the enabled lines by the DS4 - DS1 bits in the Shift Enable instruction S = “0” : display shift disable
Display ON/OFF Control	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = “1” : display on D = “0” : display off C = “1” : cursor on C = “0” : cursor off B = “1” : blink on B = “0” : blink off
Cursor or Display Shift	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C = “1” : display shift S/C = “0” : cursor shift R/L = “1” : shift to right R/L = “0” : shift to left
Icon Blink selector	0	0	1	x	x	x	x	BE	Icon Blink Enable: BE = 0, Icon Blink Enable BE = 1, Icon Blink Disable
Set RAM selector	0	1	x	x	x	R/W	x	AS	Read/Write operation: R/W = 1 : read R/W = 0 : write Address pointer selection: AS = 0, DDRAM/SEGRAM AS = 1, CGRAM

**”X” : don’t care*

20.13 Display Clear

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “1”).

20.14 Return Home

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

20.15 Entry Mode Set

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)

When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.

When S = “High”, after DDRAM write or read, the display is shifted to the right (I/D = “0”) or to the left (I/D = “1”). But it will seem as if the cursor does not move.

When S = “Low”, after DDRAM write or read, the cusor/blink is shifted to the right (I/D = “0”) or to the left (I/D = “1”).

During CGRAM/SEGRAM read/write operation, shift of display/cursor is not performed.

20.16 Display ON/OFF Control

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit.

When D = “High”, entire display is turned on.

When D =”Low”, display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit.

When C = “High”, cursor is turned on.

When C = “Low”, cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit.

When B = “High”, cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = “Low”, blink is off.

20.17 Cursor or Display Shift

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display.

This instruction is used to correct or search display data.

During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.

When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.

Note that display shift is performed simultaneously in all the line.

When display shift is perfomed, the contents of address counter are not changed.

During low power consumption mode, display shift may not be performed normally.

Table 77. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by 1
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

20.18 Set Icon Blink selector

Table 78. Blink Icon selector according to BE bit

BE	Operation
0	Icon Blink is Enable
1	Icon Blink is Disable

When BE = “High”, icon blink is on

When BE = “Low”, icon blink is off

20.19 Set read or write operation and set RAM selector

R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	x	X	R/W		AS0

- R/W

Writing and reading RAM is done by writing or reading the LCDDR register. The LCD controller need to be advised when a reading operation is necessary (in order to load the LCDDR register with the contents of the selected RAM).

Then the R/W bit must be set to one before any reading of the LCDDR register, and it must be clear before any write in this register.

If LCDDR is read while R/W is 0, the value will be unsignificant and if LCDDR isi wrote while R/W is 1, this operation won't affect LCDDR.

- AS

Writing and reading RAM affect the last selected RAM. AS bit selects the RAM that will be affected by the next write or read operation:

AS	Selected RAM
0	DDRAM/SEGRAM
1	CGRAM

20.20 Read Busy Flag

Before any following instruction, writing in LCDIR, LCDDR or LCDAC or reading LCDDR, the busy flag must be check to ensure the LCD controller is not busy.

20.21 Write data to RAM (R/W = 0)

Writing a data in a RAM is done when the R/W bit is low and by writing a data in the LCDDR register by using the C51 instruction set. It is not recommanded to use read-modify-write instructions.

The selection of RAM from DDRAM, CGRAM or SEGRAM, is set by the set RAM selector instruction.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

20.22 Read data from RAM (R/W = 1)

Reading the RAM is done when the R/W bit is high and by reading the LCDDR register with the C51 instruction set. It is not recommanded to use read-modify-write instructions.

The selection of RAM from DDRAM, CGRAM or SEGRAM, is set by the set RAM selector instruction.

After read operation, the address is automatically increased/decreased by 1, according to the entry mode.

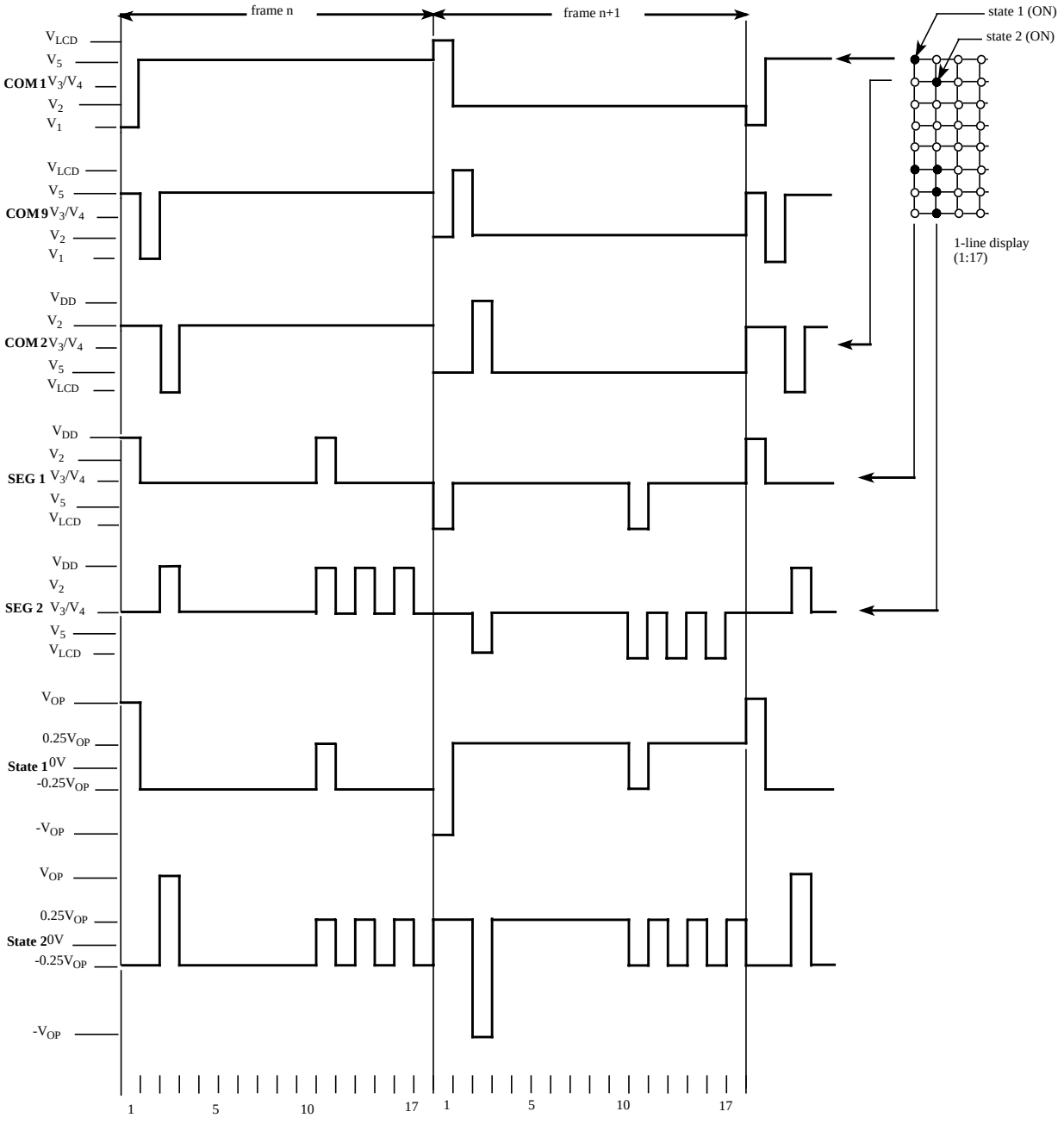


Figure 41. Typical LCD waveforms; 1-line mode.

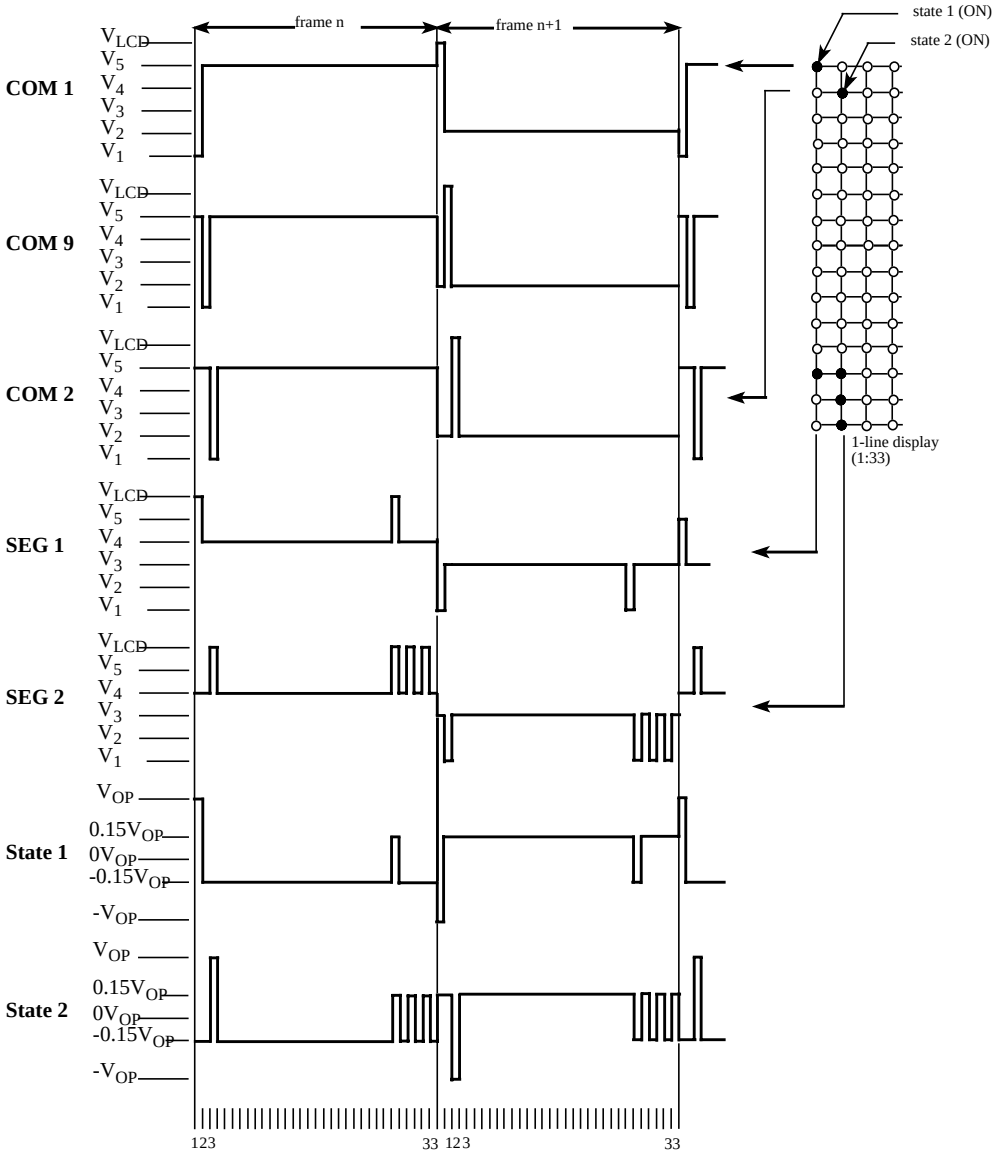


Figure 42. Typical LCD waveforms; 2-line mode.

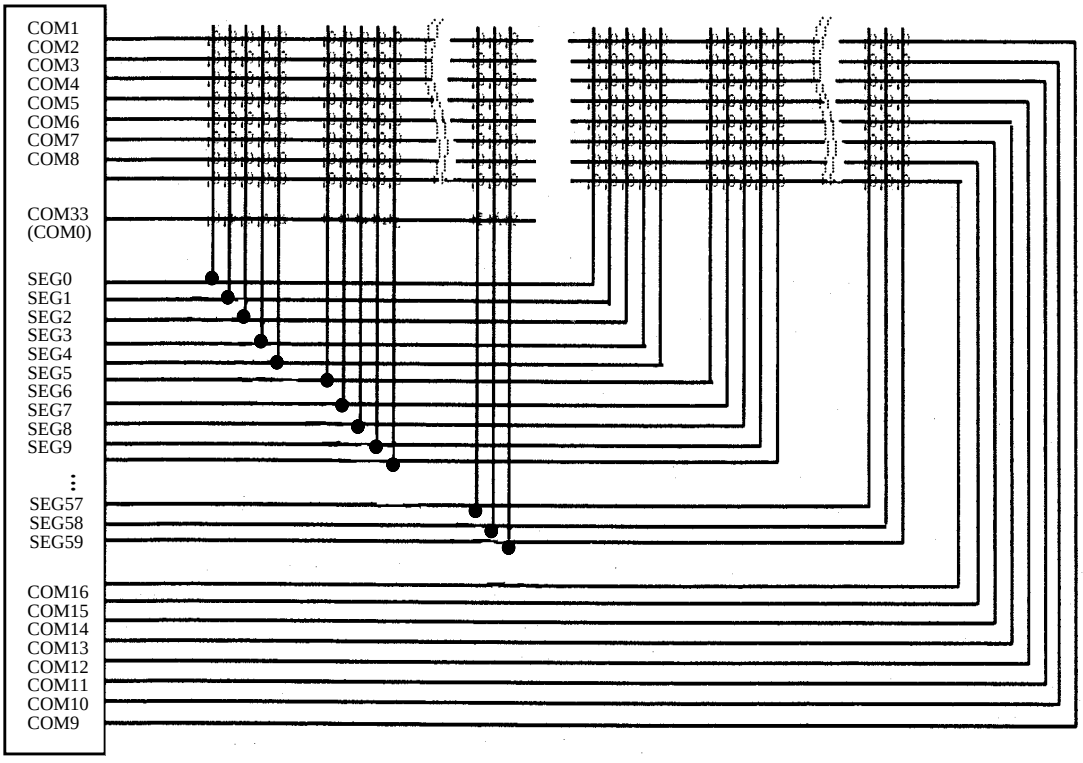


Figure 43. LCD Panel: 24 character x 1 line format (5-dot font, 1/17 duty)

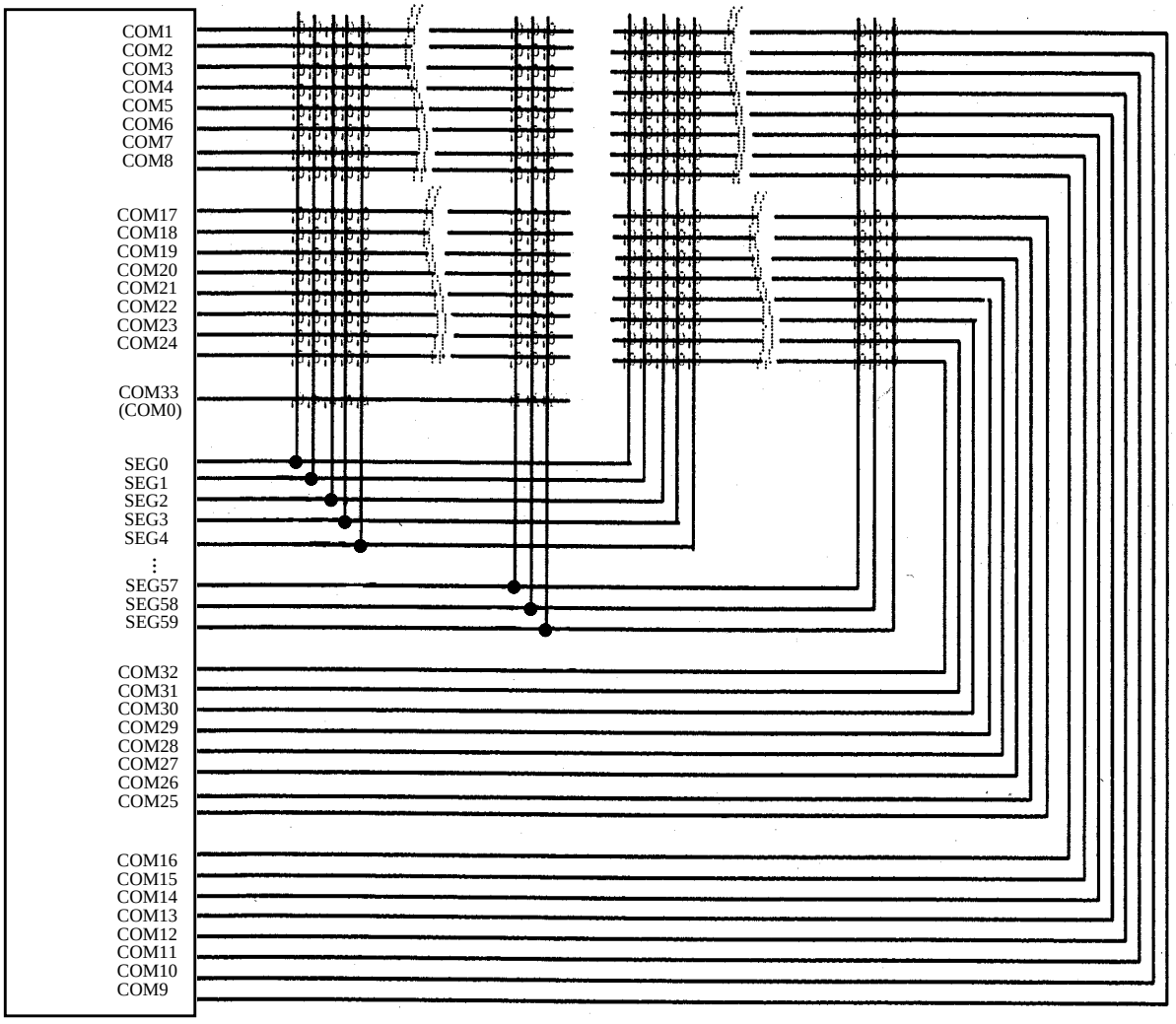


Figure 44. LCD Panel: 24 character x 2 line format (5-dot font, 1/33 duty)

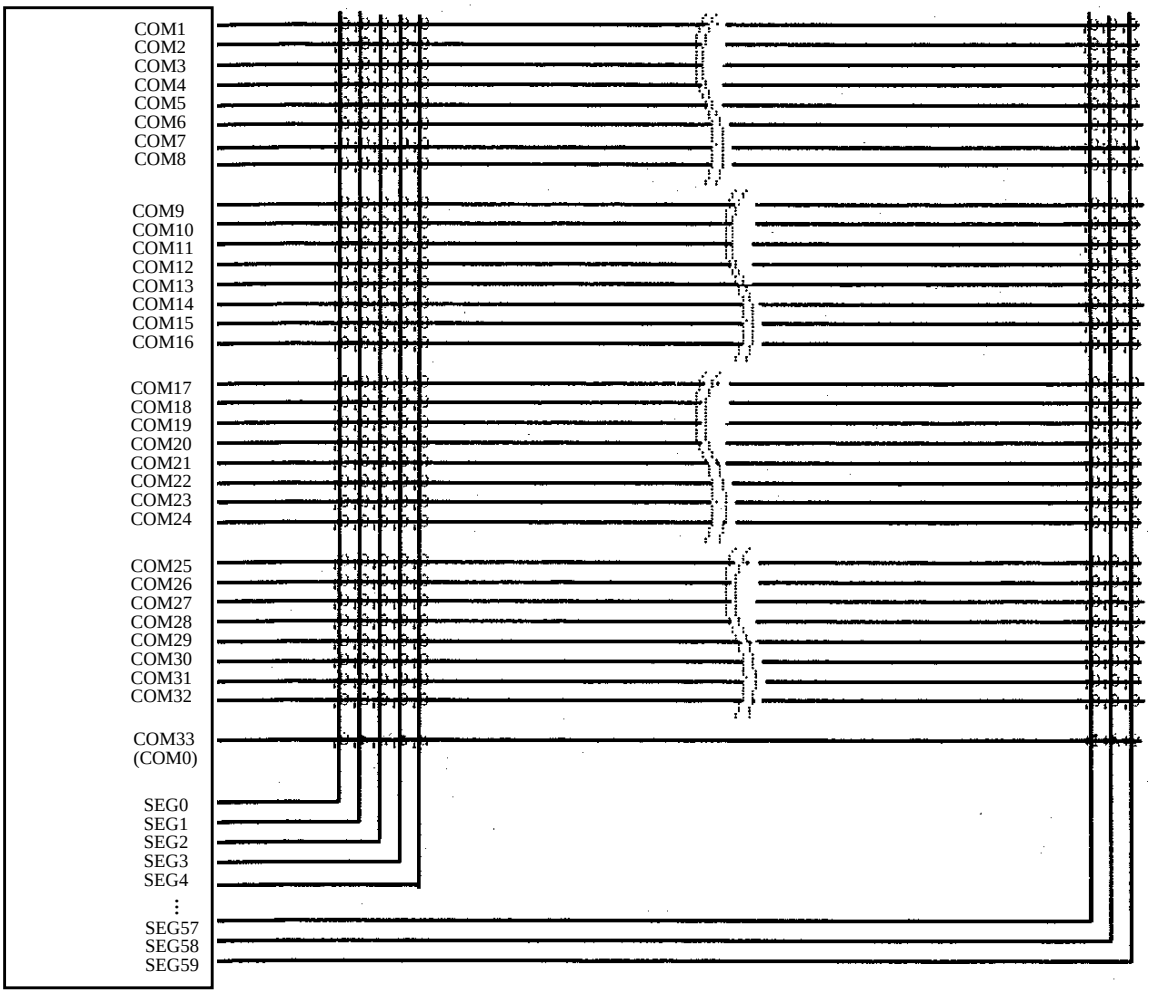


Figure 45. LCD Panel: 12 character x 4 line format (5-dot font, 1/33 duty)

21. EPROM Test Modes

21.1 Overview

The EPROM test modes are used to program data into the Code array memory, to program data into the Encryption array memory, to program Security bits but also to verify EPROM content, to verify Security bits status and to read Signatures bytes (electric identifiers). The EPROM test modes described in this document are compatible with INTEL FX core test modes.

21.2 Description

The EPROM is divided in three different arrays:

- the code array (up to 64k bytes)
- the encryption array (64 bytes)
- the bits array divided in two arrays
- the security bits array (3 bits)
- the general purpose bit array (5 bits)

In addition a fourth non programmable array is implemented:

- the signature bytes array

21.2.1 Operation

The Programming test modes of operation are invoked by driving certain pins of the microcontroller under reset condition (see Table 1). This is the similar way the test modes are enabled on the 8051 family.

Table 79. EPROM Test modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Array	1	0	⎍⎍	12.75V	0	1	1	1	1
Program Encryption Array Address 0-3Fh	1	0	⎍⎍	12.75V	0	1	1	0	1
Program Security Bit 1	1	0	⎍⎍	12.75V	1	1	1	1	1
Program Security Bit 2	1	0	⎍⎍	12.75V	1	1	1	0	0
Program Security Bit 3	1	0	⎍⎍	12.75V	1	0	1	1	0
Program Bit Array	1	0	⎍⎍	12.75V	1	0	1	0	0
Mode 3 Volt *	1	0	⎍⎍	12.75V	1	0	1	0	0
Verify Code Array	1	0	1	1	0	⎍	0	1	1
Read Signature Bytes	1	0	1	1	0	⎍	0	0	0
Verify Bits Array	1	0	1	1	0	⎍	0	0	1

** If 3 Volt power supply is chosen, mode 3V has to be programmed for proper VLCD generation. On port 0 "FEh" has to be entered during mode 3 Volt programming.*

21.3 Specification

21.3.1 Code array programming

To program data in the code array, code array programming test mode must be entered as referred to Table 1. Microcontroller pins must be held to levels indicated in Figure 1 according to the timings showed in Figure 8. Depending on the EPROM size, some address bits are unused (see Table 2).

Erasing the EPROM erases the code array, leaving all cells to FFh.

Table 80. Address bits location

ROM size	A0-A7	A8-A11	A12	A13	A14	A15
4k	P1.0-P1.7	P2.0-P2.3	-	-	-	
8k	P1.0-P1.7	P2.0-P2.3	P2.4	-	-	
16k	P1.0-P1.7	P2.0-P2.3	P2.4	P2.5	-	
32k	P1.0-P1.7	P2.0-P2.3	P2.4	P2.5	P3.4	
64k	P1.0-P1.7	P2.0-P2.3	P2.4	P2.5	P3.4	P3.5

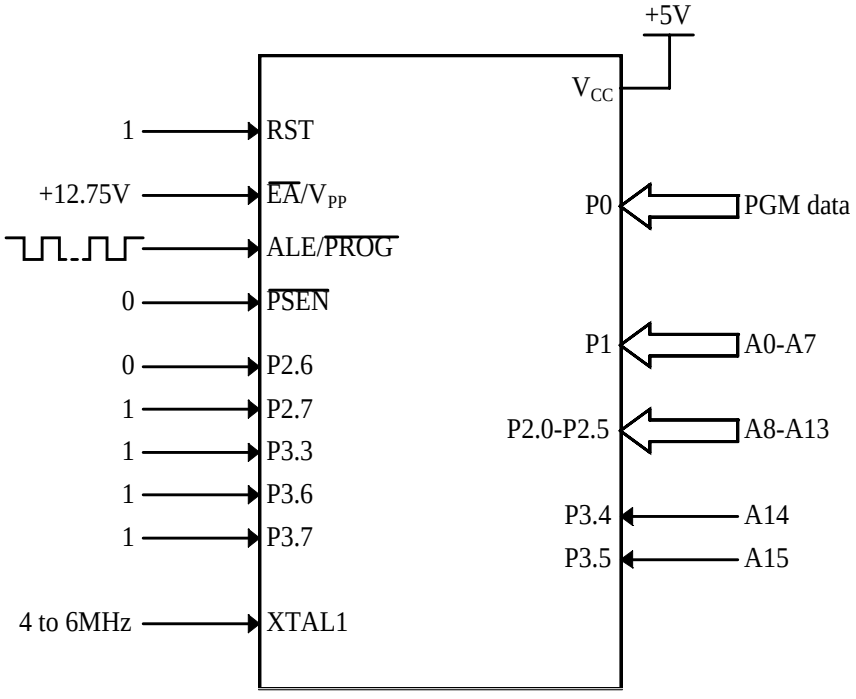


Figure 46. Code array programming configuration

21.3.2 Code array verifying

To verify the code array, code array verifying test mode must be entered as referred in Table 1. Microcontroller pins must be held to levels indicated in Figure 2 according to the timings showed in Figure 9. P2.7 is used as output enable signal. As for programming, depending on the EPROM size, some address bits are unused (see Table 2).

Verifying code array with non blank encryption array will return encrypted data.

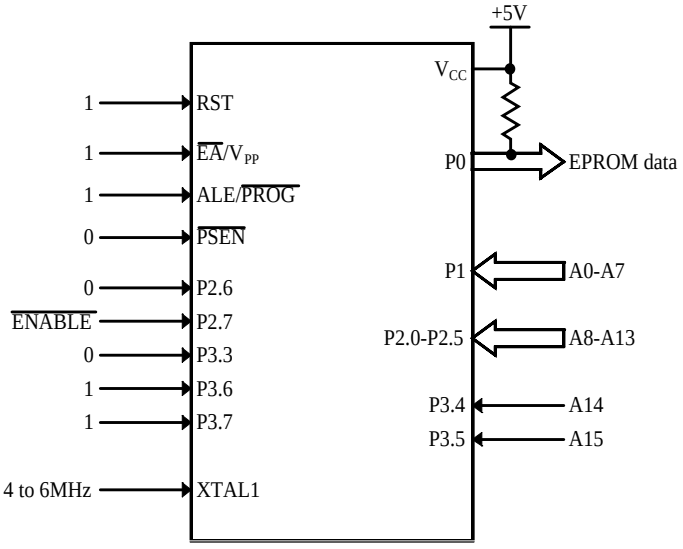


Figure 47. Code array verifying configuration

21.3.3 Encryption array programming

Within the EPROM array are 64 bytes of encryption array. Every time a byte is addressed during a verify, the 6 low order address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encryption verify byte. Thus an encryption byte is used every 64 bytes of code. Code verify, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form.

To program data in the encryption array, encryption array programming test mode must be entered as referred to Table 1. Microcontroller pins must be held to levels indicated in Figure 3 according to the timings showed in Figure 8. As encryption array size is 64 bytes, only 6 address bits are used.

Erasing the EPROM erases the encryption array, leaving all cells to FFh.

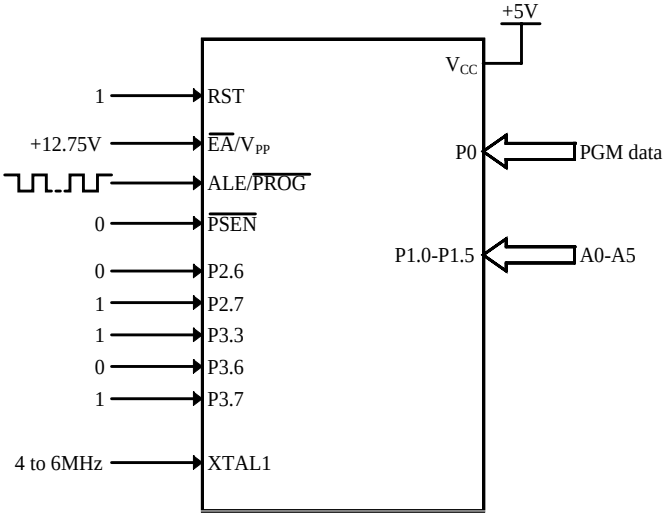


Figure 48. Encryption array programming configuration

21.3.4 Bit array programming

Within the bits array composed of eight bits are three security bits. To keep a compatibility with Intel programming mode, two different ways are available to program security bits these ways are explained in the sections hereafter.

Table 3. Security bits Table 3 shows the position of the security bits in the eight bits array.

21.3.4.1 Eight bits programming

To program the entire bits array, bits array programming test mode must be entered as referred to Table 1. Microcontroller pins must be held to levels indicated in Figure 4 according to the timings showed in Figure 8.

Erasing the EPROM erases the bits array, leaving all bits unprogrammed.

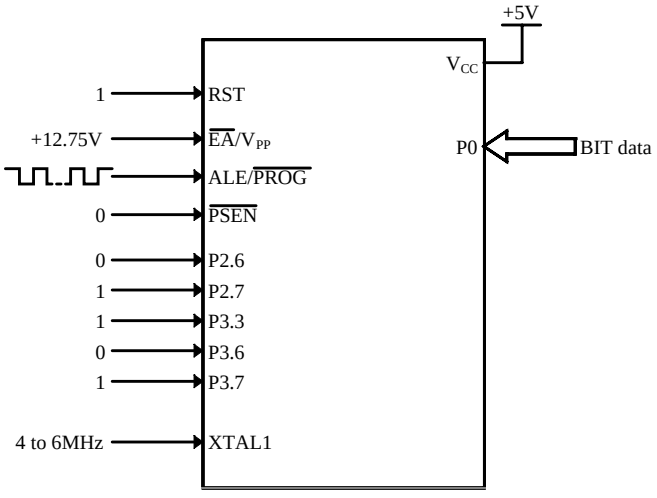


Figure 49. Bits array programming configuration

Table 81. Security bits position

S1	S2	S3	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7-5	S1-S3	Security bits.
4-0	B4-B0	General purpose bits.

21.3.4.2 Security bits programming

To program the three security bits array, security bits array programming test mode (one for each security bits) must be entered as referred to Table 1. Microcontroller pins must be held to levels indicated in Figure 5 according to the timings showed in Figure 8.

These three security bits when programmed will provide different levels of protection for the on-chip code and data. These protections are described in Table 4.

Erasing the EPROM erases the security bits array, leaving all security bits unprogrammed.

Table 82. Program Security bits description

Program Security Bits				
	SB1	**SB2**	**SB3**	**Protection description**
1	U	U	U	No program security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed).
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled. Code verify will be encrypted by the Encryption Array if programmed.
3	X	P	U	Same as 2, also verify is disabled.
4	X	X	P	Same as 3, also external execution is disabled.

U: unprogrammed, P: programmed, X: undefined.

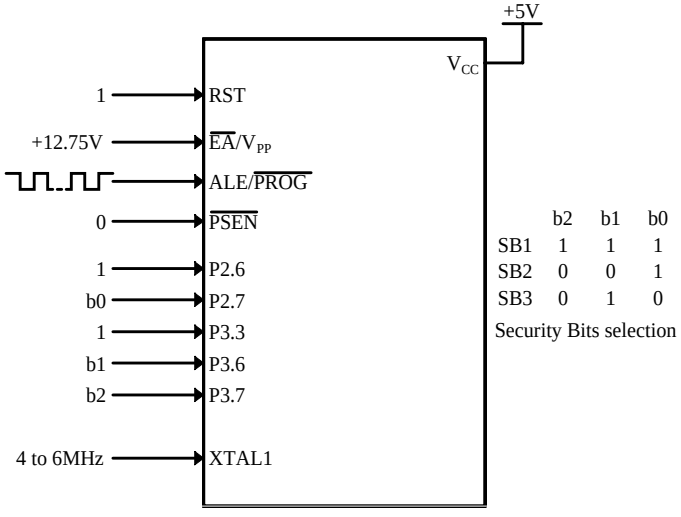


Figure 50. Security bits programming configuration

21.3.5 Bits array verifying

To read the eight bits status, bits array verifying test mode must be entered as referred in Table 1. Microcontroller pins must be held to levels indicated in Figure 6 according to the timings showed in Figure 9. P2.7 is used as output enable signal.

The content of the status byte is explained in Table 5. Reading bits status after EPROM erasing returns 1111 1111b.

Table 83. Bits Array Status Byte

S1	S2	S3	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7	S1	**Security bit 1 status** Cleared when security bit 1 is programmed. Set when security bit 1 is unprogrammed.
6	S2	**Security bit 2 status** Cleared when security bit 2 is programmed. Set when security bit 2 is unprogrammed.
5	S3	**Security bit 3 status** Cleared when security bit 3 is programmed. Set when security bit 3 is unprogrammed.
4-0	B4-B0	**General purpose bits status** Cleared when bit is programmed. Set when bit is unprogrammed.

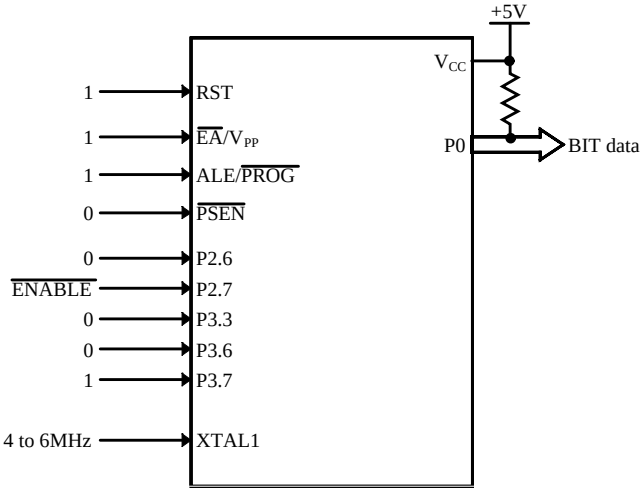


Figure 51. Bits array verifying configuration

21.3.6 Signature byte reading

To read the signature byte array, signature byte reading test mode must be entered as referred in Table 1. Microcontroller pins must be held to levels indicated in Figure 7 according to the timings showed in Figure 9. P2.7 is used as output enable signal.

The content of the signature bytes depends on the product, and are detailed in Table 6. Beta2 values are in bold type.

Table 84. Signature Bytes Content

Location	Device		Contents	Comment
30h	All		58h	Customer selection byte: TEMIC
31h	All		57h	Family selection byte: C51 X2
			58h	Family selection byte: C51
60h	4k EPROM	128 RAM	1001 1110b	e.g. 87C51= 9Eh
		256 RAM	1010 1110b	
		512 RAM	1011 1110b	
	8k EPROM	128 RAM	1001 1101b	
		256 RAM	1010 1101b	e.g. 87C52= ADh
		512 RAM	1011 1101b	
	16k EPROM	128 RAM	1001 1011b	
		256 RAM	1010 1011b	e.g. 87C154= ABh
		512 RAM	1011 1011b	
	24k EPROM	128 RAM	1001 1001b	
		256 RAM	1010 1001b	
		512 RAM	1011 1001b	e.g. 87C51A11= B9h
	32k EPROM	128 RAM	1001 0111b	
		256 RAM	1010 0111b	e.g. 87C154D= A7h
		512 RAM	1011 0111b	
	48k EPROM	128 RAM	1001 0011b	
		256 RAM	1010 0011b	
		512 RAM	1011 0011b	
	64k EPROM	128 RAM	1001 1100b	
		256 RAM	1010 1100b	
		512 RAM	1011 1100b	
61h		All	XXh start FFh	Product revision number

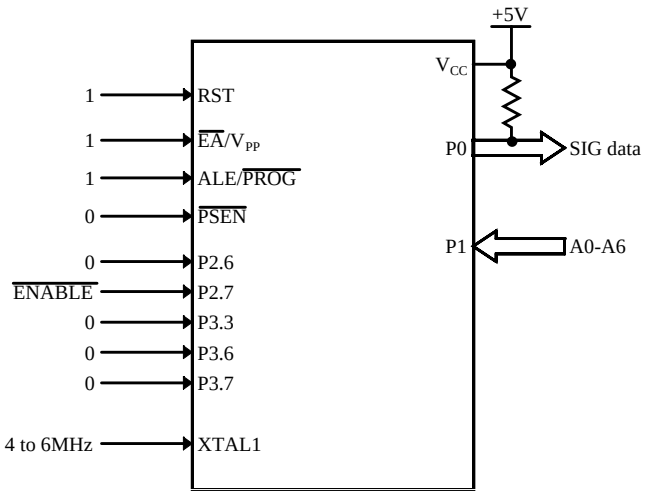


Figure 52. Signature bytes reading configuration

21.3.7 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12000 W/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves all the EPROM cells in a 1's state.

21.4 Characteristics

Table 85. EPROM Characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Temperature	+21	+27	°C
V_{cc}	Supply Voltage	4.5	5.5	V
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator frequency	4	6	MHz
TAVGL	Address set-up to PROG low	48 TCLCL		
TGHAX	Address hold after PROG	48 TCLCL		
TDVGL	Data set-up to PROG low	48 TCLCL		
TGHDX	Data hold after PROG	48 TCLCL		
TEHSH	(Enable) high to V_{PP}	48 TCLCL		
TSHGL	V_{PP} set-up to PROG low	10		s
TGHSL	V_{PP} hold after PROG	10		s
TGLGH	PROG width	90	110	s
TSHGL	PROG high to PROG low	10		s
TAVQV	Address to data valid		48 TCLCL	
TELQV	ENABLE low to data valid		48 TCLCL	
TEHQZ	Data float after ENABLE		48 TCLCL	

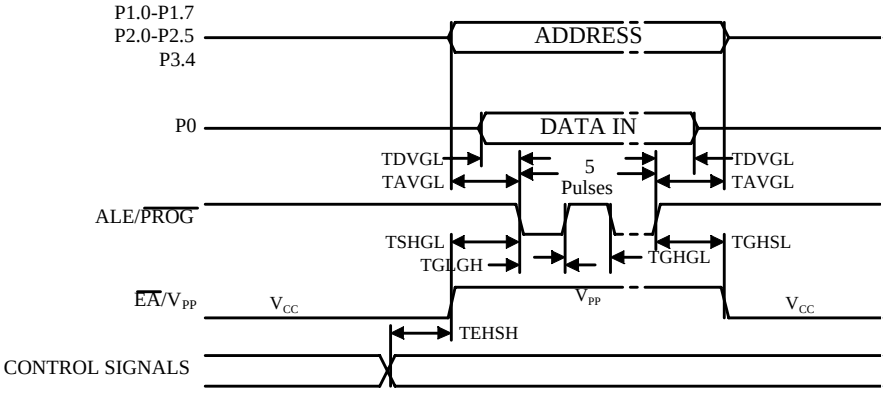


Figure 53. Programming timing

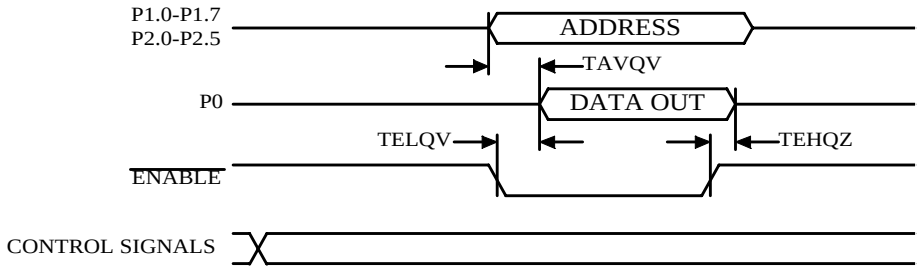


Figure 54. Reading timing

22. Application

22.1 Encrypted parts

When using the encryption, one important factor needs to be considered. If a code byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (> 64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some values other than FFh, and not all of them the same value. This will ensure maximum program protection.

23. Special Function Registers

The Special Function Registers (SFRs) of the PAROS belongs to the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3,
- Specific Ports P4, KB0, KB1
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON, BRL, BDRCON
- Power and clock control registers: CKSEL, OSCCON, PCON, CKRL
- Interrupt system registers: IE, IE1, IP0, IPL0, IPL1, IPH0, IPH1, P4F, P4IE
- WatchDog Timer: WDTRST, WDTPRG
- LCD Controller: LCDCON, LCDAC, LCDIR, LCDDR, LCDPS
- I2C: SSCON, SSCS, SSDAT, SSADR
- SPI: SPCR, SPSCR, SPDR
- PCA: CCAPnL, CCAPnH, CCAPMn, CL, CH, CMOD, CCON
- Others: AUXR, AUXR1, COMCON

Table 86. ACC Register

ACC - Accumulator (E0h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Bit addressable

Table 87. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**AO**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b
Not bit addressable

Table 88. AUXR1 Register

AUXR1 - Dual Pointer Selection Register (A2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**DPS**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer 1** Clear to select DPTR as Data Pointer. Set to select DPTR1 as Data Pointer.

Reset Value = XXXX X0X0b
Not bit addressable

Table 89. B Register

B - Register (F0h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Bit addressable

Table 90. BDRCON Register

BDRCON - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK	RBCK	SPD	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	BRR	**Baud Rate Run Control bit** Clear to stop the Baud Rate. Set to start the Baud Rate.
3	TBCK	**Transmission Baud rate Generator Selection bit for first UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for first UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for both first UART** Clear to select the SLOW Baud Rate Generator when SRC=1. Set to select the FAST Baud Rate Generator when SRC=1.
0	SRC	**Baud Rate Source select bit in Mode 0 for first UART** Clear to select $F_{OSC}/12$ as the Baud Rate Generator. Set to select the internal Baud Rate Generator.

Reset Value = XXXX 0000b
Not bit addressable

Table 91. BRL Register

BRL - Baud Rate Reload Register for UART (9Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 92.

PCA High Byte Compare/Capture Module n Registers (n = 0, 1)
CCAP0H (FAh)
CCAP1H (FBh)

High Byte Compare/Capture Module n

7	6	5	4	3	2	1	0
High Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CCAPnH 7:0	High byte of EWC-PCA comparison or capture values

Reset Value = 0000 0000b

Table 93.

PCA Low Byte Compare/Capture Module n Registers (n = 0, 1)
CCAP0L (EAh)
CCAP1L (EBh)

Low Byte Compare/Capture Module n

7	6	5	4	3	2	1	0
Low Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CCAPnL 7:0	Low byte of EWC-PCA comparison or capture values

Reset Value = 0000 0000b

Table 94.

PCA Compare/Capture Module n Mode registers (n = 0, 1)
CCAPM0 (DAh)
CCAPM1 (DBh)

7	6	5	4	3	2	1	0
-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The Value read from this bit is indeterminate. Do not set this bit.
6	ECOMn	**Enable Compare Mode Module x bit** Clear to disable the Compare function. Set to enable the Compare function.. The Compare function is used to implement the software Timer, the high-speed output, the Pulse Width Modulator (PWM) and Watchdog Timer (WDT).
5	CAPPn	**Capture Mode (Positive) Module x bit** Clear to disable the Capture function triggered by a positive edge on CEXx pin. Set to enable the Capture function triggered by a positive edge on CEXx pin
4	CAPNn	**Capture Mode (Negative) Module x bit** Clear to disable the Capture function triggered by a negative edge on CEXx pin. Set to enable the Capture function triggered by a negative edge on CEXx pin.
3	MATn	**Match Module x bit** Set when a match of the PCA Counter with the Compare/Capture register sets CCFx bit in CCON register, flagging an interrupt. Must be cleared by software.
2	TOGn	**Toggle Module x bit** The toggle mode is configured by setting ECOMx, MATx and TOGx bits. Set when a match of the PCA Counter with the Compare/Capture register toggles the CEXx pin. Must be cleared by software.
1	PWMn	**Pulse Width Modulation Module x Mode bit** Set to configure the module x as an 8-bit Pulse Width Modulator with output waveform on CEXx pin . Must be cleared by software.
0	ECCFn	**Enable CCFx Interrupt bit** Clear to disable CCFx bit in CCON register to generate an interrupt request. Set to enable CCFx bit in CCON register to generate an interrupt request.

Reset Value = X000 0000b

Table 95.

Timer/Counter Control Register CCON (D8h)

7	6	5	4	3	2	1	0
CF	**CR**	**-**	**-**	**-**	**-**	**CCF1**	**CCF0**

Bit Number	Bit Mnemonic	Description
7	CF	**PCA Timer/Counter Overflow flag** Set by hardware when the PCA Timer/Counter rolls over. This generates a PCA interrupt request if the ECF bit in CMOD register is set. Must be cleared by software.
6	CR	**PCA Timer/Counter Run Control bit** Clear to turn the PCA Timer/Counter off. Set to turn the PCA Timer/Counter on.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	CCF1	**PCA Module 1 Compare/Capture flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 1 bit in CCAPM 1 register is set. Must be cleared by software.
0	CCF0	**PCA Module 0 Compare/Capture flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 0 bit in CCAPM 0 register is set. Must be cleared by software.

Reset Value = 00XX XX00b

Table 96.

Timer/Counter Registers High value CH (F9h)

7	6	5	4	3	2	1	0
High Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CH 7:0	High byte of Timer/Counter

Reset Value = 0000 00000b

Table 97.

Timer/Counter Registers Low value CL (E9h)

Low Byte of Timer/Counter Register

7	6	5	4	3	2	1	0
Low Byte of Compare/Capture Values							

Bit Number	Bit Mnemonic	Description
7:0	CL 7:0	Low byte of Timer/Counter

Reset Value = 0000 00000b

Table 98. CMOD Register

Timer/Counter Mode Register CMOD (D9h)

7	6	5	4	3	2	1	0
CIDL	**-**	**-**	**-**	**-**	**CPS1**	**CPS0**	**ECF**

Bit Number	Bit Mnemonic	Description
7	CIDL	**PCA Counter Idle Control bit** Clear to let the PCA running during Idle mode. Set to stop the PCA when Idle mode is invoked.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	CPS1	**EWC Count Pulse Select bits** CPS1 CPS0 Clock source 0 0 Internal Clock, Fosc/12 0 1 Internal Clock, Fosc/4 1 0 Timer 0 overflow 1 1 External clock at ECI/P1.2 pin (Max. Rate = Fosc/8)
1	CPS0	
0	ECF	**Enable PCA Counter Overflow Interrupt bit** Clear to disable CF bit in CCON register to generate an interrupt. Set to enable CF bit in CCON register to generate an interrupt.

Reset Value = 0XXX X000b

Table 99. COMCON Register

COMCON - (A3h)

7	6	5	4	3	2	1	0
AF1	**AS1**	**V1R1**	**V1R0**	**AF0**	**AS0**	**V0R1**	**V0R0**

Bit Number	Bit Mnemonic	Description
7/3	AF1/AF0	= 1, indicates the input level (P4.5/P4.4) has matched the reference level. = 0, the input is less than the reference level.
6/2	AS1/AS0	= 1, start the voltage comparison process = 0, stop the voltage comparaison process
5/1	V1R1/V0R1	Disconnect the voltage reference or select one of three reference value **V1R1/V0R1 Voltage reference** 1 63% x VDD 1 50% x VDD 0 20% x VDD 0 Disconnected
4/0	V1R0/V0R0	Disconnect the voltage reference or select one of three reference value **V1R0/V0R0 Voltage reference** 1 63% x VDD 0 50% x VDD 1 20% x VDD 0 Disconnected

Reset Value = 0100 0100b

AF1, AF0 = 1 , indicates the input level has matched the reference level.

Table 100. DPH Register

DPH - Data Pointer High Register (83h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b
Not bit addressable

Table 101. DPL Register

DPL - Data Pointer Low Register (82h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b
Not bit addressable

Table 102. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**EC**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	EC	**PCA Interrupt Enable** Clear to disable the the PCA interrupt. Set to enable the the PCA interrupt.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b
Not Bit addressable

Table 103. IE1 Register

IE1 Interrupt Enable Register (C0h)

7	6	5	4	3	2	1	0
-	-	-	-	IAD	SPI	I2C	KBIE

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	IAD	**Comparator interrupt Enable bit** Clear to disable the comparator interrupt Set to enable the comparator interrupt
2	SPI	**SPI Interrupt Enable bit** Clear to disable the SPI interrupt. Set to enable the SPI interrupt.
1	I2C	**I2C Interrupt Enable bit** Clear to disable the I2C interrupt. Set to enable the I2C interrupt.
0	KBIE	**Keyboard Interrupt Enable bit** Clear to disable the Keyboard interrupt. Set to enable the Keyboard interrupt.

Reset Value = XXXX X000b
No Bit addressable

Table 104. IPL0 Register

IPL0 - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPC	**EWC Counter Interrupt Priority bit** Refer to PPCH for priority level
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X000 0000b
Bit addressable

Table 105. IPL1 Register

IPL1 - Interrupt Priority Low Register 1 (B2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**PKB**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	PKB	**Keyboard Interrupt Priority level less significant bit.** Refer to PKBH for priority level.

Reset Value = XXXX XXX0b
Not Bit addressable

Table 106. IPH0 Register

IPH0 - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**EWC-PCA Counter Interrupt Priority level most significant bit** PPCH PPC Priority level 0 0 Lowest 0 1 1 0 1 1 Highest priority
5	PT2H	Timer 2 overflow interrupt Priority High bit PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	Serial port Priority High bit PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	External interrupt 1 Priority High bit PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	Timer 0 overflow interrupt Priority High bit PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	External interrupt 0 Priority High bit PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XX00 0000b
Not bit addressable

Table 107. IPH1 Register

IPH1 - Interrupt Priority High Register 1 (B3h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**PKBH**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	PKBH	**Keyboard Interrupt Priority level most significant bit** PKBH PKB Priority level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XXXX XXX0b
Not bit addressable

Table 108. LCDPS Register

LCDPS - Prescaler register for LCD (E4h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

Table 109. LCDCON Register

LCDCON - LCD Control register (E3h)

7	6	5	4	3	2	1	0
BUSYF	**VCP2**	**KEYBONB**	**LCDRST**	**M**	**N**	**VCP1**	**VCP0**

Bit Number	Bit Mnemonic	Description
7	BUSYF	**Busy Flag** Set to one by the LCD controller to signal that the LCD controller is busy. Clear by the LCD controlled to signal that the LCD controller is ready to accept another instruction
6	VCP2	**Voltage Converter Programming bit 2**
5	KEYBONB	**Keyboard on/off** When set to one, the keyboard trame on S0 to S15 is off When cleared, the keyboard trame on S0 to S15 is on
4	LCDRST	**Display controller reset** When clear, the display logic controller is reseted. No operation can be done. When set, the display logic controller is running. It is mandatory that this bit is cleared when the display controller clock is switched (OSCB or OSCC).
3	M	**Display configuration** M N Comments 0 0 1 line x 24, MUX 1:17 0 1 reserved 1 0 2 lines x 24, MUX 1:33 1 1 4 lines x 12 MUX 1:33
2	N	
1	VCP1	**Voltage Converter Programming bit1 and bit0** VCP2 VCP1 VCP0 Comments 0 0 0 Voltage converter off 0 0 1 Voltage V_{CC} (5V or 3V) 0 1 0 Voltage 5V (only if V_{CC} = 3V) 0 1 1 Reserved 1 0 0 Voltage 6V 1 0 1 Voltage 7V 1 1 0 Voltage 8V 1 1 1 Voltage 9V
0	VCP0	

Reset Value = 0X00 0000b

Table 110. LCDIR Register

LCDIR - Instruction register for LCD (E6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

Table 111. LCDDR Register

LCDDR - Data register for LCD (E7h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

Table 112. LCDAC Register

LCDAC - Address Counter register for LCD (E5h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = 0000 0000b

Table 113. P0 Register

P0 - Port 0 Register (80h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 114. P1 Register

P1 - Port 1 Register (90h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 115. P2 Register

P2 - Port 2 Register (A0h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 116. P3 Register

P3 - Port 3 Register (B0h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 117. P4 Register

P4 - Port 4 Register (B1h)

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 118. KB0 Register

KB0 - Keyboard Output Register 0 (E8h) or Specific P5

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 119. KB1 Register

KB1 - Keyboard Output Register 1 (F8h) or Specific P6

7	6	5	4	3	2	1	0

Reset Value = 1111 1111b
Bit addressable

Table 120. IE Register

P4IE - Port 4 Interrupt Enable Register (S:9Dh)

7	6	5	4	3	2	1	0
-	-	-	-	P4IE.3	P4IE.2	P4IE.1	P4IE.0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	P4IE.3	**Port 4 line 3 Interrupt Enable bit** Clear to disable P4F.3 bit in P4F register to generate an interrupt request. Set to enable P4F.3 bit in P4F register to generate an interrupt request.
2	P4IE.2	**Port 4 line 2 Interrupt Enable bit** Clear to disable P4F.2 bit in P4F register to generate an interrupt request. Set to enable P4F.2 bit in P4F register to generate an interrupt request.
1	P4IE.1	**Port 4 line 1 Interrupt Enable bit** Clear to disable P4F.1 bit in P4F register to generate an interrupt request. Set to enable P4F.1 bit in P4F register to generate an interrupt request.
0	P4IE.0	**Port 4 line 0 Interrupt Enable bit** Clear to disable P4F.0 bit in P4F register to generate an interrupt request. Set to enable P4F.0 bit in P4F register to generate an interrupt request.

Reset Value = 0000 0000b
Not Bit addressable

Table 121. P4F Register

P4F - Port 4 Flag Register (9Eh)

7	6	5	4	3	2	1	0
-	-	-	-	P4F.3	P4F.2	P4F.1	P4F.0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	P4F.3	**Port 4 line 3 flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.3 bit in P4IE register is set. Must be cleared by software.
2	P4F.2	**Port 4 line 2 flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.2 bit in P4IE register is set. Must be cleared by software.
1	P4F.1	**Port 4 line 1 flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.1 bit in P4IE register is set. Must be cleared by software.
0	P4F.0	**Port 4 line 0 flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the P4IE.0 bit in P4IE register is set. Must be cleared by software.

Reset Value = 0000 0000b
Not bit addressable

Table 122. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Table 123. CKSEL Register

CKSEl - Clock Select Register (85h)

7	6	5	4	3	2	1	0
-	-	-	-	-	RSTD	CKS1	CKS0

Bit Number	Bit Mnemonic	Description
7		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	RSTD	Reset Detector Disable Bit
1	CKS1	Cpu Ocillator Select Bit When cleared, Cpu and peripherals connected to OSCA When set, Cpu and peripherals connected to OSCB Cleared by hardware after a Power-up (OSCA selected by default)
0	CKS0	Lcd Ocillator Select Bit When cleared, Lcd connected to OSCC When set, Lcd connected to OSCB Set by hardware after a Power-up (OSCC selected by default)

Reset Value = XXXXX000b
Not bit addressable

Table 124. OSCCON Register

OSCCON - Oscillator Control Register (86h)

7	6	5	4	3	2	1	0
-	-	-	-	-	OscCEn	OscBEn	OscAEn

Bit Number	Bit Mnemonic	Description
7		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3		**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	OscCEn	OscC enable bit Set by software to run OscC Cleared by software to stop OscC Cleared by hardware after a Power-up
1	OscBEn	OscB enable bit Set by software to run OscB Cleared by software to stop OscB Cleared by hardware after a Power-up
0	OscAEn	OscA enable bit Set by software to run OscA Cleared by software to stop OscA Set by hardware after a Power-up

Reset Value = XXXXX001b
Not bit addressable

Table 125. CKRL Register

CKRL - Oscillator Prescalar Register (97h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7:0	CKRL	Clock Reload Register : Prescaler value

Reset Value = 1111 1111b

Table 126. SSCON Register

SSCON - Synchronous Serial Control register (93h)

7	6	5	4	3	2	1	0
CR2	SSIE	STA	STO	SI	AA	CR1	CR0

Bit Number	Bit Mnemonic	Description
7	CR2	**Control Rate bit 2** See Table 1.
6	SSIE	**Synchronous Serial Interface Enable bit** Clear to disable SSLC. Set to enable SSLC.
5	STA	**Start flag** Set to send a START condition on the bus.
4	ST0	**Stop flag** Set to send a STOP condition on the bus.
3	SI	**Synchronous Serial Interrupt flag** Set by hardware when a serial interrupt is requested. Must be cleared by software to acknowledge interrupt.
2	AA	**Assert Acknowledge flag** Clear in master and slave receiver modes, to force a not acknowledge (high level on SDA). Clear to disable SLA or GCA recognition. Set to recognise SLA or GCA (if GC set) for entering slave receiver or transmitter modes. Set in master and slave receiver modes, to force an acknowledge (low level on SDA). This bit has no effect when in master transmitter mode.
1	CR1	**Control Rate bit 1** See Table 1
0	CR0	**Control Rate bit 0** See Table 1

Reset Value = 0000 0000b
Not bit addressable

Table 127. SSCS Register

SSCS - Synchronous Serial Control and Status register (94h) WRITE mode

7	6	5	4	3	2	1	0
CSS	-	-	-	-	-	IS1	IS0

Bit Number	Bit Mnemonic	Description
7	CSS	**Clock Source Selection bit** (see Table 1) Clear to select internal bit rate controlled by CR0 to CR2. Set to select external bit rate generator.
6	-	Reserved
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	-	Reserved
1	IS1	**Interface Selection bit 1** Clear to select I^2C interface.
0	IS0	**Interface Selection bit 0** Clear to select I^2C interface.

Reset Value = 0XXX XX00b
Not bit addressable

SSCS - Synchronous Serial Control and Status register (94h) READ mode

7	6	5	4	3	2	1	0
CSS	-	-	-	-	-	IS1	IS0

Bit Number	Bit Mnemonic	Description
0	0	Always zero
1	0	Always zero
2	0	Always zero
3	SC0	**Status Code bit 0** See Table 6 to Table 10
4	SC1	Status Code bit 1 See Table 6 to Table 10
5	SC2	**Status Code bit 2** See Table 6 to Table 10
6	SC3	**Status Code bit 3** See Table 6 to Table 10
7	SC4	**Status Code bit 4** See Table 6 to Table 10

Reset Value = F8b
Not bit addressable

Table 128. SSDAT Register

SSDAT - Synchronous Serial Data register (read/write) (95h)

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Bit Number	Bit Mnemonic	Description
7	SD7	Address bit 7 or Data bit 7.
6	SD6	Address bit 6 or Data bit 6.
5	SD5	Address bit 5 or Data bit 5.
4	SD4	Address bit 4 or Data bit 4.
3	SD3	Address bit 3 or Data bit 3.
2	SD2	Address bit 2 or Data bit 2.
1	SD1	Address bit 1 or Data bit 1.
0	SD0	Address bit 0 (R/W) or Data bit 0.

Reset Value = 1111 1111b
Not bit addressable

Table 129. SSADR Register

SSADR - Synchronous Serial Address register (read/write) (96h)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Bit Number	Bit Mnemonic	Description
7	A7	Slave address bit 7.
6	A6	Slave address bit 6.
5	A5	Slave address bit 5.
4	A4	Slave address bit 4.
3	A3	Slave address bit 3.
2	A2	Slave address bit 2.
1	A1	Slave address bit 1.
0	GC	**General call bit** Clear to disable the general call address recognition. Set to enable the general call address recognition.

Reset Value = 1111 1110b
Not bit addressable

Table 130. SPCR Register

SPCR - Control and data register (C3h)

7	6	5	4	3	2	1	0
SPRIE	-	SPMSTR	CPOL	CPHA	SPWOM	SPE	SPTIE

Bit Number	Bit Mnemonic	Description
7	SPRIE	Spi Receiver Interrupt Enable ; This R/W bit enables CPU interrupt requests or DMA service requests generated by the SPRF bit Cleared by Reset signal
6	-	RESERVED Cleared by Reset signal Do not set this bit
5	SPMSTR	Spi Master : This R/W bit selects master or slave mode operations 1 = master mode 0 = slave mode Set by Reset signal
4	CPOL	Clock Polarity: This R/W signal determines the logic state of the SPSCK pin between transmissions To transmit datas between Spi modules, these modules must have the same polarity . Cleared by Reset signal
3	CPHA	Clock Phase : This R/W bit controls the timing relationship between the serial clock and SPI data . To transmit datas between Spi modules, these modules must have the same phase Set by Reset signal
2	SPWOM	Spi Wire-Or Mode : This R/W bit disables the pull-up devices on pins SPSCK, MOSI and MISO, so that those pins become open-drain outputs 1 = Wired-or SPCK, MOSI and MISO 0 = Normal push pull SPCK, MOSI and MISO Cleared by Reset signal
1	SPE	Spi Enable : This R/W bit enables the SPI module Cleared by Reset signal
0	SPTIE	Spi Transmit Interrupt Enable : This R/W bit enables CPU interrupt request generated by the SPTE bit Cleared by Reset signal

Reset Value = 0010 1000b
Not bit addressable

Table 131. SPSCR Register

SPSCR - SPI Status and Control Register (C4h)

7	6	5	4	3	2	1	0
SPRIE	-	SPMSTR	CPOL	CPHA	SPWOM	SPE	SPTIE

Bit Number		Mnemonic	Description
Read	7	SPRF	Spi Receiver Full : This Read only flag is set each time a byte transfers from the shift register to rhe receive register . Cleared by hardware : ■ during an SPRF CPU interrupt : if the CPU reads the status and control register with SPRF =1 , and then reads the data register. ■ by Reset signal
Write			
Read	6	ERRIE	Error Interrupt Enable : This R/W (?) bit enables the MODF and OVRF flags to generate CPU interrupt requests Cleared by Reset signal .
Write			
Read	5	OVRF	Overflow Flag : This read-only flag is set if the software does not read the byte in the receive data register before the next byte enters the shift register. Cleared by hardware : ■ if the CPU reads the status and control register with OVRF =1 , and then reads the data register. ■ by Reset signal
Write			
Read	4	MODF	Mode Fault : This read-only flag is set ■ in a slave SPI if the $\overline{SS}$ pin goes high during a transmission ■ in a master SPI if the $\overline{SS}$ pin goes high at any time Cleared by hardware : ■ if the CPU reads the status and control register with MODF =1 , and then writes the data register. ■ by Reset signal
Write			
Read	3	SPTE	Spi Transmitter Empty : This read-only flag is set each time the transmit data register transfers a byte into the shift register . SPTE generates an SPTE CPU interrupt request if the bit SPTIE is also set. Set by Reset signal .
Write			
Read	2	MODFEN	Mode Fault Enable : This R/W bit , when set, allows the MODF flag to be set . In addition, this bit determines the availability of the $\overline{SS}$ pin : ■ if MODFEN = 0 and the SPI in master mode, then the $\overline{SS}$ pin is available as a general purpose I/O. ■ if MODFEN = 1, then the $\overline{SS}$ pin is not available as a general purpose I/O.
Write			
Read	1	SPR1	Spi Baud Rate Select : SPR1:SPR0 : Baud rate divisor (BD) Baud Rate = Internal clock / (2xBD) **(see note)** 00 BD = 2 => Baud Rate = Internal clock / 4 11 BD = 8 => Baud Rate = Internal clock / 16 10 BD = 32 => Baud Rate = Internal clock / 64 11 BD = 128 => Baud Rate = Internal clock / 256
Write			
Read	0	SPR0	
Write			

Reset Value = 0000 1000b
Not bit addressable

Table 132. SPDR Register

SPDR - SPI Data Register (C5h)

Read	R7:0	Receive Data Register
Write	T7:0	Transmit Data register

Table 133. PSW Register

PSW - Program Status Word Register (D0h)

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P

Bit Number	Bit Mnemonic	Description
7	CY	**Carry flag** Receive carry out from bit 1 of ALU operands.
6	AC	Auxiliary Carry flag Receive carry out from bit 1 of addition operands.
5	F0	Flag 0 Cleared by user for general purpose usage. Set by user for general purpose usage.
4	RS1	Register bank Selector bit 1 RS1 RS0 Register Bank 0 0 0 (00h - 07h) 0 1 1 (08h - 0Fh) 1 0 2 (10h - 17h) 1 1 3 (18h - 1Fh)
3	RS0	Register bank Selector bit 0 Refer to RS1 for register bank selection.
2	OV	Overflow flag Cleared when arithmetic operations do not overflow. Set when arithmetic operations overflow.
1	F1	Flag 1 Cleared by user for general purpose usage. Set by user for general purpose usage.
0	P	Parity flag Cleared if the accumulator contains an even number of 1s. Set if the accumulator contains an odd number of 1s.

Reset Value = 0000 0000b
Bit addressable

Table 134. RCAP2H Register

RCAP2H - Timer 2 Reload/Capture High Register (CBh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 135. RCAP2L Register

RCAP2L - Timer 2 Reload/Capture Low Register (CAh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 136. SADEN Register

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 137. SADDR Register

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 138. SBUF Register

SBUF - Serial Data Buffer (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb
Not bit addressable

Table 139. SCON Register

SCON (S:98h)
Serial Control Register

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit**. To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.
	SM0	**Serial Port Mode bit 0**. To select this function, clear SMOD0 bit in PCON register. Software writes to bits SM0 and SM1 to select the Serial Port operating mode. Refer to SM1 bit for the mode selections.
6	SM1	**Serial Port Mode bit 1.** To select this function, set SMOD0 bit in PCON register. Software writes to bits SM1 and SM0 to select the Serial Port operating mode. SM0 SM1 Mode DescriptionBaud Rate 0 0 0Shift RegisterF_{OSC}/12 or variable if SRC bit in BDRCON is set 0 1 18-bit UARTVariable 1 0 29-bit UARTF_{OSC}/32 or F_{OSC}/64 1 1 39-bit UARTVariable
5	SM2	**Serial Port Mode bit 2** Software writes to bit SM2 to enable and disable the multiprocessor communication and automatic address recognition features. This allows the Serial Port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN	**Receiver Enable bit** Clear to disable reception in mode 1, 2 and 3, and to enable transmission in mode 0. Set to enable reception in all modes.
3	TB8	**Transmit bit 8** Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.
2	RB8	**Receiver bit 8** Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.
1	TI	**Transmit Interrupt flag** Set by the transmitter after the last data bit is transmitted. Must be cleared by software.
0	RI	**Receive Interrupt flag** Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.

Reset Value= 0000 0000b

Table 140.

SP - Stack pointer Register (81h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0111b
Not bit addressable

Table 141. T2CON

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer 2 overflow.
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. Set to cause the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software.
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T2 input pin).
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b
Bit addressable

Table 142. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	**T2OE**	**DCEN**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Decrement Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b
Not bit addressable

Table 143. TCON Register

TCON - Timer Control Register (88h)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer 1 overflow.
6	TR1	**Timer 1 Run control bit** Clear to turn off timer 1. Set to turn on timer 1.
5	TF0	Timer 0 overflow Flag Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer 0 overflow.
4	TR0	Timer 0 Run control bit Clear to turn off timer 0. Set to turn on timer 0.
3	IE1	Interrupt 1 Edge flag Cleared when interrupt processed. Set by hardware when external interrupt 1 edge detected.
2	IT1	Interrupt 1 Type control bit Clear to specify low level triggered external interrupt 1. Set to specify falling edge triggered external interrupt 1.
1	IE0	Interrupt 0 Edge flag Cleared when interrupt processed. Set by hardware when external interrupt 0 edge detected.
0	IT0	Interrupt 0 Type control bit Clear to specify low level triggered external interrupt 0. Set to specify falling edge triggered external interrupt 0.

Reset Value = 0000 0000b
Bit addressable

Table 144. TH0 Register

TH0 - Timer 0 High Register (8Ch)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 145. TH1 Register

TH1 - Timer 1 High Register (8Dh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 146. TH2 Register

TH2 - Timer 2 High Register (CDh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 147. TMOD

TMOD - Timer Mode Control (89h)

7	6	5	4	3	2	1	0
GATE	**C/T#**	**M1**	**M0**	**GATE**	**C/T#**	**M1**	**M0**
Timer 1				**Timer 0**			

Bit Number	Bit Mnemonic	Description
7	GATE	**Timer 1 Gating control bit** Clear to enable timer 1 whenever TR1 bit is set. Set to enable timer 1 only while INT1# pin is high and TR1 bit is set.
6	C/T#	Timer/Counter 1 select bit Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T1 input pin).
5	M1	Timer 1 Mode select bits M1 M0 Mode Description 0 0 0 TH1 is an 8-bit timer/counter with a 5-bit prescaler (TL1). 0 1 1 (TH1,TL1) is an 16-bit timer/counter. 1 0 2 TL1 is an 8-bit auto-reload timer/counter. TH1 holds a value which is to be reloaded into TL1 at each overflow. 1 1 3 Timer 1 is stopped and retains count.
4	M0	
3	GATE	Timer 0 Gating control bit Clear to enable timer 0 whenever TR0 bit is set. Set to enable timer 0 only while INT0# pin is high and TR0 bit is set.
2	C/T#	Timer/Counter 0 select bit Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T0 input pin).
1	M1	**Timer 0 Mode select bits** M1 M0 Mode Description 0 0 0 TH0 is an 8-bit timer/counter with a 5-bit prescaler (TL0). 0 1 1 (TH0,TL0) is an 16-bit timer/counter. 1 0 2 TL0 is an 8-bit auto-reload timer/counter. TH0 holds a value which is to be reloaded into TL1 at each overflow. 1 1 3 TL0 is an 8-bit timer/counter controlled by TR0 and TF0 bits. TH0 is an 8-bit timer/counter controlled by TR1 and TF1 bits.
0	M0	

Reset Value = 0000 0000b
Not bit addressable

Table 148. TL0 Register

TLO - Timer 0 Low Register (8Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 149. TL1 Register

TL1 - Timer 1 Low Register (8Bh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 150. TL2 Register

TL2 - Timer 2 Low Register (CCh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 151. WDTPRG Register

WDTPRG - WatchDog Timer Duration Programming Register (A7H)

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	S2	**WatchDog Timer Duration selection bit 2** Work in conjunction with bit 1 and bit 0.
1	S1	**WatchDog Timer Duration selection bit 1** Work in conjunction with bit 2 and bit 0.
0	S0	**WatchDog Timer Duration selection bit 0** Work in conjunction with bit 1 and bit 2.

Reset Value = XXXX X000b
Not bit addressable

Table 152. WDTRST Register

WDTRST - WatchDog Timer Enable Register (Write Only) (A6H)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb
Not bit addressable

24. Typical Application

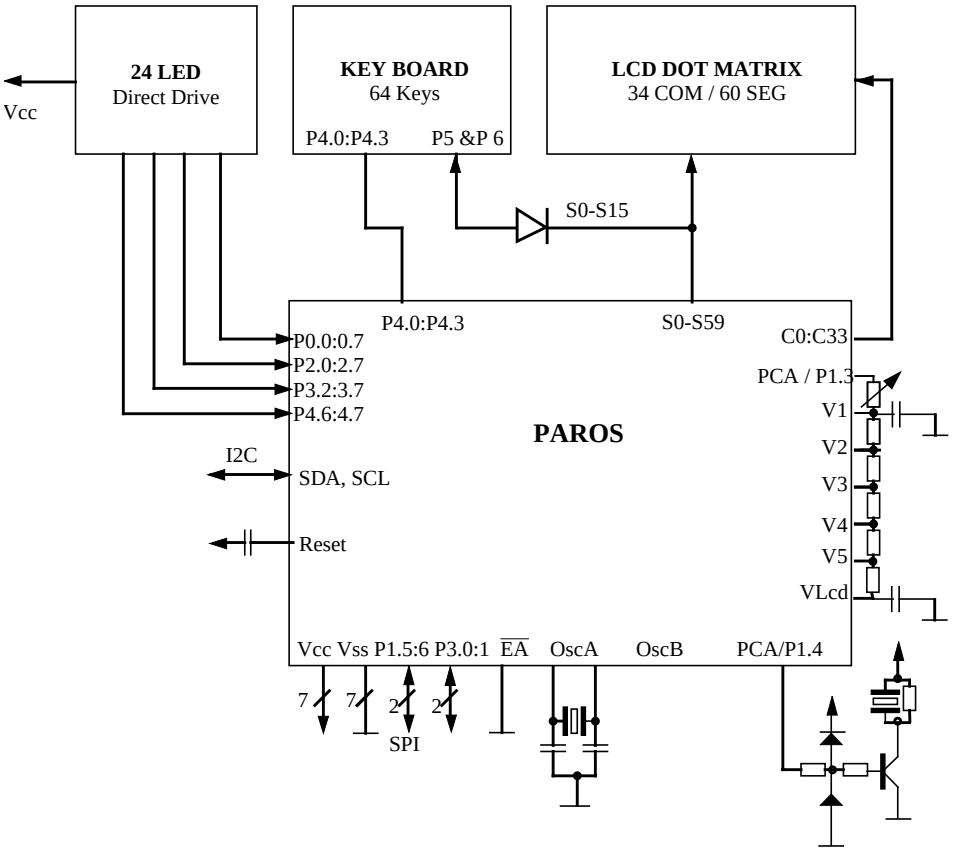


Figure 55. Typical Application

25. Extended Application

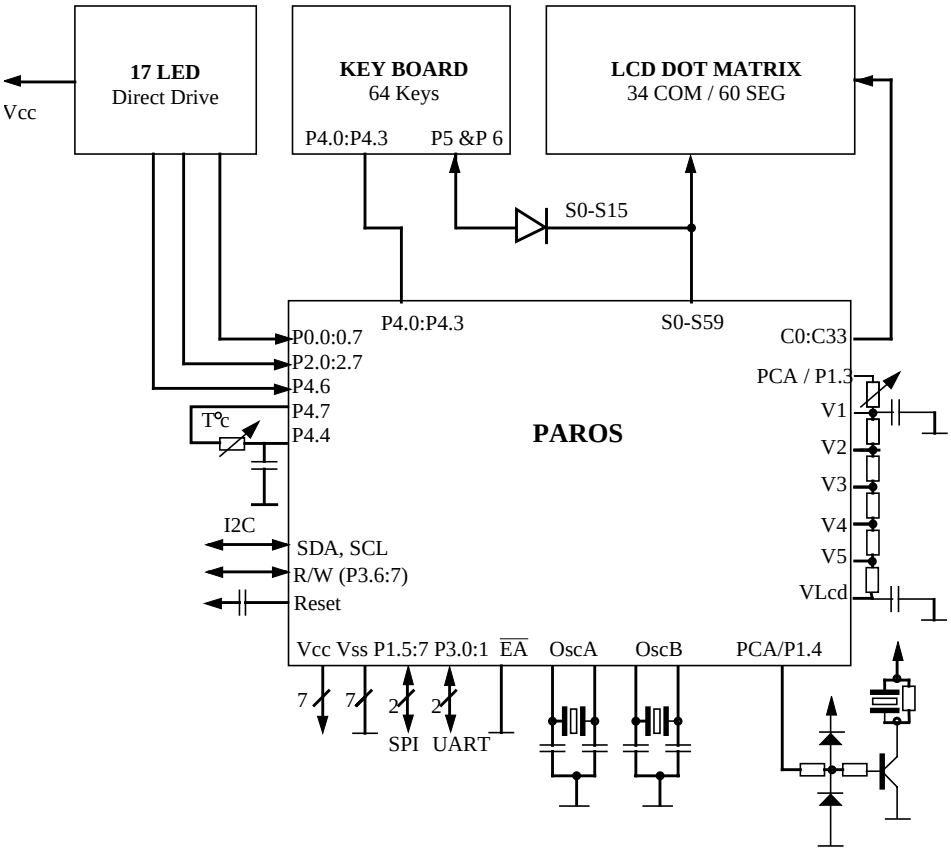
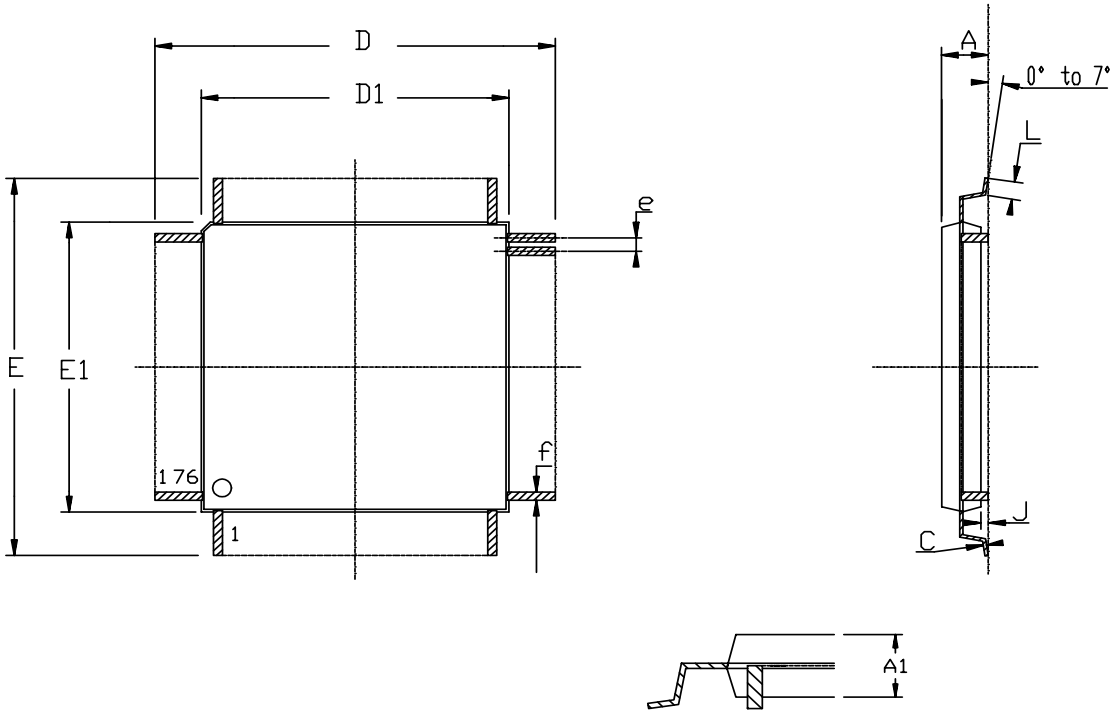


Figure 56. Extended Application

26. TQFP176 Package



	MM		INCH	
	Min	Max	Min	Max
A	1.40	1.60	.055	.063
A1	1.35	1.45	.053	.057
C	0.090	0.200	.004	.008
D	25.90	26.10	1.020	1.028
D1	23.90	24.00	.941	.949
E	25.90	26.10	1.020	1.028
E1	23.90	24.10	.941	.949
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.020 BSC	
f	0.17	0.27	.007	.011

26.1

PAD Name	Pin	PAD Name	Pin	PAD Name	Pin	PAD Name	Pin
$V_{CC}1$	3	SEG25	47	P.0.6	92	COM1	136
V4	4	SEG24	48	P.0.7	93	COM2	137
V3	5	SEG23	49	Rst	94	COM3	138
V_{CC}ANA	6	SEG22	50	P.3.0	95	COM4	139
SEG59	7	SEG21	51	P.3.1	96	COM5	140
SEG58	8	SEG20	52	P.3.2	97	COM6	141
SEG57	9	SEG19	53	P.3.3	98	COM7	142
SEG56	10	SEG18	54	P.3.4	99	COM8	143
SEG55	11	SEG17	55	P.3.5	100	COM9	144
SEG54	12	SEG16	56	P.3.6	101	COM10	145
SEG53	13	SEG15	57	P.3.7	102	COM11	146
SEG52	14	SEG14	58	XTALA2	103	COM12	147
SEG51	15	SEG13	59	XTALA1	104	COM13	148
SEG50	16	SEG12	60	XTALB2	105	COM14	149
SEG49	17	SEG11	61	XTALB1	106	COM15	150
SEG48	18	SEG10	62	V_{CC}Core2	107	COM16	151
SEG47	19	SEG9	63	V_{SS}Core2	108	COM17	152
SEG46	20	SEG8	64	EAVPP	109	COM18	153
SEG45	21	SEG7	65	$V_{SS}5$	110	COM19	154
SEG44	22	SEG6	66	P.2.0	111	COM20	155
V_{CC}Core1	23	SEG5	67	P.2.1	112	COM21	156
V_{SS}Core1	24	SEG4	68	P.2.2	113	COM22	157
SEG43	25	SEG3	69	P.2.3	114	COM23	158
SEG42	26	SEG2	70	P.2.4	115	COM24	159
SEG41	27	SEG1	71	P.2.5	116	COM25	160
SEG40	28	SEG0	72	P.2.6	117	COM26	161
SEG39	29	P.4.0	73	P.2..7	118	COM27	162
SEG38	30	P.4.1	74	ALE	119	COM28	163
SEG37	31	P.4.2	75	PSENB	120	COM29	164
SEG36	32	P.4.3	76	P.1.0	121	COM30	165
SEG35	33	P.4.4	77	P.1.1	122	COM31	166
SEG34	34	P.4.5	78	P.1.2	123	COM32	167
SEG33	35	P.4.6	79	P.1.3	124	COM33	168
SEG32	36	P.4.7	80	P.1.4	125	V_{SS}ANA	169
SEG31	37	P.0.0	81	P.1.5	126	V2	170
SEG30	38	P.0.1	82	P.1.6	127	V5	171
SEG29	39	P.0.2	83	P.1.7	128	V1	172
SEG28	40	P.0.3	84	SCL	129	VLCD	173
SEG27	41	P.0.4	85	SDA	130	$V_{SS}1$	174
SEG26	42	P.0.5	86	$V_{SS}4$	131	V_{SS}BUF3	175
$V_{SS}2$	43	$V_{CC}3$	87	$V_{CC}4$	134		
$V_{CC}2$	46	$V_{SS}3$	91	COM0	135		

Pins 1, 2, 44, 45, 88, 89, 90, 132, 133 and 176 are not connected.