ANALOG DEVICES

MicroConverter® Multi-Channel 12-bit ADC and DACs, ARM7TDMI® Core

Preliminary Technical Data

ADuC7023

FEATURES

Analog I/O
  8 Channel, 12-bit, 1MSPS ADC
  Fully differential and single-ended modes
  0 to V_{REF} Analog Input Range
  Quad 12-bit Voltage Output DACs
  On-Chip 20ppm/°C Voltage Reference
  On-Chip Temperature Sensor (±3°C)
  Uncommitted Voltage Comparator
Microcontroller
  ARM7TDMI Core, 16/32-bit RISC architecture
  JTAG Port supports code download and debug
  Clocking options: - Trimmed On-Chip Oscillator
                                 - External Watch crystal
                                 - External clock source
  45MHz PLL with Programmable Divider
Memory
  62k Bytes Flash/EE Memory, 8k Bytes SRAM
  In-Circuit Download, JTAG based Debug
  In application programmability

On-Chip Peripherals
  UART, I²C and SPI Serial I/O
  19 Pin GPIO Port
  4 X General Purpose Timers
  Power Supply Monitor
  16-bit PWM
  PLA – Programmable Logic (Array)
Power
  Specified for 3V operation
  Active Mode: 6mW (@1MHz)
                          300mW (@45MHz)
Packages and Temperature Range
  48 Pin LFCSP 7x7mm body package
  Fully specified for –40°C to 85°C operation
Tools
  Low-Cost QuickStart Development System
  Full Third-Party Support

APPLICATIONS

Smart Sensors, Precision Instrumentation
Base Station Systems, Optical Networking

FUNCTIONAL BLOCK DIAGRAM

Figure 1

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700   **www.analog.com**
Fax: 781.326.8703   © 2003 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

REVISION HISTORY

Revision PrA: Initial Preliminary Version

ADUC7023—SPECIFICATIONS

Table 1. (AV$_{DD}$ = IOV$_{DD}$ = 3 V ± 10%, V$_{REF}$ = 2.5 V Internal Reference, All specifications T$_A$ = T$_{MAX}$ to T$_{MIN}$, unless otherwise noted.)

Parameter	ADuC7023[1]	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS			
DC Accuracy			f$_{SAMPLE}$ = 1MSPS
Resolution	12	Bits	
Integral Nonlinearity	±1.5	LSB max	
Differential Nonlinearity	±1	LSB max	
Offset Error	±5	LSB max	
Gain Error	±5	LSB max	
DYNAMIC PERFORMANCE			Fin = 10kHz Sine Wave, f$_{SAMPLE}$ = 1MSP S
Signal-to-Noise Ratio (SNR)	71	dB typ	
Total Harmonic Distortion (THD)	-78	dB typ	
Peak Harmonic or Spurious Noise	-78	dB typ	
ANALOG INPUT			
Input Voltage Ranges			
Differential mode	V$_{CM}$[2]±V$_{REF}$/2	Volts	
Single-ended mode	0 to V$_{REF}$	Volts	
Leakage Current	±5	μA max	
Input Capacitance	20	pF typ	When in track
	6	pF typ	When in hold
REFERENCE INPUT/OUTPUT			0.47μF from V$_{REF}$ (pin x) to AGND
Input Voltage Range	0.625	V min	
	AV$_{DD}$	V max	
Output Voltage	2.5	V	
Accuracy	±2.5	% max	
Reference Temperature Coefficient	±20	ppm/°C typ	
Output Impedance	10	Ω	
DAC CHANNEL SPECIFICATIONS			R$_L$ = 5kΩ, C$_L$ = 100pF
DC ACCURACY			
Resolution	12	Bits	
Relative Accuracy	±3	LSB typ	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Offset Error	±0.5	% max	
Gain Error	±10	mV	
ANALOG OUTPUTS			
Output Voltage Range	5	mV min	Unloaded
	V$_{REF}$	V max	Unloaded
Output Impedance	1	Ω max	
AC CHARACTERISTICS			
Voltage Output Settling Time	10	μs typ	
COMPARATOR			
Response Time	5	μs typ	
TEMPERATURE SENSOR			
Voltage TC	-2.0	mV/°C typ	
Accuracy	±3	°C typ	
POWER SUPPLY MONITOR (PSM)			
IOV$_{DD}$ Trip Point Selection	2.79	V	Two selectable Trip Points
	3.07	V	
Power Supply Trip Point Accuracy	±2.5	% max	Of the selected nominal Trip Point Voltage

Parameter	ADuC7023[1]	Unit	Test Conditions/Comments
Flash/EE MEMORY			
Endurance[3]	10,000	Cycles min	
Data Retention[4]	30	Years min	$T_J = 55°C$
Logic Ouputs			
V_{OH}, Output High Voltage	TBD	V min	
V_{OL}, Output Low Voltage	TBD	V max	
POWER REQUIREMENTS			
Power Supply Voltage Range			
AV_{DD} – AGND and IOV_{DD} - IOGND	2.7	V min	
	3.6	V max	
Power Consumption Normal Mode	2	mA	1MHz clock
	100	mA	45MHz clock
Power Consumption Power Down Mode	1	mA	

[1] Temperature Range –40°C to +85°C.
[2] Common-mode voltage. The input signal can be centered on any choice of dc common-mode voltage as long as this value is in the range specified in the ADC section.
[3] Endurance is qualified to 50,000 cycles as per JEDEC Std. 22 method A117 and measured at -40°C, +25°C and +85°C. Typical endurance at 25°C is 70,000 cycles.
[4] Retention lifetime equivalent at junction temperature (Tj) = 55°C as per JEDEC Std. 22 method A117.

TERMINOLOGY

ADC Specifications

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

Gain Error

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent upon the number of quantization levels in the digitisation process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (Noise + Distortion) = (6.02N + 1.76) dB

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change..

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings (T$_A$ = 25°C unless otherwise noted)

| Parameter	Rating
AV$_{DD}$ to DV$_{DD}$	TBD
AGND to DGND	TBD
DV$_{DD}$ to DGND, AV$_{DD}$ to AGND	TBD
Digital Input Voltage to DGND	TBD
Digital Output Voltage to DGND	TBD
VREF to AGND	TBD
Analog Inputs to AGND	TBD
Operating Temperature Range Industrial ADuC7023	−40°C to +85°C
Storage Temperature Range	TBD
Junction Temperature	TBD
θ$_{JA}$ Thermal Impedance (ADuC7023BCP)	TBD
Lead Temperature, Soldering	
Vapor Phase (60 sec)	TBD
Infrared (15 sec)	TBD

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION

48-Leads CSP
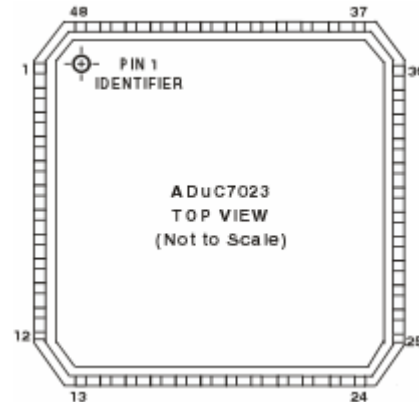
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC7023	−40°C to + 85°C	48-Lead Chip Scale Package	CP-48
EVAL_ADuC7023QS		QuickStart-Plus Development System	

Contact the factory for chip availability.

ESD Caution

PIN FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions

Pin# ADuC7023	Mnemonic	Type*	Function
x	ADC0	I	Single-ended or differential Analog input 0
x	ADC1	I	Single-ended or differential Analog input 1
x	ADC2/CMP0	I	Single-ended or differential Analog input 2
x	ADC3/CMP1	I	Single-ended or differential Analog input 3
x	ADC4	I	Single-ended or differential Analog input 4
x	ADC5	I	Single-ended or differential Analog input 5
x	ADC6	I	Single-ended or differential Analog input 6
x	ADC7	I	Single-ended or differential Analog input 7
x	GND$_{REF}$	S	Ground voltage reference for the ADC. For optimal performance the analog power supply should be separated from IOGND and DGND
x	DAC0/ADC12	I/O	DAC0 Voltage Output / Single-ended or differential Analog input 12
x	DAC1/ADC13	I/O	DAC1 Voltage Output / Single-ended or differential Analog input 13
x	DAC2/ADC14	I/O	DAC2 Voltage Output / Single-ended or differential Analog input 14
x	DAC3/ADC15	I/O	DAC3 Voltage Output / Single-ended or differential Analog input 15
x	TMS	I	JTAG Test Port Input - Test Mode Select. Debug and download access
x	TDI	I	JTAG Test Port Input – Test Data In. Debug and download access
x	TCK/XCLK	I	JTAG Test Port Input - Test Clock. Debug and download access/ Input to the internal clock generator circuits
x	TDO	O	JTAG Test Port Output - Test Data Out. Debug and download access
x	TRST/GPIO	I	JTAG Test Port Input – Test Reset. Debug and download access / General Purpose Input-Output
x	IOGND	S	Ground for GPIO. Typically connected to DGND
x	IOV$_{DD}$	S	3.3V Supply for GPIO and input of the on-chip voltage regulator.
x	LV$_{DD}$	S	2.5V. Output of the on-chip voltage regulator. Must be connected to a 1μF capacitor to DGND
x	DGND	S	Ground for digital logic. Must be connected to two 0.1uF capacitors to the two LV$_{DD}$ pins
x	RST	I	Reset Input. (active low)
x	IRQ0/GPIO/CONV$_{START}$/PLA	I/O	Multifunction I/O pin: External Interrupt Request0 / General Purpose Input-Output / Start conversion input signal for ADC / Programmable Logic Array Input-Output
x	IRQ1/GPIO/PLA	I/O	Multifunction I/O pin: External Interrupt Request1 / General Purpose Input-Output / Programmable Logic Array Input-Output

Pin# ADuC7023	Mnemonic	Type*	Function
x	BM/GPIO/CMP$_{OUT}$/PLA	I/O	Multifunction I/O pin: Boot Mode. The ADuC702X will enter UART serial download mode if BM is low at reset and will execute code if BM is pulled high at reset through a 1kOhm resistor/ General Purpose Input-Output / Voltage Comparator Output / Programmable Logic Array Input-Output
x	GPO/PLA/MRESET	O	Multifunction pin: driven low after reset General Purpose Output / Programmable Logic Array Output / Power on reset output
x	V$_{REF}$	I/O	2.5V internal Voltage Reference. Must be connected to a 0.47uF capacitor when using the internal reference.
x	DACGND	S	Ground for the DAC. Typically connected to AGND
x	AGND	S	Analog Ground. Ground reference point for the analog circuitry
x	DACV$_{DD}$	S	3.3V Power Supply for the DACs. Typically connected to AV$_{DD}$
x	AV$_{DD}$	S	3.3V Analog Power
x	GPIO/SPM0/PLAI0	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / I²C / Programmable Logic Array Input-Output
x	GPIO/SPM1/PLAI1	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / I²C / Programmable Logic Array Input-Output
x	GPIO/SPM2/PLAI2	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / Programmable Logic Array Input-Output
x	GPIO/SPM3/PLAI3	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / Programmable Logic Array Input-Output
x	GPIO/SPM4/PLAI4	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / SPI / Programmable Logic Array Input-Output
x	GPIO/SPM5/PLAI5	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / SPI / Programmable Logic Array Input-Output
x	GPIO/SPM6/PLAI6	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / SPI / Programmable Logic Array Input-Output
x	GPIO/SPM7/PLAI7	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / SPI / Programmable Logic Array Input-Output
x	GPIO/SPM8/PLAI8	I/O	Serial Port Multiplexed: General Purpose Input-Output / Output for External Clock signal / UART / Programmable Logic Array Input-Output
x	GPIO/SPM9/PLAI9	I/O	Serial Port Multiplexed: General Purpose Input-Output / UART / Programmable Logic Array Input-Output
x	XCLKO	O	Output to the crystal oscillator inverter
x	XCLKI	I	Input to the crystal oscillator inverter and input to the internal clock generator circuits
x	GPIO/PWM0$_H$/PLAI8	I/O	General Purpose Input-Output / PWM phase 0 high side output / Programmable Logic Array Input of element 8
x	GPIO/PWM0$_L$/PLAI9	I/O	General Purpose Input-Output / PWM phase 0 low side output / Programmable Logic Array Input of element 9
x	GPIO/PLAO8	I/O	General Purpose Input-Output / Programmable Logic Array Output of element 8
x	GPIO/PLAO9	I/O	General Purpose Input-Output / Programmable Logic Array Output of element 9

* I = Input, O = Output, S = Supply.

- No pin assigned.

GENERAL DESCRIPTION

The ADuC7023 is fully integrated, 1MSPS, 12-bit data acquisition systems incorporating a high performance multi-channel ADC, a 16/32-bit MCU and Flash/EE Memory on a single chip.

The ADC consists of 8 single-ended inputs. An additional 4 inputs are available but are multiplexed with the 4 DAC output pins. The ADC can operate in single-ended or differential input mode with a fully flexible front end. The ADC input voltage is 0 to V_{REF}. Low drift bandgap reference, temperature sensor and voltage comparator complete the ADC peripheral set.

The part also integrates 4 buffered voltage output DACs on-chip. The DAC output range is 0 to AV_{DD} max.

The device has three clock options, internal oscillator, external watch crystal or external clock source. By default it operates from the on-chip oscillator and PLL generating an internal high-frequency clock of 45 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI, 16/32-bit RISC machine, offering up to 45 MIPS peak performance. 62k Bytes of non-volatile Flash/EE are provided on-chip as well as 8k Bytes of SRAM. Both the Flash/EE and SRAM memory arrays are mapped into a single linear array.

On-chip factory firmware supports in-circuit serial download via the UART and JTAG serial interface ports while non-intrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart system supporting this MicroConverter family.

The parts operate from 2.7V to 3.6V and are specified over an industrial temperature range of -40°C to 85°C. When operating @45MHz the power dissipation is 300mW. The ADuC7023 is available in a 48-lead LFCSP package.

OVERVIEW OF THE ARM7TDMI CORE

The ARM7 core is a 32-bit Reduced Instruction Set Computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8, 16 or 32 bits and the length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with 4 additional features:
- T support for the Thumb (16 bit) instruction set.
- D support for debug
- M support for long multiplies
- I include the EmbeddedICE module to support embedded system debugging.

Thumb mode (T)

An ARM instruction is 32-bits long. The ARM7TDMI processor supports a second instruction set that has been compressed into 16-bits, the Thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However the Thumb mode has two limitations:
- Thumb code usually uses more instructions for the same job, so ARM code is usually best for maximising the performance of the time-critical code.
- The Thumb instruction set does not include some instructions that are needed for exception handling, so ARM code needs to be used for exception handling.

See ARM7TDMI User Guide for details on the core architecture, the programming model and both the ARM and ARM Thumb instruction sets.

Long multiple (M)

The ARM7TDMI instruction set includes four extra instructions which perform 32-bit by 32-bit multiplication with 64-bit result and 32-bit by 32-bit multiplication-accumulation (MAC) with 64-bit result.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers which allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.
When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, The processor registers may be inspected as well as the Flash/EE, the SRAM and the Memory Mapped Registers.

Exceptions

ARM supports five types of exceptions, and a privileged processing mode for each type. The five type of exceptions are:
- Normal interrupt or IRQ. It is provided to service general-purpose interrupt handling of internal and external event
- Fast interrupt or FIQ. It is provided to service data transfer or communication channel with low latency. FIQ has priority over IRQ
- Memory abort
- Attempted execution of an undefined instruction
- Software interrupt (SWI) instruction which can be used to make a call to an operating system.

Typically the programmer will define interrupts as IRQ but for higher priority interrupt, i.e. faster response time, the programmer can define interrupt as FIQ.

ARM Registers

ARM7TDMI has a total of 37 registers, of which 31 are general purpose registers and six are status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general purpose 32-bit registers (r0 to r14), the program counter (r15) and the current program status register (CPSR) are usable. The remaining registers are used only for system-level programming and for exception handling.

When an exception occurs, some of the standard register are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (r13) and the link register (r14) as represented in Figure 2. The fast interrupt mode has more registers (8 to 12) for fast interrupt processing, so that the interrupt processing can begin without the need to save or restore these registers and thus save critical time in the interrupt handling process.
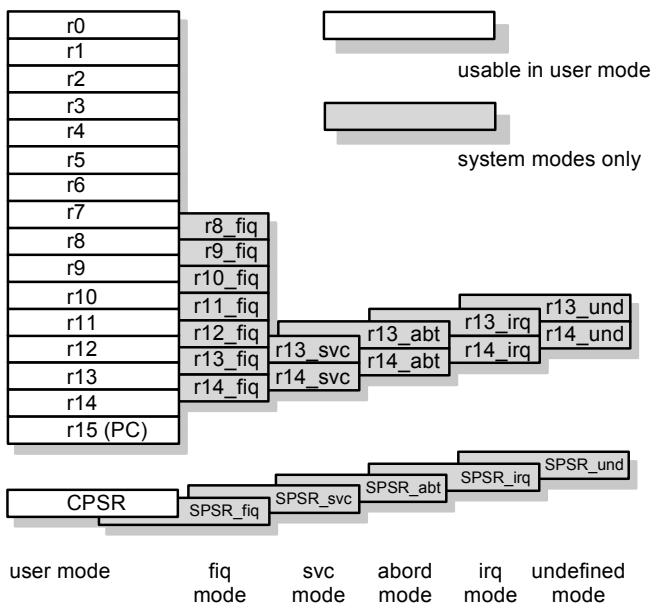

Figure 2: register organisation

Interrupt latency

The worst case latency for an FIQ, assuming that it is enabled, consists of the longest time the request can take to pass through the synchronizer, plus the time for the longest instruction to complete (the longest instruction is an LDM) which loads all the registers including the PC, plus the time for the data abort entry, plus the time for FIQ entry. At the end of this time, the ARM7TDMI will be executing the instruction at 0x1C (FIQ interrupt vector address). The total time is 28 processor cycles, which is just over 622 nanoseconds in a system using a continuous 45 MHz processor clock.

The maximum IRQ latency calculation is similar, but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time.The minimum latency for FIQ or IRQ interrupts is five cycles in total which consists of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI will always be run in ARM (32-bit) mode when in privileged modes, i.e. when executing interrupt service routines.

Memory Access

The ARM core sees memory as a linear array of 2^{32} byte location where the different blocks of memory are mapped as detailed in the next chapter (Memory Organisation) Figure 4.

The ADuC7023 memory organisation is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address.
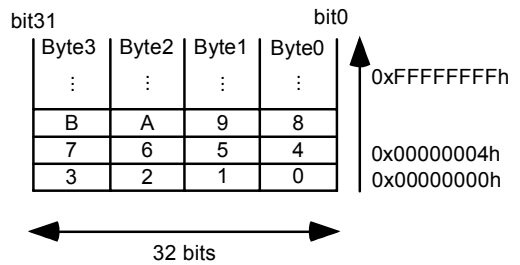

Figure 3: little endian format
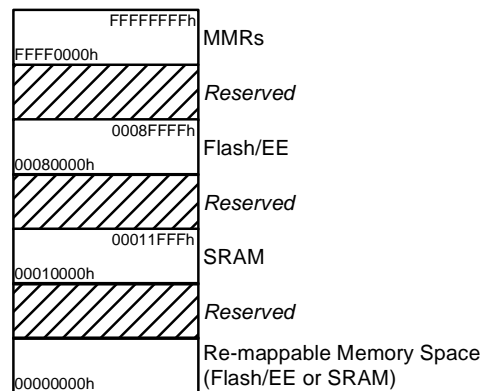
MEMORY ORGANISATION

Figure 4: Physical memory map

The ADuC7023 incorporates two separate blocks of memory, 8kByte of SRAM and 64kByte of On-Chip Flash/EE memory. 62kByte of On-Chip Flash/EE memory are available to the user, and the remaining 2kBytes are reserved for the factory configured boot page. These two blocks are mapped as shown Figure 4.

Flash/EE Memory

The total 64kBytes of Flash/EE are organised as 32k X 16 bits. 31k X 16 bits are user space and 1k X 16 bits is reserved for boot loader. The page size of this Flash/EE memory is 512Bytes.

62kBytes of Flash/EE are available to the user for code and non-volatile data. There is no distinction between data and program as ARM code shares the same space.

The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is therefore recommended to use Thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 45MHz in Thumb mode and 22.5MHz in full ARM mode.

Erasing a page (512 Bytes) is completed in 20ms, while writing a half-word (2 bytes) is 22μs and writing a page 6ms. During these erasing and writing times, the processor won't be able to access the Flash/EE, so it is recommended to erase the page(s) at the start of the program execution if possible and to place the interrupt routine in RAM so that the processor can service an interrupt when erasing/writing in Flash/EE.

SRAM

8kBytes of SRAM are available to the user, organised as 2k X 32 bits, i.e. 2kWords. ARM code can run directly from SRAM at 45MHz , given that the SRAM array is configured as a 32-bit wide memory array.

Memory Mapped Registers

The Memory Mapped Register (MMR) space is mapped into the upper 2 pages of the Flash/EE space and accessed by indirect addressing through the ARM7 banked registers.

It provides an interface between the CPU and all on-chip peripherals. All registers except the core registers reside in the MMR area. The MMR registers include control, configuration, mode, status and data registers that provide an interface between the CPU and each peripheral.
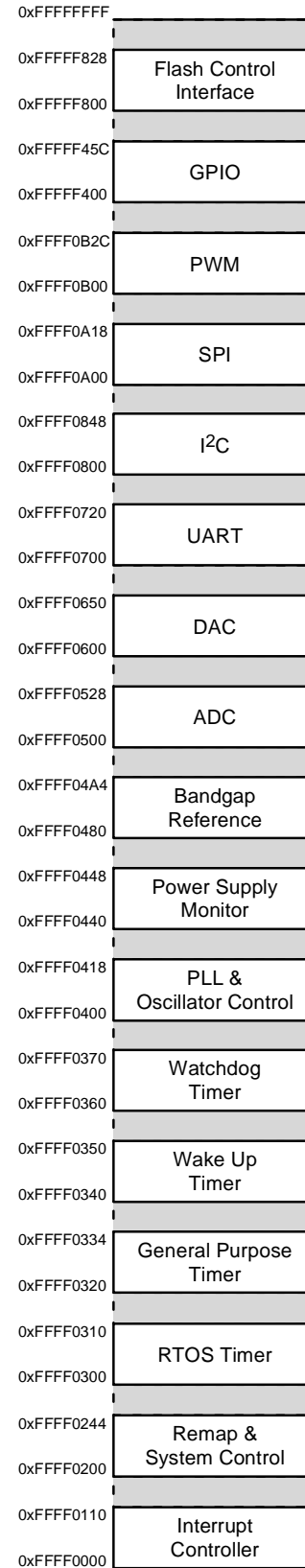
Address	Block
0xFFFFFFFF	
0xFFFFF828 – 0xFFFFF800	Flash Control Interface
0xFFFFF45C – 0xFFFFF400	GPIO
0xFFFF0B2C – 0xFFFF0B00	PWM
0xFFFF0A18 – 0xFFFF0A00	SPI
0xFFFF0848 – 0xFFFF0800	I²C
0xFFFF0720 – 0xFFFF0700	UART
0xFFFF0650 – 0xFFFF0600	DAC
0xFFFF0528 – 0xFFFF0500	ADC
0xFFFF04A4 – 0xFFFF0480	Bandgap Reference
0xFFFF0448 – 0xFFFF0440	Power Supply Monitor
0xFFFF0418 – 0xFFFF0400	PLL & Oscillator Control
0xFFFF0370 – 0xFFFF0360	Watchdog Timer
0xFFFF0350 – 0xFFFF0340	Wake Up Timer
0xFFFF0334 – 0xFFFF0320	General Purpose Timer
0xFFFF0310 – 0xFFFF0300	RTOS Timer
0xFFFF0244 – 0xFFFF0200	Remap & System Control
0xFFFF0110 – 0xFFFF0000	Interrupt Controller

Figure 5: Memory Mapped

ADC CIRCUIT INFORMATION

GENERAL OVERVIEW

The Analog Digital Converter (ADC) incorporates a fast, multichannel, 12-bit, 1MSPS, single supply ADC. This block provides the user with multichannel mux, differential track-and-hold, on-chip reference and ADC.

The ADC consists of a 12-bit successive-approximation converter based around two capacitor DACs. It can operate in one of three different modes, depending on the input signal configuration :

- *fully differential mode*, for small and balanced signals
- *single-ended mode*, for any single-ended signals
- *pseudo-differential mode*, for any single-ended signals, taking advantage of the common mode rejection offered by the pseudo differential input.

The converter accepts an analog input range of 0 to V_{REF} when operating in single-ended mode or pseudo-differential mode. In fully differential mode, the input signal must be balanced around a common mode voltage V_{CM}, in the range 0V to AV_{DD} and with a maximum amplitude of 2 V_{REF} (see Figure 6).
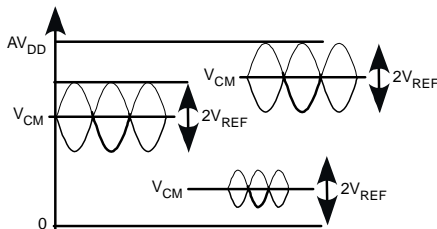

Figure 6: examples of balanced signals for fully differential mode

A high precision, low drift, and factory calibrated 2.5 V reference is provided on-chip. An external reference can also be connected as described later.

Single or continuous conversion modes can be initiated in software. An external CONV$_{START}$ on pin x, an output generated from the on-chip PLA or a Timer2 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip bandgap reference proportional to absolute temperature can also be routed through the front end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

ADC TRANSFER FUNCTION

Pseudo-differential and single-ended modes

In pseudo-differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with 1 LSB = FS/4096 or 2.5 V/4096 = 0.61 mV or 610 µV when V_{REF} = 2.5 V. The ideal code transitions occur midway between successive integer LSB values (i.e. 1/2 LSB, 3/2 LSBs, 5/2 LSBs, . . ., FS −3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 7.
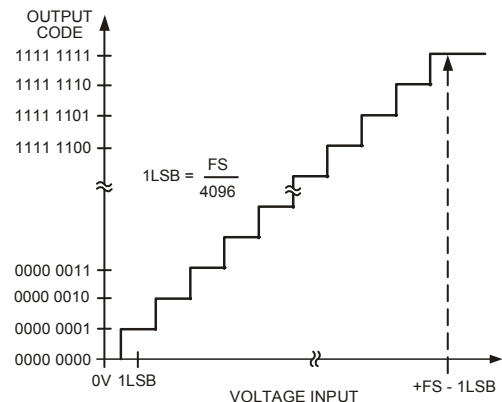

Figure 7: ADC transfer function in pseudo differential mode or single-ended mode

Fully differential mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins (i.e., V_{IN+} − V_{IN-}). V_{IN+} and V_{IN-} are simultaneously driven by two signals each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore −V_{REF} to +V_{REF} p-p (i.e., 2 X V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e., (V_{IN+} + V_{IN-})/2, and is therefore the voltage that the two inputs are centred on. This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally and its range varies with V_{REF}, (see driving the ADC).

The output coding is two's complement in fully differential mode with 1 LSB = $2V_{REF}$/4096 or 2x2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs, . . ., FS −3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 8.
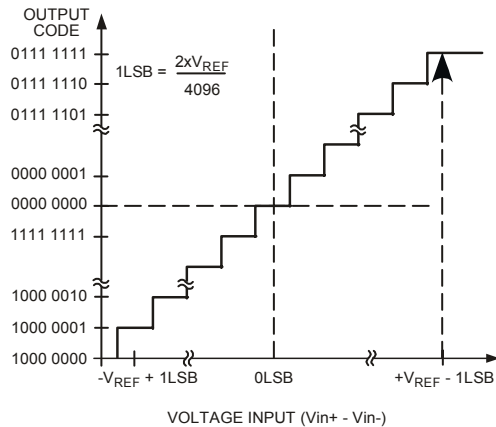
Figure 8: ADC transfer function in differential mode

TYPICAL OPERATION

Once configured via the ADC control and configuration registers, the ADC will convert the analog input and provide a 12-bit result in the ADC data register.

For software compatibility with the ADuC706X family, whose ADC is 16 bits, the ADC data register is a 32-bit register. The top bit are the sign bits and the 12-bit result is placed from bit 16 to 27 as shown in Figure 9. Again, it should be noted that in fully differential mode, the result is represented in two's complement format, and in pseudo differential and single-ended mode, the result is represented in straight binary format.
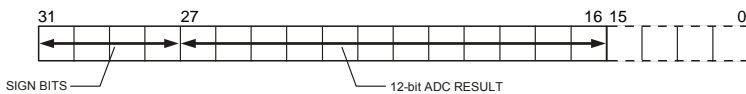

Figure 9: ADC Result Format

ADC MMRS INTERFACE

Six MMRs are used to control the operation of the ADC peripheral block, these include:

- **ADCCON:** ADC Control Register, for channel selection and conversion start
- **ADCCFG:** ADC Configuration Register for mode of operation and conversion type
- **ADCSTA:** ADC Status Register, indicates when an ADC conversion result is ready
- **ADCDAT:** ADC Data Result Register, hold the 12-bit ADC result
- **ADCRST:** ADC Reset Register. Resets all the ADC registers to their default value.

- **ADCOF:** 10-bit calibration register for offset error.

- **ADCGN:** 10-bit calibration register for gain error.

ADC END-POINT CALIBRATION

The ADuC702X has two ADC calibration coefficients, one for offset calibration and one for gain calibration. Both the offset and gain calibration coefficients are 10-bit words, located in the MMR area.

The offset calibration coefficient compensates for dc offset errors in both the ADC and the input signal. Increasing the offset coefficient compensates for positive offset, and effectively pushes the ADC transfer function down. Decreasing the offset coefficient compensates for negative offset, and effectively pushes the ADC transfer function up. The maximum offset that can be compensated is typically ±3.125% of V_{REF}, which equates to typically ±78 mV with a 2.5 V reference.

Similarly, the gain calibration coefficient compensates for dc gain errors in both the ADC and the input signal. Increasing the gain coefficient compensates for a smaller analog input signal range and scales the ADC transfer function up, effectively increasing the slope of the transfer function. Decreasing the gain coefficient compensates for a larger analog input signal range and scales the ADC transfer function down, effectively decreasing the slope of the transfer function. The maximum analog input signal range for which the gain coefficient can compensate is 1.031 X V_{REF}, and the minimum input range is 0.969 X V_{REF}, which equates to ±3.125% of the reference voltage.

TEMPERATURE SENSOR

The ADuC7023 provides a voltage output from an on-chip bandgap reference proportional to absolute temperature. It can also be routed through the front end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

BANDGAP REFERENCE

The ADuC7023 provides an on-chip bandgap reference of 2.5V, which can be used for the ADC and for the DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a capacitor of 0.47μF must be connected from the external V_{REF} pin to AGND, to ensure stability and fast response during ADC conversions.

A programmable option also allows an external reference input on the V_{REF} pin.

NONVOLATILE FLASH/EE MEMORY

FLASH/EE MEMORY OVERVIEW

The ADuC7023 incorporates Flash/EE memory technology on-chip to provide the user with non-volatile, in-circuit reprogrammable memory space.

Like EEPROM, Flash memory can be programmed in-system at a byte level, although it must first be erased, the erase being performed in page blocks. Thus, Flash memory is often and more correctly referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes non-volatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC702X, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace onetime programmable (OTP) devices at remote operating nodes.

FLASH/EE MEMORY AND THE ADUC7023

The ADuC7023 contains a 64 kByte array of Flash/EE Memory. The lower 62 Kbytes is available to the user and the upper 2 Kbytes of this Flash/EE program memory array contain permanently embedded firmware, allowing in-circuit serial download. These 2 Kbytes of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals (ADC, temperature sensor, bandgap references and so on).

This 2 KByte embedded firmware is hidden from user code.

The 62kBytes of Flash/EE memory can be programmed in-circuit, using the serial download mode or the JTAG mode provided or via parallel programming. A first boot downloader is also provided to facilitate in-circuit programming through any of the Serial Port, I2C, SPI or UART in applications where the BM pin can't be pulled low.

(1).Serial Downloading (In-Circuit Programming)

The ADuC702X facilitates code download via the standard UART serial port. The ADuC702X will enter serial download mode after a reset or power cycle if the BM pin is pulled low through an external 1kOhm resistor. Once in serial download mode, the user can download code to the full 62kBytes of Flash/EE memory while the device is in circuit in its target application hardware. A PC serial download executable is provided as part of the development system. The Serial Download protocol is detailed in a MicroConverter Application Note AN XXXX.

(2) Parallel Programming

The parallel programming protocol is detailed in a MicroConverter Application Note AN XXXX.

(3) JTAG access

The JTAG Download and Debug protocol is detailed in a MicroConverter Application Note AN XXXX.

(4) First boot downloader

The first boot downloader is placed in the user space and allows downloading code in the entire 62kB of user space and can therefore be used only once. It is provided to facilitate in-circuit programming in applications where the BM pin can't be pulled low.

On a first boot, if BM is not pulled low, the first boot downloader starts executing. It first checks for communication on any of the serial ports and if communication is detected, it downloads according to the protocol described in a MicroConverter Application Note AN XXXX.

FLASH/EE MEMORY SECURITY

The 62kByte of Flash/EE memory available to the user can be protected in reading, writing or both.

Bit 31, of the FEEPRO MMR protects the 62kBytes from being read through JTAG and also in parallel programming mode.

The other 31 bit of this register protect in writing, each bit protects 4 pages, i.e. 2kBytes. Write protection is activated for all type of access. Protection can be removed by writing again to this register if it is not protected by a key.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7023 incorporate quad 12-bit voltage output DACs on-chip. Each DAC has a rail-to-rail voltage output buffer capable of driving 5kΩ/100 pF. Each buffer can be bypassed to reduce offset and gain error introduced by the buffer. The DAC must then be buffered externally. The DACs have three selectable ranges, 0V to V_{REF}, 0V to DAC_{REF} (pin x) and 0V to AV_{DD}.

Each DAC is configurable independently through a DAC Control Register and a DAC Data Register.

POWER SUPPLY MONITOR

The Power Supply Monitor, monitors the IOV_{DD} supply on the ADuC7023. IOV_{DD} is monitored through PSMCON register which allows the programmer to configure the monitor to generate an interrupt once the external IOV_{DD} supply falls below one of two supply trip points.

This monitor function allows the user to save working registers to avoid possible data loss due to the low supply or brown-out conditions, and also ensures that normal code execution will not resume until a safe supply level has been well established.

COMPARATOR

The ADuC7023 also integrates an uncommitted voltage comparator. The output of the comparator can be configured to generate a system interrupt or can be routed directly to the Programmable Logic Array described later.

OSCILLATOR AND PLL - POWER CONTROL

The ADuC7023 integrates a 32.768kHz oscillator, a clock divider and a PLL. It is also intended for use with a 32.768 kHz watch crystal and the PLL or an external clock signal up to 45MHz.

The PLL locks onto a multiple of the internal oscillator to provide a stable 45.088 MHz clock for the system. The core can operate at this frequency, or at binary submultiples of it, to allow power saving. The default core clock is the PLL clock divided by 8 (CD = 3) or 5636 Hz.

The PLL and programmable clock divider are controlled via two MMRs, PLLCON and PLLSTAT. PLLCON controls the core clock frequency and the operating mode of the device while PLLSTAT monitors PLL and on-chip oscillator.

The core clock output can be enabled on ECLK pin.

DIGITAL PERIPHERALS

GENERAL PURPOSE I/O

The ADuC7023 provides 32 General Purpose bi-directional I/O pins (GPIO). All I/O pins are 5V tolerant which means that the GPIOs support an input voltage of 5V. In general many of the GPIO pins have multiple functions but by default the GPIO pins are configured in GPIO mode. All GPIO pins have internal pull up resistor and their drive capability is 2mA. The drive capability of the six pins supporting the PWM outputs is 8mA.

The 32 GPIO are grouped in 5 ports, controlled by the following MMRs:
- **GPxCON:** Port x Control Register, to enable port x.
- **GPxDAT:** Port x Configuration and Data Register. It configures the direction of the GPIO pins of port x, sets the output value for the pins configured as output and receives the stores the input value of the pins configured as input.

With x representing the port number (0 to 4).

SERIAL PORT MUX

The Serial Port Mux multiplexes the serial port peripherals (I^{2}C, SPI, UART) and the Programmable Logic Array (PLA) to a set of ten SPM GPIO pins. Each pin must be configured to one of its specific I/O function as described in table 4. This configuration is done via the SPMCON0 and SPMCON1 MMRs. By default these ten pins are configured as GPIOs.

	GPIO	UART	UART/I^{2}C/SPI	PLA
	00	**01**	**10**	**11**
SPM0	GPIO	SIN	I2CSCL	PLA
SPM1	GPIO	SOUT	I2CSDA	PLA
SPM2	GPIO	RTS	-	PLA
SPM3	GPIO	CTS	-	PLA
SPM4	GPIO	RI	SPICLK	PLA
SPM5	GPIO	DCD	SPIMISO	PLA
SPM6	GPIO	DSR	SPIMOSI	PLA
SPM7	GPIO	DTR	SPICSL	PLA
SPM8	GPIO	ECLK	SIN	PLA
SPM9	GPIO	PWM$_{TRIP}$	SOUT	PLA

Table 4: SPM configuration

UART SERIAL INTERFACE

The UART peripheral is a full-duplex Universal Asynchronous Receiver / Transmitter, fully compatible with the industry standard 16450. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The UART includes a fractional divider for baudrate generation and has complete MODEM-control capability. The UART function is made available on the following 10 pins of the ADuC7023:

Pin	Signal	Description
SPM0	SIN	Serial Receive Data
SPM1	SOUT	Serial Transmit Data
SPM2	RTS	Request To Send
SPM3	CTS	Clear To Send
SPM4	RI	Ring Indicator
SPM5	DCD	Data Carrier Detect
SPM6	DSR	Data Set Ready
SPM7	DTR	Data Terminal Ready
SPM8	SIN	Serial Receive Data
SPM9	SOUT	Serial Transmit Data

Table 5: UART signal description

The serial communication adopts an asynchronous protocol that supports various word length, stop bits and parity generation options selectable in the configuration register.

SERIAL PERIPHERAL INTERFACE

The ADuC7023 integrates a complete hardware Serial Peripheral Interface (SPI) on-chip. SPI is an industry standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex up to a maximum bit rate 23Mbs. The SPI Port can be configured for Master or Slave operation and typically consists of four pins, namely:

MISO (Master In, Slave Out Data I/O Pin)

The MISO (master in slave out) pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI (master out slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCL (Serial Clock I/O Pin)

The master serial clock (SCL) is used to synchronize the data being transmitted and received through the MOSI SCL period. Therefore, a byte is transmitted/received after eight SCL periods. The SCL pin is configured as an output in master mode

and as an input in slave mode.

In master mode polarity and phase of the clock are controlled by the SPICON1 register, and the bit-rate is defined in the SPIDIV register as follow:

$$f Serial\ Clock = f Core\ Clock/(2\ x\ (1\ +\ SPIDIV))$$

The maximum serial bit clock frequency is 1/2 of the core clock which, based on a maximum core clock frequency of 47MHz is just under 23Mbs.

In slave mode the SPICON1 register must be configured with the phase and polarity of the expected input clock.

In both master and slave modes, the data is transmitted on one edge of the SCL signal and sampled on the other. It is important therefore that the polarity and phase are configured the same for the master and slave devices.

Slave Select (SS) Input Pin

In SPI Slave Mode, a transfer is initiated by the assertion of $\overline{SS}$ which is an active low input signal. The SPI port will then transmit and receive 8-bit data until the transfer is concluded by deassertion of $\overline{SS}$. In slave mode $\overline{SS}$ is always an input. In SPI Master Mode, the $\overline{SS}$ input is not used

The following MMR registers are used to control the SPI interface: SPICON0, SPICON1, SPISTA, SPIDIV, SPITX and SPIRX

I²C Compatible Interface

The ADuC7023 supports a fully licensed* I²C interface. The I²C interface is implemented as full hardware master and/or slave interface. The two pins used for data transfer, SDA and SCL are configured in a Wired-AND format that allows arbitration in a multi-master system.

The address(es) of the I²C peripheral can be modified by the user via the I2CADD MMR.

The transfer sequence of a I²C system consists of a master device initiating a transfer by generating a START condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the master does not lose arbitration and the slave acknowledges then the data transfer is initiated. This continues until the master issues a STOP condition and the bus becomes idle.

The I²C peripheral master and slave functionality are independent and may be active simultaneously.

A slave is activated when a transfer has been initiated on the bus. If it is not being addressed it will remain inactive until another transfer is initiated. This also allows a master device

which loses arbitration to respond as a slave in the same cycle.

Serial Clock Generation

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in Fast mode (400 kHz) or Standard mode (100 kHz).

The bit-rate is defined in the I2CDIV0 and I2CDIV1 MMRs as follow:

$$f_{Serial\ Clock} = f_{Core\ Clock}/(2\ x\ (2\ +\ I2CDIV0\ +\ I2CDIV1))$$

PROGRAMMABLE LOGIC ARRAY (PLA)

The ADuC7023 integrates a fully Programmable Logic Array (PLA) which consists of two independent but interconnected PLA blocks, each block consists of eight PLA cells. A cell contains a two-input lookup table that can be configured to generate any logic output function based on two inputs, for example AND, OR, NOR, EXOR, NAND and a flip-flop.

In total, 32 GPIO pins are available as Input/Output for the PLA. These include 16 Input/Output pins, 8 input only pins and 8 output only pins. Note the comparator output is also included as one of the 16 I/O pins

The PLA is configured via a set of user MMRs and the output(s) of the PLA can be routed to the internal interrupt system, to the CONVSTART signal of the ADC, to a MMR or to any of the 24 PLA output pins.

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* Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use the ADuC702X in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 22 interrupt sources on the ADuC7023 which are controlled by the Interrupt Controller.

Most interrupts are generated from the on-chip peripherals like ADC, UART, etc. and two additional interrupt sources are generated from external interrupt request pins, XIRQ0 and XIRQ1.

The ARM7TDMI CPU core can only recognise interrupts as one of two types, namely: a normal interrupt request IRQ and a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt-related registers, four dedicated to IRQ, four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source.

Interrupt sources		
FIQ	PLL lock	Comparator
SWI	I²C Slave	PSM
RTOS timer	I²C Master	PLA IRQ0
GP timer	SPI Slave	PLA IRQ1
Wake Up timer	SPI Master	IO onto SPM4
Watchdog timer	UART	IO onto SPM5
Flash control	External IRQ0	
ADC channel	External IRQ1	

Table 6: List of the interrupt sources

TIMERS

The ADuC7023 has four general purpose Timer/Counters: -
Timer1 or RTOS Timer,
- Timer2,
- Timer3 or Wake-up Timer,
- Timer4 or Watchdog Timer.

The four timers in their normal mode of operation can be either free-running or periodic.
- In free-running mode the counter decrements/increments from the maximum/minimum value until zero/full scale and starts again at the maximum /minimum value.
- In periodic mode the counter decrements/increments from the value in the Load Register until zero/full scale and starts again at the value stored in the Load Register.

The value of a counter can be read at any time by accessing its value register. Timers are started by writing in the Control register of the corresponding timer.

In normal mode, an IRQ is generated each time the value of the counter reaches zero, if counting down, or full-scale, if counting up. An IRQ can be cleared by writing any value to Clear register of the particular timer.

Timer1 – RTOS Timer

Timer1 is a general purpose 16-bit count-down timer with a programmable prescaler. The prescaler source is the core clock frequency and can be scaled by factors of 1, 16 or 256.

Timer2

Timer2 is a 32-bit general purpose timer, count-down or count-up, with a programmable prescaler. The prescaler source can be the 32kHz Oscillator, the core clock frequency, an external GPIO or the baudrate generator. This source can be scaled by a factor of 1, 16, 256 or 32768.

The counter can be formatted as a standard 32-bit value or as Hours:Minutes:Seconds:Hundreths.

Timer2 has a capture register, which can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event with more accuracy than the precision allowed by the RTOS timer at the time the IRQ is serviced.

Timer3 - Wake-Up Timer

Timer3 is a 32-bit wake-up timer, count-down or count-up, with a programmable prescaler. It is clocked directly by the internal 32.768kHz oscillator. The wake-up timer will continue to run when the core clock is disabled. The clock source can be scaled by a factor of 1, 16, 256 or 32768.

The counter can be formatted as plain 32-bit value or as Hours:Minutes:Seconds:Hundreths.

Timer4 - Watchdog Timer

Timer4 is a 16-bit count-up/down timer with programmable prescaler. The clock source is the 32kHz Oscillator and can be scaled by a factor of 1, 16 or 256. Timer4 has two modes of operation, normal mode and watchdog mode.

In watchdog mode, timer4 decrements from the value present in T4LD Register until zero. T4LD is used as timeout. The timeout can be 512 seconds maximum, using the maximum prescaler, /256, full-scale in T4LD and 32kHz Clock.

If the timer reaches 0, a reset or an interrupt occurs, depending on the option selected in T4CON register, the control register. To avoid reset or interrupt, a write access must be written to T4CLR before the expiration period. This reloads the counter with T4LD and begins a new timeout period.

To enter Watchdog mode, bit 5 of the control register must be set. As soon as bit 5 of the control register is set, T4LD and T4CON are write-protected. These two registers can not be modified until a reset clears the watchdog enable bit and causes Timer4 to exit watchdog mode.

DEVELOPMENT TOOLS

An entry level, low cost development system is available for the ADuC702X family. This system consists of the following PC-based (Windows® compatible) hardware and software development tools:

Hardware:
- ADuC702X Evaluation board
- Serial Port programming cable
- JTAG emulator

Software:
- mIDAS Integrated Development Environment, incorporating GNU assembler, GNU compiler, Serial Downloader.
- non intrusive JTAG-based GNU debugger
- Serial Downloader software
- Example Code

Miscellaneous:
- CD-ROM Documentation

IN-CIRCUIT SERIAL DOWNLOADER

The Serial Downloader is a Windows application that allows the user to serially download an assembled program (Intel Hex format file) to the on-chip program FLASH/EE memory via the serial port on a standard PC. An Application Note (uC004) detailing this serial download protocol is available from www.analog.com/microconverter.

mIDAS IDE

The mIDAS Integrated Development Environment is a Windows application that allows the user to edit, assemble, compile and download code in the same environment.

DEBUGGER

The Debugger which can be launched from the mIDAS environment, targets the device through the JTAG port using an emulation pod included in the development system.

The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step and break-point code execution control.

ADuC7023
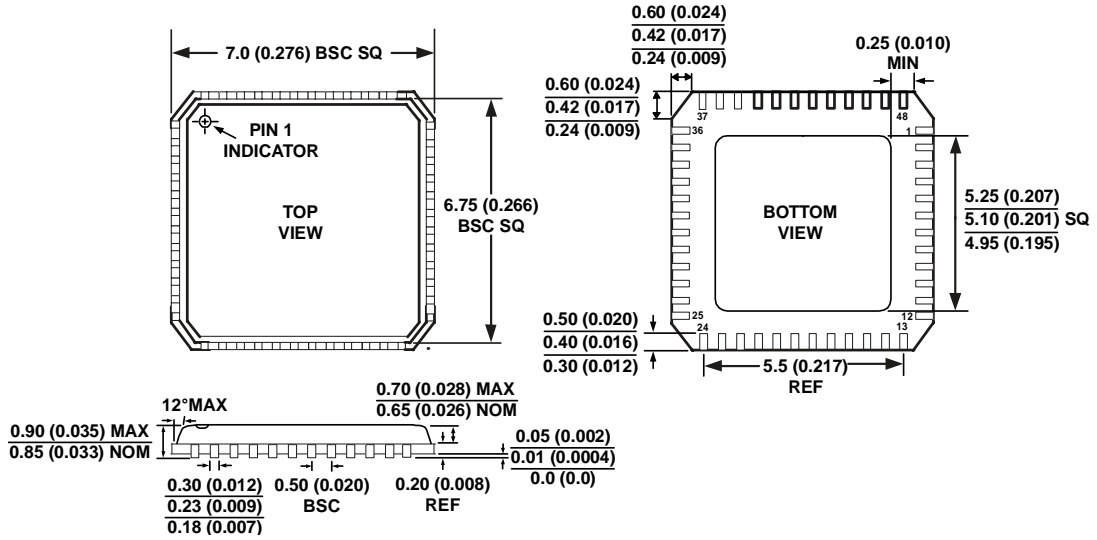
OUTLINE DIMENSIONS

Figure 10.   48-Lead Frame Chip Scale Package [LFCSP] (CP-48)—Dimensions shown in millimetres