Single-Phase Energy Measurement IC with 8052 MCU, RTC and LCD driver

Preliminary Technical Data

ADE75xx/ADE71xx

GENERAL FEATURES

Wide supply voltage operation 2.4 to 3.7V

Battery supply input with Automatic switch-over

Reference 1.2 V ± 1% (drift 50 ppm/°C Maximum)

64-Lead Quad Flat (LQFP) or Chip Scale (LCSP) Lead Free Packages[1]

Operating Temperature -40°C to 85°C

ENERGY MEASUREMENT FEATURES

High accuracy active, reactive energy measurement IC, supports IEC 62053-21, 62053-22, 62053-23

Two differential inputs with PGAs to support Shunt, Current Transformer and di/dt current sensors

Selectable Digital integrator to support di/dt current sensor

Digital parameters for Gain, offset and phase compensation

Selectable No-load threshold level for Watt, VA, and VAR anti-creep

Less than 0.1% error on active energy over a dynamic range of 1000 to 1 @ 25C

Less than 0.5% error on reactive energy over a dynamic range of 1000 to 1 @ 25C

Less than 0.5% error on rms measurements over a dynamic range of 1000 to 1 for current and 100:1 for voltage @ 25C

Auto-calibration of offsets

High frequency outputs supply proportional to Irms, active, reactive or apparent power

Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time

Temperature monitoring

[1] Please contact your Analog Devices representative to check availability of this package

MICROPROCESSOR FEATURES

8052 based core

- **Single-cycle 4MIPS 8052 core**
- **8052 compatible instruction set**
- **32.768 kHz external crystal with on-chip PLL**
- **Two external interrupt sources**
- **External reset pin**

Real Time Clock

- **Counter for seconds, minutes and hours**
- **Automatic battery switchover for RTC back up**
- **Ultra-Low Battery Supply Current < 1μA**
- **Software clock calibration with temperature and offset compensation**

Integrated LCD driver

- **104-segment with 2, 3 or 4 Multiplexer**
- **3V/5V driving capability**
- **Internally generated LCD drive voltages**
- **Temperature and Supply compensated drive voltages**

Low power battery mode

- **Wake-up from I/O and UART**
- **LCD driver capability**

On-chip peripherals

- **UART, SPI or I^2C**
- **Watch-Dog timer**
- **Power Supply Monitoring with User Selectable Levels**

Memory: 16kBytes Flash Memory, 512 Bytes RAM

Development tools

- **Single pin emulation**
- **IDE based assembly and C source debugging**

GENERAL DESCRIPTION

The ADE75xx/ADE71xx integrates Analog Devices Energy (ADE) Metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, a RTC, an LCD driver and all the peripherals to make an electronic energy meter with LCD display with a single part.

The ***ADE*** Energy Measurement core includes Active, Reactive, Apparent Energy calculations, as well as voltage and current rms measurements. This information is ready to use for energy billing by using built-in energy scalars. Many power line supervisory features like SAG, Peak, Zero-crossing are also included in the energy measurement DSP to simplify energy meter design.

The microprocessor functionality includes a single cycle 8052 core, a Real Time Clock with a power supply back-up pin, a UART, and a SPI or I^2C interface. The ready to use information from the ***ADE*** core reduces the program memory size requirement thus making it easy to integrate complicated design in 16k Bytes of Flash memory.

The ADE75xx/ADE71xx also includes a 108/104-segment LCD driver respectively. This driver generates voltages capable of driving 5V LCDs.

Rev. PrE 01/07

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FUNCTIONAL BLOCK DIAGRAM

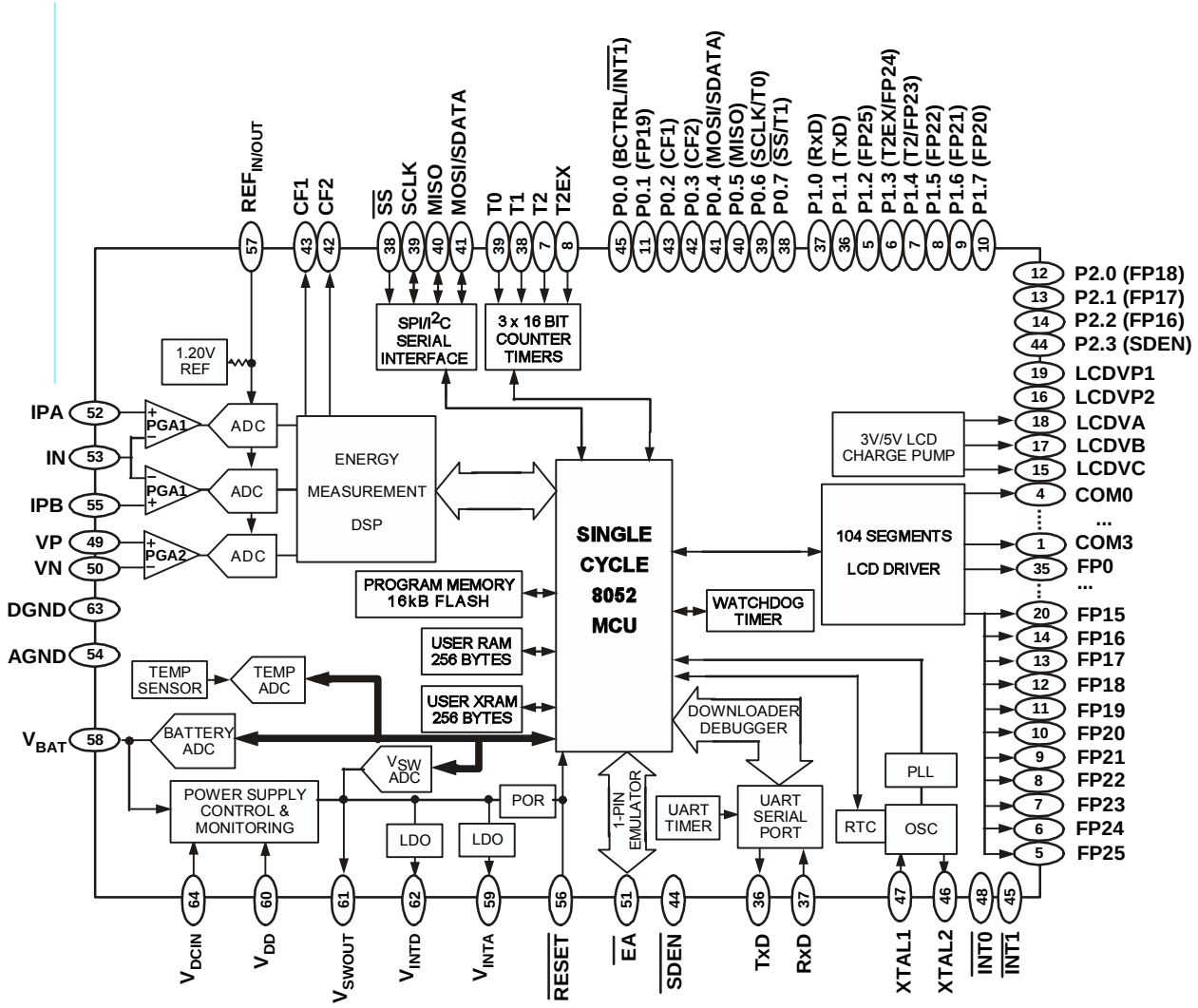


Figure 1. ADE75xx/ADE71xx Functional Block Diagram

TABLE OF CONTENT

ADE75XX/ADE71XX—SPECIFICATIONS

Table 1. (V_{DD} = 3.3 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, XTAL = 32.768kHz, T_{MIN} to T_{MAX} = −40°C to +85°C)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ENERGY METERING					
MEASUREMENT ACCURACY[1]					
Phase Error between Channels					
(PF = 0.8 Capacitive)		±0.05		°	Phase lead 37°
(PF = 0.5 Inductive)		±0.05		°	Phase lag 60°
Active Energy Measurement Error[2]		0.1		% of reading	Over a dynamic range of 1000 to 1 @25C
AC Power Supply Rejection[2]					V_{DD} = 3.3 V + 100 mV rms/120 Hz
Output Frequency Variation		0.01		%	$I_P = V_P$ = ±100 mV rms
DC Power Supply Rejection[2]					V_{DD} = 3.3 V ± 117 mV dc
Output Frequency Variation		0.01		%	$I_P = V_P$ = ±100 mV rms
Active Energy Measurement Bandwidth[1, 2]		14		kHz	
Reactive Energy Measurement Error[2]		0.5		% of reading	Over a dynamic range of 1000 to 1 @25C
VRMS Measurement Error[2]		0.5		% of reading	Over a dynamic range of 100 to 1 @25C
VRMS Measurement Bandwidth[1, 2]		14		kHz	
IRMS Measurement Error[2]		0.5		% of reading	Over a dynamic range of 1000 to 1 @25C
IRMS Measurement Bandwidth[1, 2]		14		kHz	
ANALOG INPUTS					$V_P - V_N$, $I_A - I_N$ and $I_B - I_N$
Maximum Signal Levels			±500	mV peak	Differential input
Input Impedance (DC)	TBD			kΩ	
Bandwidth (−3 dB)[1]		14		kHz	
ADC Offset Error[2]			1	mV	
Gain Error[2]					
Current channel					
Range = 0.5 V Full scale		±4		%	Current channel = 0.5V dc
Range = 0.25 V Full scale		±4		%	Current channel = 0.25V dc
Range = 0.125 V Full scale		±4		%	Current channel = 0.125V dc
Voltage channel		±4		%	Voltage channel = 0.5V dc
Gain Error Match[2]		±3		%	
CF1 and CF2 pulse output					
Maximum output frequency		21.1		kHz	V_P-V_N = I_{AP}-I_N=500mV peak sine wave
Duty cycle		50		%	If CF1 or CF2 frequency > 5.55Hz
Active High pulse width		90		ms	If CF1 or CF2 frequency < 5.55Hz
FAULT Detection					
Fault Detection Threshold					
Inactive Input <> Active Input		6.25		%, of larger	I_A or I_B active
Input Swap Threshold					
Inactive Input <> Active Input		6.25		% of larger	I_A or I_B active
Accuracy Fault Mode Operation					
I_A Active, I_B = AGND		0.1		% of reading	Over a dynamic range of 500 to 1
I_B Active, I_A = AGND		0.1		% of reading	Over a dynamic range of 500 to 1
Fault Detection Delay		3		Seconds	
Swap Delay		3		Seconds	
ANALOG PERIPHERALS					

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Internal ADCs (Battery, Temperature, V_{DD})					
Power supply operating range	2.2		3.7	V	Measured on V_{SWOUT}
No missing codes[1]	8			bits	
AC Power Supply Rejection		TBD		dB	
DC Power Supply Rejection		TBD		dB	
Integral Linearity Error	-1		1	LSB[3]	
Differential Linearity Error	-1		1	LSB	
Conversion Delay[4]		1		ms	
Temperature sensor accuracy	-1		1	°C	at 25°C
	-4		4	°C	between -40°C and 85°C
V_{DCIN} ANALOG INPUT					
Maximum Signal Levels	0		V_{SWOUT}	V	
Input Impedance (DC)		1		MΩ	
Low V_{DCIN} detection threshold	1.08	1.2	1.32	V	
Power-On Reset (POR)					
V_{DD} POR					
Voltage operating range	1		3.7	V	
Detection threshold	1.6		2.9	V	
POR active Time-out period		TBD		ms	
Strobe period in Battery operation		TBD		Ms	
V_{SWOUT} POR					
Voltage operating range (V_{SWOUT})	1		3.7	V	
Detection threshold	1.8		2.2	V	
POR active Time-out period		TBD		ms	
V_{INTA} and V_{INTD} POR					
Voltage operating range (V_{SWOUT})	1		3.7	V	
Detection threshold	2.25		2.4	V	
POR active Time-out period		TBD		ms	
BATTERY SWITCH OVER					
Voltage operating range (V_{SWOUT})	2.4		3.7	V	
V_{DD} ➔ V_{BAT} switching threshold (V_{SWOUT})	2.75		TBD	V	
V_{DD} ➔ V_{BAT} switching delay		TBD		ms	
V_{BAT} ➔ V_{DD} switching threshold (V_{DD})	2.75		TBD	V	
V_{BAT} ➔ V_{DD} switching delay		TBD		ms	
V_{SWOUT} to V_{BAT} leakage current			1	nA	
LCD – Charge pump active					
LCDVP1 – LCDVP2 charge pump capacitance	200			nF	
LCDVA, LCDVB, LCDVC decoupling capacitance	470			nF	
LCDVA	0		1.7	V	
LCDVB	0		4.0	V	1/2 bias modes
LCDVB	0		3.4	V	1/3 bias modes
LCDVC	0		5.1	V	1/3 bias mode
LCD stand-by current		100		nA	1/2 and 1/3 bias modes
V1 Segment line voltage	LCDVA-0.1	LCDVA		V	Current on segment line = -2µA
V2 Segment line voltage	LCDVB-0.1	LCDVB		V	Current on segment line = -2µA
V3 Segment line voltage	LCDVC-0.1	LCDVC		V	Current on segment line = -2µA
DC voltage across Segment and COM pin		50		mV	LCDVC-LCDVB, LCDVC-LCDVA or LCDVB-LCDVA
LCD – Resistor ladder active					

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Leakage current			±20	nA	1/2 and 1/3 bias modes – No load
V1 Segment line voltage	LCDVA-0.1V		LCDVA	V	Current on segment line = -2μA
V2 Segment line voltage	LCDVB-0.1V		LCDVB	V	Current on segment line = -2μA
V3 Segment line voltage	LCDVC-0.1V		LCDVC	V	Current on segment line = -2μA
ON-CHIP REFERENCE					
Reference Error			±12	mV	
Power supply rejection		80		dB	
Temperature Coefficient			50	ppm/°C	
DIGITAL INTERFACE					
LOGIC INPUTS					
All inputs except XTAL1, XTAL2, BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.4	V	
BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$					
Input High Voltage, V_{INH}	1.3			V	
Input Low Voltage, V_{INL}			0.4	V	
Input currents					
$\overline{RESET}$			±10	μA	$\overline{RESET}$ = 0V
			100	μA	$\overline{RESET}$ = V_{SWOUT} = 3.3V
Port 0, 1 , 2			±10	μA	Internal pull-up disabled, input – 0V or V_{OUT}
			-250	μA	Internal pull-up enabled, input = 2V, V_{SWOUT}=3.3V
			-50	μA	Internal pull-up enabled, input = 0.4V, V_{SWOUT}=3.3V
Input capacitance		10		pF	All digital input
CRYSTAL OSCILLATOR					
Crystal Equivalent Series Resistance	30		50	kΩ	
Crystal frequency	32	32.768	33.5	kHz	
XTAL1 Input Capacitance		12		pF	
XTAL2 Output Capacitance		12		pF	
MCU CLOCK RATE - F_{core}		4.096		MHz	Crystal = 32.768kHz and CD[2:0]=0
		32		kHz	Crystal = 32.768kHz and CD[2:0]=0b111
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	V_{DD} = 3.3 V ± 5%
I_{SOURCE}			80	μA	
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 3.3 V ± 5%
I_{SINK}			2	mA	
Floating state Leakage current			±10	μA	
Floating state Output Capacitance		TBD		pF	
STARTUP TIME[5]					
At Power-On		TBD		ms	
From Power Saving Mode 2 (PSM2)		TBD		μs	
From Power Saving Mode 1 (PSM1)		TBD		μs	
POWER SUPPLY INPUTS					
V_{DD}	3.0	3.3	3.6	V	
V_{BAT}	2.4	3.3	3.7	V	
POWER SUPPLY OUTPUTS					
V_{BAT} to V_{SWOUT} ON-Resistance			25	Ω	V_{BAT} = 2.4V
V_{DD} to V_{SWOUT} ON-Resistance			6.1	Ω	V_{DD} = 3V
V_{SWOUT} output current drive			1	mA	
V_{INTA}, V_{INTD}	2.25		2.75	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{INTA} power supply rejection		80		dB	
V_{INTD} power supply rejection		60		dB	
POWER SUPPLY CURRENTS					
Current in **Normal** Mode (PSM0)		3.5		mA	F_{core} = 4.096 MHz
Current in **Normal** Mode (PSM0)		2.1		mA	F_{core} = 1.024 MHz
Current in PSM1 with V_{INTA} disabled		880		µA	F_{core} = 1.024 MHz
Current in PSM2		1.5		µA	

[1] These numbers are not production tested but are guaranteed by design and/or characterization data on production release
[2] See Terminology section for explanation of specifications.
[3] LSB means Least Significant Bit
[4] Delay between ADC conversion request and interrupt set
[5] Delay between power supply valid and execution of first instruction by 8052 core

TIMING SPECIFICATIONS

AC inputs during testing are driven at V_{SWOUT} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 2.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 2.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

V_{DD} = 2.7 V to 3.6 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	TBD	TBD	4.096	MHz

[1] ADE75xx/ADE71xx internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.

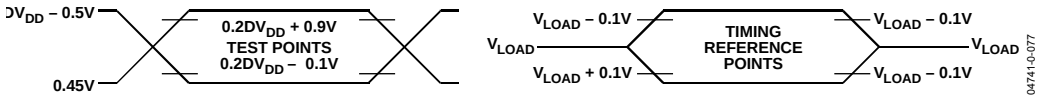


Figure 2. Timing Waveform Characteristics

Table 3. I²C COMPATIBLE INTERFACE TIMING Parameter

Parameter		Min	Max	Unit
t_L	SCLOCK Low Pulse Width	1.95		µs
t_H	SCLOCK High Pulse Width	1.95		µs
t_{SHD}	Start Condition Hold Time	TBD		µs
t_{DSU}	Data Setup Time	TBD		µs
t_{DHD}	Data Hold Time		TBD	µs
t_{RSU}	Setup Time for Repeated Start	TBD		µs
t_{PSU}	Stop Condition Setup Time	TBD		µs
t_{BUF}	Bus Free Time between a Stop Condition and a Start Condition	TBD		µs
t_R	Rise Time of Both SCLOCK and SDATA		300	ns
t_F	Fall Time of Both SCLOCK and SDATA		300	ns
t_{SUP}[1]	Pulse Width of Spike Suppressed		50	ns

[1] Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

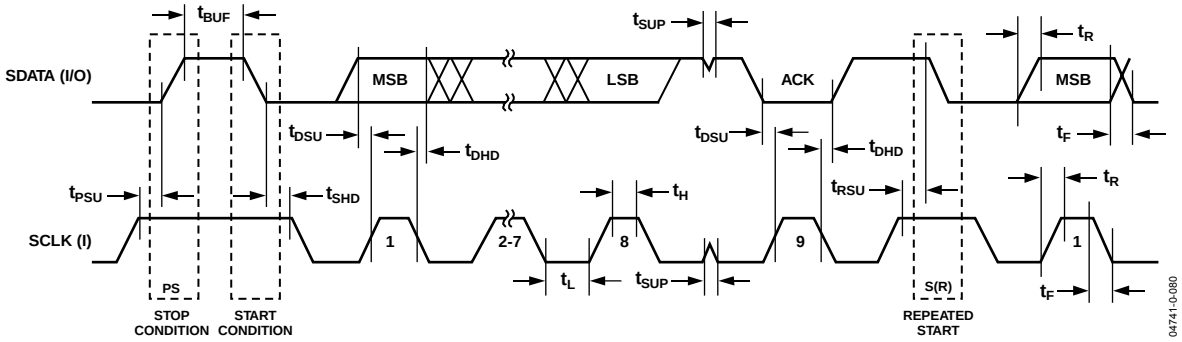


Figure 3. I²C Compatible Interface Timing

Table 4. SPI MASTER MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]	977			ns
t_{SH}	SCLOCK High Pulse Width[1]	977			ns
t_{DAV}	Data Output Valid after SCLOCK Edge			TBD	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	TBD			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	TBD			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in POWCON SFR set to 0, 0, and 0, respectively, that is, core clock frequency = 4.096/8 MHz.
b. SPI bit-rate selection bits SPIR1 and SPR0 in SPI2CMOD SFR set to 0 and 0, respectively.

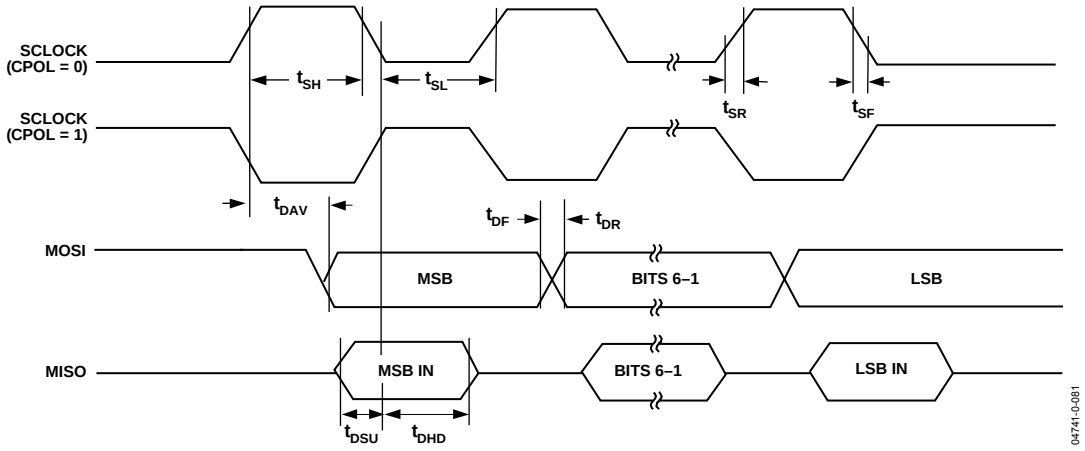


Figure 4. SPI Master Mode Timing (CPHA = 1)

Table 5. SPI MASTER MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]	977			ns
t_{SH}	SCLOCK High Pulse Width[1]	977			ns
t_{DAV}	Data Output Valid after SCLOCK Edge			TBD	ns
t_{DOSU}	Data Output Setup before SCLOCK Edge			TBD	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	TBD			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	TBD			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in POWCON SFR set to 0, 0, and 0, respectively, that is, core clock frequency = 4.096/8 MHz.
b. SPI bit-rate selection bits SPIR1 and SPR0 in SPI2CMOD SFR set to 0 and 0, respectively.

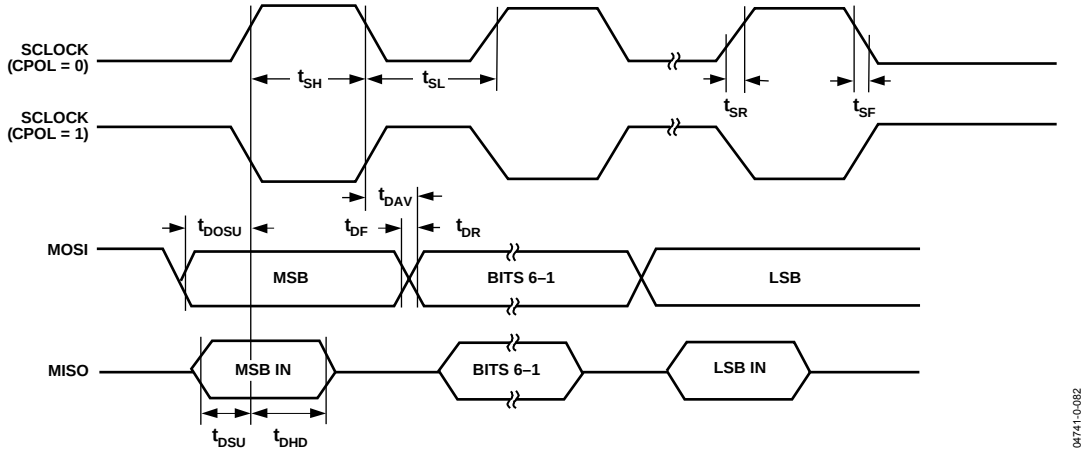


Figure 5. SPI Master Mode Timing (CPHA = 0)

Table 6. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width	977			ns
t_{SH}	SCLOCK High Pulse Width	977			ns
t_{DAV}	Data Output Valid after SCLOCK Edge			TBD	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	TBD			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	TBD			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{DIS}	MISO disable after $\overline{SS}$ rising edge	TBD			ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

1

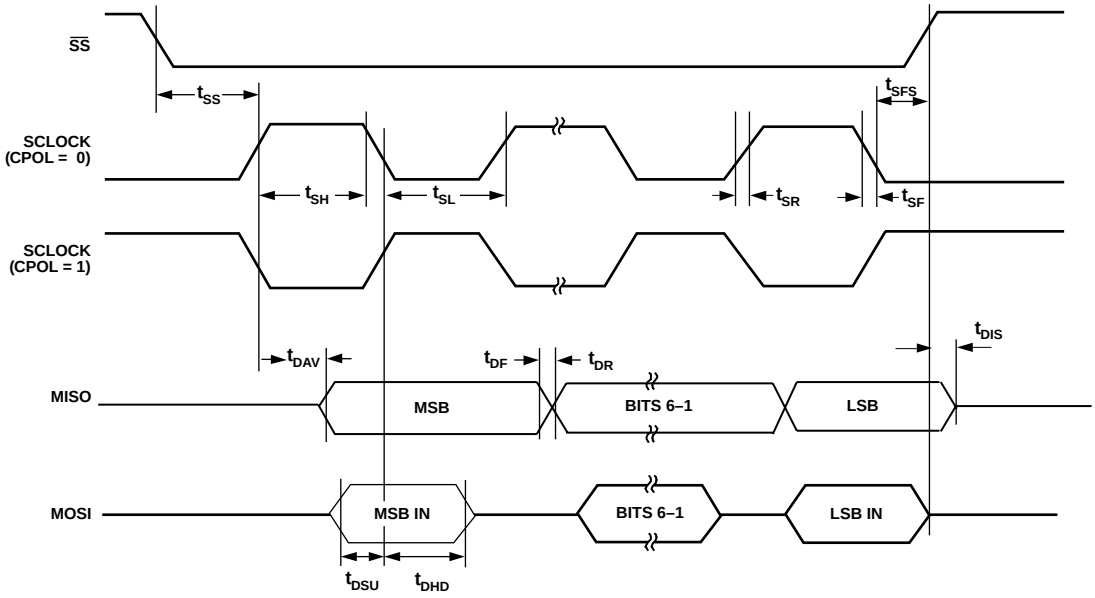


Figure 6. SPI Slave Mode Timing (CPHA = 1)

Table 7. SPI SLAVE MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width	977			ns
t_{SH}	SCLOCK High Pulse Width	977			ns
t_{DAV}	Data Output Valid after SCLOCK Edge			TBD	ns
t_{DSU}	Data Input Setup Time before SCLOCK Edge	TBD			ns
t_{DHD}	Data Input Hold Time after SCLOCK Edge	TBD			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{DOSS}	Data Output Valid after $\overline{SS}$ Edge			20	ns
t_{DIS}	MISO disable after $\overline{SS}$ rising edge	TBD			ns
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns

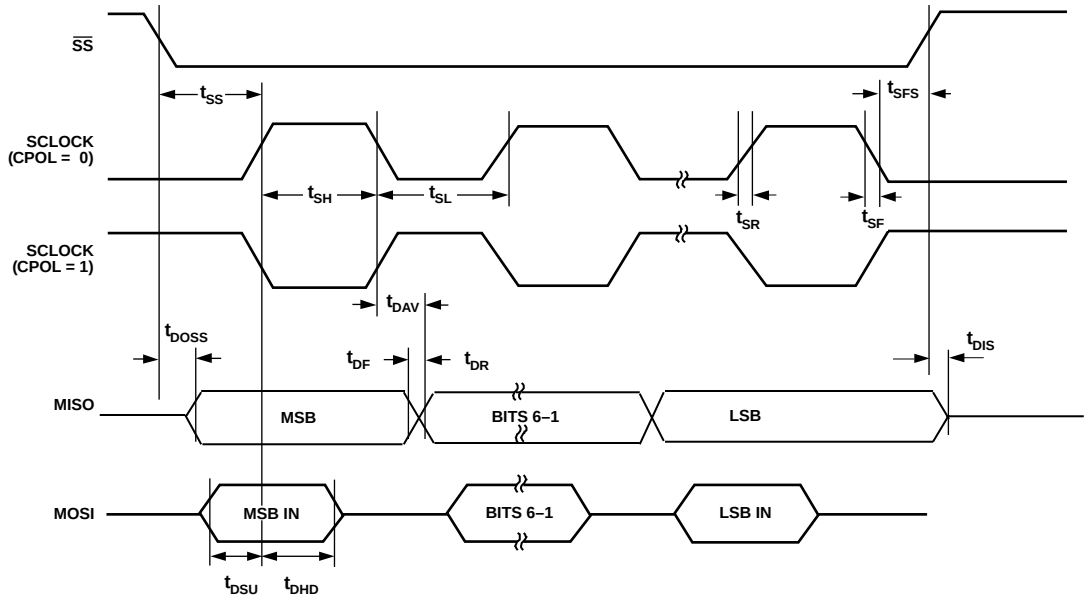


Figure 7. SPI Slave Mode Timing (CPHA = 0)

Table 8. UART Timing (Shift Register Mode) Parameter

		4.09612.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		2.93			$12t_{core}$		µs
TQVXH	Output Data Setup to Clock	TBD						µs
TDVXH	Input Data Setup to Clock	TBD						µs
TXHDX	Input Data Hold after Clock	TBD						µs
TXHQX	Output Data Hold after Clock	TBD						µs

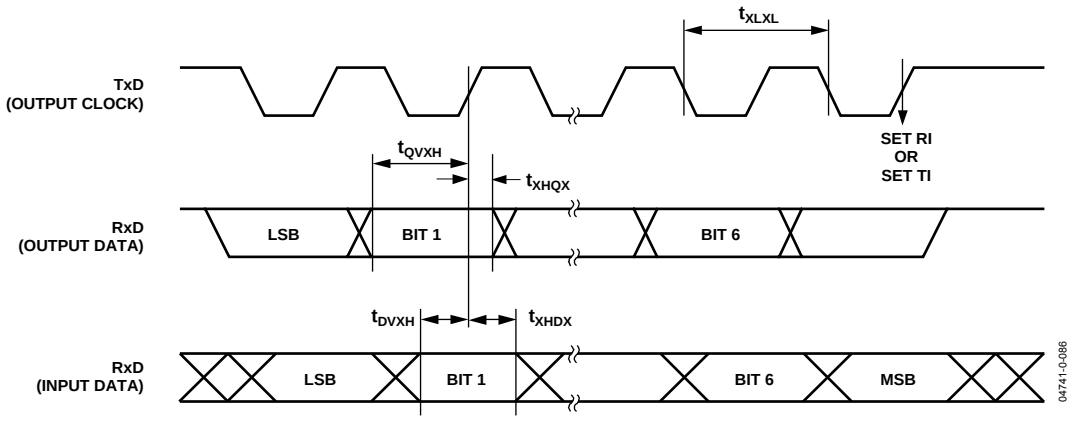
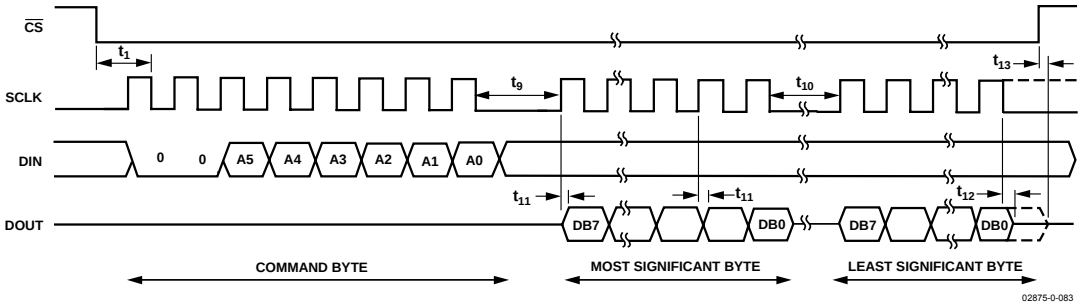


Figure 8. UART Timing in Shift Register Mode



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 9. Absolute Maximum Rating

Parameter	Rating
V_{DD} to DGND	–0.3 V to +3.7 V
V_{BAT} to DGND	–0.3 V to +3.7 V
V_{DCIN} to DGND	–0.3 V to V_{SWOUT} + 0.3 V
Input LCD voltage to AGND	–0.3 V to V_{SWOUT} + 0.3 V
LCDVA, LCDVB, LCDVC[2]	
Analog Input Voltage to AGND	–2 V to +2 V
V_P, V_N, I_{AP}, I_{BPN} and I_N	
Digital Input Voltage to DGND	–0.3 V to V_{SWOUT} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to V_{SWOUT} + 0.3 V
Operating Temperature Range	
Industrial	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	TBD°C
64-Lead LQFP, Power Dissipation	TBD
θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (TBD sec)	TBD°C
Infrared (TBD sec)	TBD°C
64-Lead CSP, Power Dissipation	TBD
θJA Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (TBD sec)	TBD°C
Infrared (TBD sec)	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] When used with external resistor divider

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE75xx/ADE71xx is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ \text{Re}gister - True\ Energy}{True\ Energy} \right) \times 100\%$$

PHASE ERROR BETWEEN CHANNELS

The digital integrator and the high-pass filter (HPF) in the current channel have a non-ideal phase response. To offset this phase response and equalize the phase response between channels, two phase-correction networks are placed in the current channel: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding component and ensure a phase match between current channel and voltage channel to within ±0.1° over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within ±0.4°
over a range of 45 Hz to 65 Hz.

POWER SUPPLY REJECTION

This quantifies the ADE75xx/ADE71xx measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac (100 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of the reading.

ADC OFFSET ERROR

The dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection—see the Typical Performance Characteristics section. However, when HPF1 is switched on, the offset is removed from the current channel and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration—see the Analog Inputs section.

GAIN ERROR

The difference between the measured ADC output code (minus the offset) and the ideal output code—see the Current Channel ADC and Voltage Channel ADC sections. It is measured for each of the input ranges on the current channel (0.5 V, 0.25 V, and 0.125 V). The difference is expressed as a percentage of the ideal code.

PIN DESCRIPTIONS

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COM3/ FP27	Common output, COM3 is used for LCD backplane / LCD segment outputs 27
2	COM2/ FP28	Common output, COM2 is used for LCD backplane / LCD segment outputs 28
3	COM1	Common output, COM1 is used for LCD backplanes
4	COM0	Common output, COM0 is used for LCD backplanes
5	P1.2/FP25	General-purpose digital I/O / LCD segment outputs 25
6	P1.3/T2EX/FP24	General-purpose digital I/O / Timer 2 control input / LCD segment outputs 24
7	P1.4/T2/FP23	General-purpose digital I/O / Timer 2 input / LCD segment outputs 23
8	P1.5/FP22	General-purpose digital I/O / LCD segment outputs 22
9	P1.6/FP21	General-purpose digital I/O / LCD segment outputs 21
10	P1.7/FP20	General-purpose digital I/O / LCD segment outputs 20
11	P0.1/FP19	General-purpose digital I/O / LCD segment outputs 19
12	P2.0/FP18	General-purpose digital I/O / LCD segment outputs 18
13	P2.1/FP17	General-purpose digital I/O / LCD segment outputs 17
14	P2.2/FP16	General-purpose digital I/O / LCD segment outputs 16
15	LCDVC	Output port for LCD levels. This pin should be decoupled with a 470nF capacitor.
16	LCDVP2	This pin is an analog output. A capacitor of 470nF should be connected between this pin and LCDVP1 for internal LCD charge pump device.
17, 18	LCDVB, LCDVA	Output ports for LCD levels. These pins should be decoupled with a 470nF capacitor.
19	LCDVP1	This pin is an analog output. A capacitor of 470nF should be connected between this pin and LCDVP2for internal LCD charge pump device.
35-20	FP0-15	LCD segment outputs 0-15
36	P1.1/TxD	General-purpose digital I/O / Transmitter Data Output 1 (Asynchronous)
37	P1.0/RxD	General-purpose digital I/O / Receiver Data Input 1 (Asynchronous)
38	P0.7 /$\overline{SS}$/T1	General-purpose digital I/O / Slave select when SPI is in Slave mode / Timer 1 input
39	P0.6/SCLK/T0	General-purpose digital I/O / Clock output for I^2C or SPI port / Timer 0 input
40	P0.5/MISO	General-purpose digital I/O / Data In for SPI port
41	P0.4/MOSI/SDATA	General-purpose digital I/O / Data Line I^2C compatible or Data Out for SPI port
42	P0.3/CF2	General-purpose digital I/O / Calibration Frequency Logic Output. The CF2 logic output gives instantaneous active, reactive or apparent power information.
43	P0.2/CF1/RTCCAL	General-purpose digital I/O / Calibration Frequency Logic Output/ RTC calibration output.. The CF1 logic output gives instantaneous active, reactive or apparent power information. The RTCCAL output provides a way to calibrate the RTC to within ±2ppm, or 0.17s/day –see the RTC Calibration section.
44	$\overline{SDEN}$/P2.3	This pin is used to enable serial download mode when pulled low through a resistor on power-up or reset. On reset this pin will momentarily become an input and the status of the pin is sampled. If there is no pulldown resistor in place, the pin will go momentarilly high and then user code will execute. If a pull-down resistor is in place, the embedded serial download/debug kernel will execute and this pin remains low during internal program execution. This pin can also be used as a general purpose output.
45	BCTRL/$\overline{INT1}$/ P0.0	Digital Input for Battery control. This logic input connects V_{DD} or V_{BAT} to V_{SW} internally when set to logic High or Low respectively. When left open, the connection between V_{DD} or V_{BAT} to V_{SW} is selected internally / External Interrupt input / General-purpose digital I/O
46	XTAL2	A crystal can be connected across this pin andXTAL1 as described above to provide a clock source for the ADE75xx/ADE71xx.The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit.
47	XTAL1	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE75xx/ADE71xx.The clock frequency for specified operation is 32.768 kHz.
48	$\overline{INT0}$	General-purpose digital I/O / Interrupt input

Pin No.	Mnemonic	Description
49, 50	V_P, V_N	Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500mV for specified operation. This channel also has an internal PGA.
51	$\overline{EA}$	This pin is used as an input for emulation. When held high, this input enables the device to fetch code from internal program memory locations.The ADE75xx/ADE71xx does not support external code memory. This pin should not be left floating.
52, 53	I_P, I_N	Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500mV for specified operation. This channel also has an internal PGA.
54	AGND	This pin provides the ground reference for the analog circuitry
55	I_{PB}	Analog Inputs for second Current Channel. This input is fully differential with a maximum differential level of ±500mVrefered to I_N for specified operation. This channel also has an internal PGA.
56	$\overline{RESET}$	Reset input, Active low
57	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 8% and a typical temperature coefficient of 50 ppm/°C maximum
58	V_{BAT}	3.3V Power supply input from Battery. This pin is connected internally to V_{DD} when the Battery is selected as the power supply for the ADE75xx/ADE71xx.
59	V_{INTA}	This pin provides access to the on-chip 2.5V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
60	V_{DD}	3.3V Power supply input from regulator. This pin is connected internally to V_{DD} when the regulator is selected as the power supply for the ADE75xx/ADE71xx. This pin should be decoupled with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
61	V_{SWOUT}	3.3V Power supply output from ADE75xx/ADE71xx. This pin provides the supply voltage for the LDOs and internal cicuitry of the ADE75xx/ADE71xx. This pin should be decoupled with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
62	V_{INTD}	This pin provides access to the on-chip 2.5V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10μF capacitor in parallel with a ceramic 100nF capacitor.
63	DGND	This pin provides the ground reference for the digital circuitry
64	V_{DCIN}	Analog input for dc voltage monitoring. The maximum input voltage on this pin is xxxmV with respect to AGND. This pin is used to monitor the pre-regulated dc voltage. A dedicated ADC measures the voltage on this pin—see the External Voltage Measurement section.

SFR MAPPING

IPSMF xF8 Table 13	**STRBPER** xF9 Table 46	**BATVTH** xFA Table 49	**SCRATCH1** xFB Table 17	**SCRATCH2** xFC Table 18	**SCRATCH3** xFD Table 19	**SCRATCH4** xFE Table 20	**INTPR** xFF Table 12
B xF0			**DIFFPROG** xF3 Table 47	**PERIPH** xF4 Table 15	**BATPR** xF5 Table 14	**RTCCOMP** xF6 Table 116	**TEMPCAL** xF7 Table 117
SPIMOD1 **I2CMOD** xE8 Table 130 Table **135**	**SPIMOD2** **I2CADR** xE9 Table **131** Table 136	**SPISTAT** **I2CSTAT** xEA Table 132 Table 137		**IPSME** xEC Table 16	**LCDSEGE2** xED Table 84		**VDCINADC** xEF Table 50
xE8 Table 130 Table **135**	xE9 Table **131** Table 136	xEA Table 132		xEC Table 16	xED Table 84		xEF Table 50
ACC xE0		**WAV1L** xE2 Table 27	**WAV1M** xE3 Table 27	**WAV1H** xE4 Table 27	**WAV2L** xE5 Table 27	**WAV2M** xE6 Table 27	**WAV2H** xE7 Table 27
ADCGO xD8 48	**MIRQENL** xD9 Table 39	**MIRQENM** xDA Table **40**	**MIRQENH** xDB Table 41	**MIRQSTL** xDC Table 36	**MIRQSTM** xDD Table **37**	**MIRQSTH** xDE Table 38	**BATADC** xDF Table 51
PSW xD0 Table 54	**VRMSL** xD1 Table 27	**VRMSM** xD2 Table 27	**VRMSH** xD3 Table 27	**IRMSL** xD4 Table 27	**IRMSM** xD5 Table 27	**IRMSH** xD6 Table 27	**TEMPADC** xD7 Table 52
T2CON xC8 Table 99		**RCAP2L** xCA Table 107	**RCAP2H** xCB Table 106	**TL2** xCC Table 105	**TH2** xCD Table 104		
WDCON xC0 Table 71	**KYREG** xC1 Table 109				**POWCON** xC5 Table 22	**EADRL** xC6 Table 94	**EADRH** xC7 Table 95
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	LCDCONY xB1 Table 77	**PINMAP0** xB2 Table **141**	**PINMAP1** xB3 Table **142**	**PINMAP2** xB4 Table **143**			
IE xA8 Table 63	**IEIP2** xA9 Table 65			**LCDPTR** xAC Table 82		**LCDDAT** xAE Table 83	**CFG** xAF Table 59
P2 xA0 Table **146**	**TIMECON** xA1 Table 110	**HTHSEC** xA2 Table 111	**SEC** xA3 Table 112	**MIN** xA4 Table 113	**HOUR** xA5 Table 114	**INTVAL** xA6 Table 115	**DPCON** xA7 Table 138
SCON x98 Table 122	**SBUF** x99 Table 123	**SPI2CTx** x9A Table 128	**SPI2CRx** x9B Table 129	**LCDCONX** x9C Table 75	**SBAUDF** x9D Table 125	**SBAUDT** x9E Table 124	**EPCFG** x9F Table **140**
P1 x90 Table **145**	**MADDPT** x91 Table 27	**MDATL** x92 Table 27	**MDATM** x93 Table 27	**MDATH** x94 Table 27	**LCDCON** x95 Table 74	**LCDCLK** x96 Table 78	**LCDSEGE** x97 Table 81
TCON x88 Table 98	**TMOD** x89 Table 97	**TL0** x8A Table 101	**TL1** x8B Table 103	**TH0** x8C Table 100	**TH1** x8D Table 102		
P0 x80 Table **144**	**SP** x81 Table 58	**DPL** x82 Table 56	**DPH** x83 Table 57				**PCON** x87 Table 55

MAPKEY

Mnemonic

WDCON
xC0 Table 71

Address Link to detailed table

POWER MANAGEMENT

The ADE75XX/ADE71XX has an elaborate power management circuitry that manages the regular power supply to Battery switch over and power supply failures. The power management functionalities can be accessed directly through the 8052 SFR – see Table 11.

Table 11. Power Management SFRs

SFR address (hex)	R/W	Name	Description
0xC1	R/W	KYREG	Key Register
0xC5	R/W	POWCON	Power Management Configuration
0xEC	R/W	IPSME	Power Management Interrupt enable
0xF4	R/W	PERIPH	Power Management Configuration
0xF5	R/W	BATPR	Battery Switchover configuration
0xF8	R/W	IPSMF	Power Management Interrupt Flag
0xFB	R/W	SCRATCH1	Scratch pad register
0xFC	R/W	SCRATCH2	Scratch pad register
0xFD	R/W	SCRATCH3	Scratch pad register
0xFE	R/W	SCRATCH4	Scratch pad register
0xFF	R/W	INTPR	Interrupt Wake-up Configuration

POWER MANAGEMENT REGISTER DETAILS

Table 12. Interrupt pins configuration SFR (INTPR, 0xFF)

Bit Location	Bit Mnemonic	Default Value	Description
7	RTCCAL	0	Control RTC calibration output When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.
6-5	FSEL[1:0]		Sets RTC calibration output frequency and calibration window
			FSEL[1:0] — Calibration window, frequency
			0 0 — 30.5 seconds, 1Hz
			0 1 — 30.5 seconds, 512 Hz
			1 0 — 0.244 seconds, 500Hz
			1 1 — 0.244 seconds, 16.384 kHz
4	Reserved		
3-1	INT1PRG[2:0]	000	Controls the function of $\overline{\text{INT1T}}$
			INT1PRG[2:0] — Function
			x 0 0 — GPIO
			x 0 1 — BCTRL
			0 1 x — $\overline{\text{INT1}}$ input disabled
			1 1 x — $\overline{\text{INT1}}$ input enabled

0	INT0PRG	0	Controls the function of $\overline{\text{INT0}}$	
			INT0PRG	Function
			0	$\overline{\text{INT0}}$ input disabled
			1	$\overline{\text{INT0}}$ input enabled

Table 13. Power Management Interrupt Flag SFR (IPSMF, 0xF8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0xFF	FPSR	0	Power Supply Restored Interrupt flag. Set when the V_{DD} power supply has been restored. This occurs when the source of V_{SW} changes from V_{BAT} to V_{DD}.
6	0xFE	FPSM	0	PSM Interrupt flag. Set when an enabled PSM interrupt condition occurs.
5	0xFD	FSAG	0	Voltage SAG Interrupt flag. Set when an ADE energy measurement SAG condition occurs.
4	0xFC	RESERVED	0	This bit must be kept cleared for proper operation
3	0xFB	FVADC	0	V_{DCIN} ADC interrupt flag. Set when V_{DCIN} changes by VDCINDIF or when a V_{DCIN} measurement is ready.
2	0xFA	FBAT	0	V_{BAT} Monitor interrupt flag. Set when V_{BAT} falls below BATVTH or when the V_{BAT} measurement is ready.
1	0xF9	FBSO	0	Battery Switchover interrupt flag. Set when V_{SW} switches from V_{DD} to $V_{BAT.}$
0	0xF8	FVDC	0	V_{DCIN} Monitor interrupt flag. Set when V_{DCIN} falls below 1.2V.

Table 14. Battery Switchover Configuration SFR (BATPR, 0xF5)

Bit Location	Bit Mnemonic	Default Value	Description	
7-2	Reserved	00	These bits must be kept to 0 for proper operation	
1-0	BATPRG [1:0]	00	Control bits for Battery Switchover.	
			BATPRG [1:0]	Function
			0 0	Battery Swichover Enabled on Low V_{DD}
			0 1	Battery Swichover Enabled on Low V_{DD} and Low V_{DCIN}
			1 X	Battery Switchover Disabled

Table 15. Peripheral Configuration SFR (PERIPH, 0xF4)

Bit Location	Bit Mnemonic	Default Value	Description	
7	RXFLAG	0	If set, indicates that a RX Edge event triggered wakeup from PSM2	
6	VSWSOURCE	1	Indicates the power supply that is connected internally to V_{SW}. 0 V_{SW}=V_{BAT} 1 V_{SW}=V_{DD}	
5	VDD_OK	1	If set, indicates that VDD power supply is ok for operation	
4	PLL_FLT	0	If set, indicates that a PLL fault occurred where the PLL lost lock. Set the PLL_FLT_ACK bit in the Start ADC Measurement SFR (ADCGO, 0xD8) SFR to acknowledge the fault and clear the PLL_FLT bit	
3	REF_BAT_EN	0	If set, Internal voltage reference enabled in PSM2 mode. This bit should be set to maintain the LCD in PSM2 mode.	
2	Reserved	0	This bit should be kept to zero	
1-0	RXPROG[1:0]	00	Controls the function of the P1.0/RX pin.	
			RXPROG [1:0]	Function
			0 0	GPIO

			0	1	RX with wakeup disabled
			1	1	RX with wakeup enabled

Table 16. Power Management Interrupt Enable SFR (IPSME, 0xEC)

Bit Location	Bit Mnemonic	Default Value	Description
7	EPSR	0	Enables a PSM interrupt when the Power Supply Restored flag is set.
6	RESERVED	0	Reserved
5	ESAG	0	Enables a PSM interrupt when the voltage sag flag (FSAG) is set.
4	RESERVED	0	This bit must be kept cleared for proper operation
3	EVADC	0	Enables a PSM interrupt when the V_{DCIN} ADC flag (FVADC) is set.
2	EBAT	0	Enables a PSM interrupt when the V_{BAT} monitor flag (FBAT) is set.
1	EBSO	0	Enables a PSM interrupt when the Battery Switchover flag (FBSO) is set.
0	EVDCIN	0	Enables a PSM interrupt when the V_{DCIN} monitor flag (FVDCIN) is set.

Table 17. Scratch Pad 1 SFR (SCRATCH1, 0xFB)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SCRATCH1	0	Value can be written/read in this register. This value will be maintained in all the power saving modes of the ADE75xx/ADE71xx

Table 18. Scratch Pad 2 SFR (SCRATCH2, 0xFC)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SCRATCH2	0	Value can be written/read in this register. This value will be maintained in all the power saving modes of the ADE75xx/ADE71xx

Table 19. Scratch Pad 3 SFR (SCRATCH3, 0xFD)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SCRATCH3	0	Value can be written/read in this register. This value will be maintained in all the power saving modes of the ADE75xx/ADE71xx

Table 20. Scratch Pad 4 SFR (SCRATCH4, 0xFE)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SCRATCH4	0	Value can be written/read in this register. This value will be maintained in all the power saving modes of the ADE75xx/ADE71xx

Table 21. Key SFR (KYREG, 0xC1)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	KYREG	0	Write 0xA7 to the KYREG SFR before writing the POWCON SFR, to unlock it Write 0xEA to the KYREG SFR before writing to the HTHSEC, SEC, MIN, or HOUR timekeeping register to unlock it..

Table 22. Power Control SFR (POWCON, 0xC5)

Bit Location	Bit Mnemonic	Default Value	Description
7	RESERVED	X	

6	METER_OFF	0	Set this bit to turn off the modulators and energy metering DSP circuitry to reduce power if metering functions are not needed in PSM0			
5	RESERVED	0				
4	COREOFF	0	Set this bit to shut down the core if in the PSM1 operating mode.			
3	RESERVED					
2-0	CD[2:0]	010	Controls the core clock frequency, F_{core}. F_{core}=4.096MHz/2^{CD}			
			CD[2:0]			F_{core} (MHz)
			0	0	0	4.096
			0	0	1	2.048
			0	1	0	1.024
			0	1	1	0.512
			1	0	0	0.256
			1	0	1	0.128
			1	1	0	0.064
			1	1	1	0.032

Note: The POWCON register must be unlocked by first writing to the KYREG key register. The KYREG SFR is set to 0xA7 to unlock the POWCON SFR and then the POWCON SFR can be modified. For example:

```
MOV KYREG,#0A7h          ;Write KYREG to 0xA7 to get write access to the POWCON SFR
MOV POWCON, #10H         ;Shutdown the core
```

POWER SUPPLY ARCHITECTURE

ADE75XX/ADE71XX has two power supply inputs, V_{DD} and V_{BAT}, and requires only a single 3.3V power supply at V_{DD} for full operation. A battery backup, or secondary power supply, with a maximum of 3.6V can be connected to the V_{BAT} input. Internally, the ADE75XX/ADE71XX connects V_{DD} or V_{BAT} to V_{SW}, which is used to derive the power for the ADE75XX/ADE71XX circuitry. The V_{SWOUT} output pin reflects the voltage at V_{SW}, and has a maximum output current of TBD mA. This pin may also be used to power a limited number of peripheral components. The 2.5V analog supply, V_{INTA} and the 2.5V supply for the core logic, V_{INTD}, are derived by on-chip linear regulators from V_{SW}. Figure 9 shows the power supply architecture of ADE75XX/ADE71XX.

The ADE75XX/ADE71XX provides automatic battery switchover between V_{DD} and V_{BAT} based on the voltage level detected at V_{DD} or V_{DCIN}. Additionally, the BCTRL input can also be used to trigger a battery switchover. The conditions for switching V_{SW} from V_{DD} to V_{BAT} and back to V_{DD} are described in the Battery Switchover section.

V_{DCIN} is an input pin that can be connected to a 0V to 3.3V DC signal. This input is intended for power supply supervisory purposes and does not provide power to the ADE75XX/ADE71XX circuitry - see Battery Switchover section.

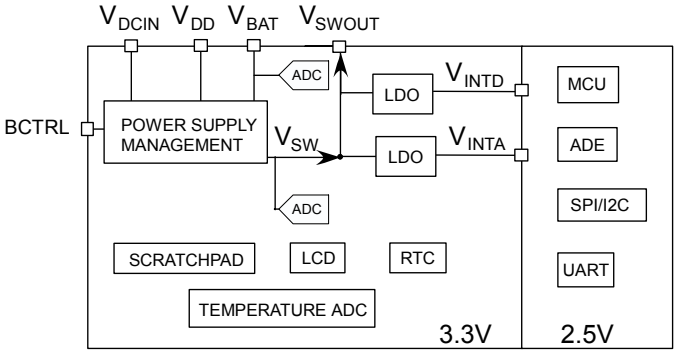


Figure 9: Power Supply Architecture

BATTERY SWITCHOVER

ADE75XX/ADE71XX monitors V_{DD}, V_{BAT}, and V_{DCIN}. Automatic battery switchover from V_{DD} to V_{BAT} can be configured based on the status of V_{DD}, V_{DCIN}, or the BCTRL pin. Battery switchover is enabled by default. Setting bit 1 in the Battery Switchover Configuration SFR (BATPR, 0xF5), disables battery switchover so that V_{DD} is always connected to V_{SW}. The source of V_{SW} is indicated by bit 6 in the Peripheral Configuration SFR (PERIPH, 0xF4), which is set when V_{SW} is connected to V_{DD} and cleared when V_{SW} is connected to V_{BAT}.

The battery switchover functionality provided by the ADE75XX/ADE71XX allows a seamless transition from V_{DD} to V_{BAT}. An automatic battery switchover option ensures a stable power supply to the ADE75XX/ADE71XX, as long as the external battery voltage is above TBD V. It allows continuous code execution even while the internal power supply is switching from V_{DD} to V_{BAT} and back. Note that the energy metering ADCs are not available when V_{BAT} is being used for

V_{SW}.

Power supply monitor (PSM) interrupts can be enabled to indicate when battery switchover occurs and when the V_{DD} power supply is restored - see the Power Supply Monitor Interrupt (PSM) section.

Switching from V_{DD} to V_{BAT}

There are three events that can be enabled to switch the internal power supply, V_{SW}, from V_{DD} to V_{BAT}:

1. **(V_{DCIN} < 1.2 V):** When V_{DCIN} falls below 1.2V V_{SW} switches from V_{DD} to V_{BAT}. This event is enabled when the BATTPROG[1:0] bits in the Battery Switchover Configuration SFR (BATPR, 0xF5) are clear. Setting this bit will disable switchover based on V_{DCIN}. Battery switchover on low V_{DCIN} is disabled by default.
2. **(V_{DD} < TBD V):** When V_{DD} falls below TBD V V_{SW} switches from V_{DD} to V_{BAT}. This event is enabled when BATTPROG[1] in the Battery Switchover Configuration SFR (BATPR, 0xF5) is cleared.
3. **Rising edge on BCTRL:** When the battery control pin, BCTRL, goes high, V_{SW} switches from V_{DD} to V_{BAT}. This external switchover signal can trigger a switchover to V_{BAT} at any time. Setting bits INT1PRG[4:2] to 0bx01 in the Interrupt pins configuration SFR (INTPR, 0xFF) enables the battery control pin.

Switching from V_{BAT} to V_{DD}

To switch V_{SW} back from V_{BAT} to V_{DD} all of the events that are enabled to force battery switchover must be false:

1. **(V_{DCIN} < 1.2 V) and (V_{DD} < TBD V) Enabled:** If the low V_{DCIN} condition is enabled, V_{SW} switches to V_{DD} after V_{DCIN} remains above TBD V for TBD seconds and V_{DD} remains above TBD V for TBD seconds.
2. **(V_{DD} < TBD V) Enabled:** V_{SW} switches back to V_{DD} after V_{DD} has been above TBD V for TBD seconds.
3. **BCTRL Enabled:** V_{SW} switches back to V_{DD} after BCTRL is low and number 1 or number 2 are satisfied.

POWER SUPPLY MONITOR INTERRUPT (PSM)

The Power Supply Monitor Interrupt (PSM) alerts the 8052 core of power supply events. The PSM interrupt is disabled by default. Setting the EPSM bit in the Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9) enables the PSM interrupt. The Power Management Interrupt Enable SFR (IPSME, 0xEC) controls the events that result in a PSM interrupt. Figure 10 is a diagram illustrating how the PSM interrupt vector is shared among the PSM interrupt sources. The PSM interrupt flags are latched and must be cleared by writing to the flag register.

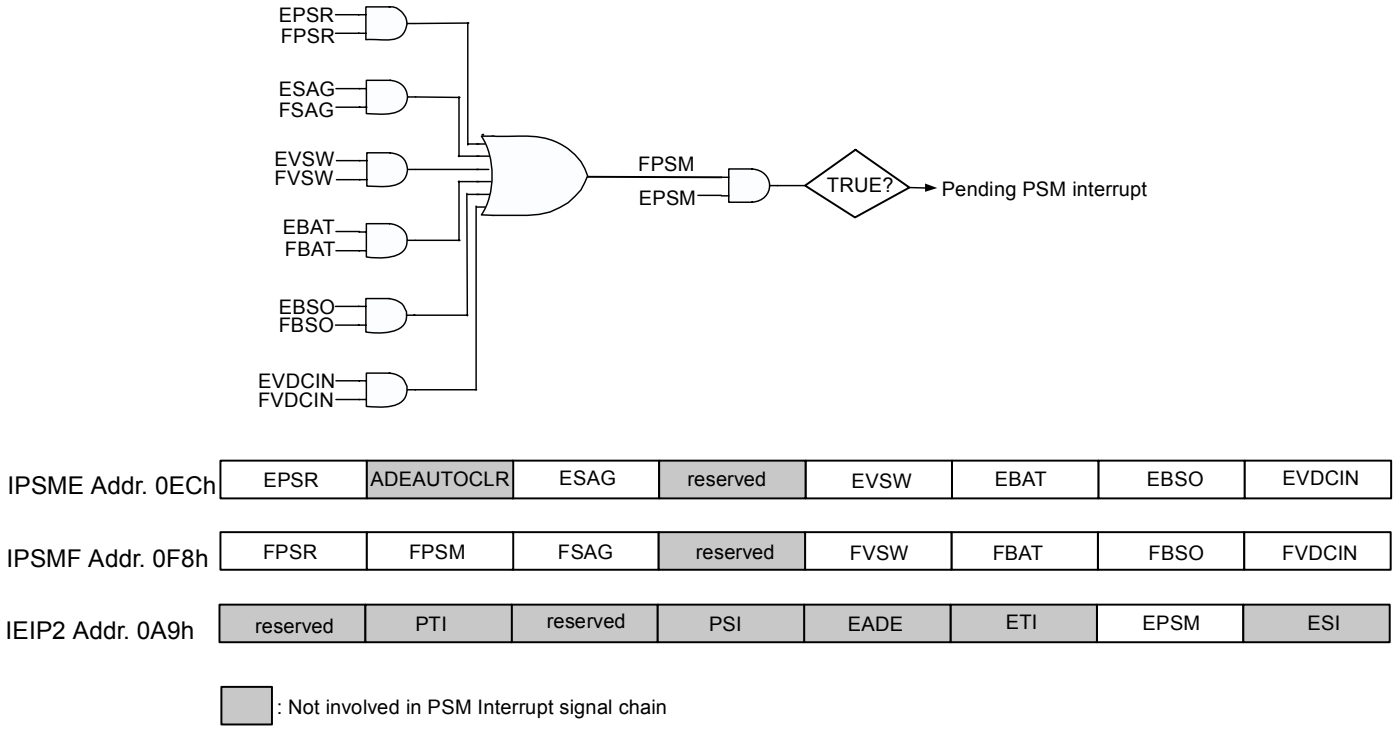


Figure 10: PSM Interrupt Sources

Battery Switchover and Power Supply Restored PSM Interrupt

The ADE75XX/ADE71XX can be configured to generate a PSM interrupt when the source of V_{SW} changes from V_{DD} to V_{BAT}, indicating battery switchover. Setting the EBSO bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

The ADE75XX/ADE71XX can also be configured to generate an interrupt when the source of V_{SW} changes from V_{BAT} to V_{DD}, indicating that the V_{DD} power supply has been restored. This event is enabled to generate a PSM interrupt by setting the EPSR bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC).

The flags in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) for these interrupts, BSOF and PSRF are set regardless of whether the respective enable bits have been set. The battery switchover and power supply restore event flags, BSOF and PSRF, are latched. These events must be cleared by writing a zero to these bits. Bit 6 in the Peripheral Configuration SFR (PERIPH, 0xF4), VSWSOURCE, tracks the source of V_{SW}. The bit is set when V_{SW} is connected to V_{DD} and cleared when V_{SW} is connected to V_{BAT}.

V_{DCIN} ADC PSM Interrupt

The ADE75XX/ADE71XX can be configured to generate a PSM interrupt when V_{DCIN} changes magnitude by more than a configurable threshold. This threshold is set in the Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3) –see External Voltage Measurement section. Setting the EVADC bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

The V_{DCIN} voltage is measured using a dedicated ADC. These measurements take place in the background at intervals to check the change in V_{DCIN}. Conversions can also be initiated by writing to the Start ADC Measurement SFR (ADCGO, 0xD8). The FVADC flag will indicate that a V_{DCIN} measurement is ready. See the External Voltage Measurement section for details on how V_{DCIN} is measured.

V_{BAT} Monitor PSM Interrupt

The V_{BAT} voltage is measured using a dedicated ADC. These measurements take place in the background at intervals to check the change in V_{BAT}. The BATTF bit is set when the battery level is lower than the threshold set in the Battery detection threshold SFR (BATVTH, 0xFA) or when a new measurement is ready in the Battery ADC value SFR (BATADC, 0xDF) - see Battery measurement section. Setting the EBATT bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

V_{DCIN} Monitor PSM Interrupt

The V_{DCIN} voltage is monitored by a comparator. The FVDC bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set when the V_{DCIN} input level is lower than 1.2 V. Setting the EVDCIN bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt. This event associated with the SAG monitoring can be used to detect a power supply - V_{DD} - being compromised and trigger further actions prior to decide a switch of V_{DD} to V_{BAT}.

SAG Monitor PSM Interrupt

The ADE75XX/ADE71XX energy measurement DSP monitors the ac voltage input at the V_P and V_N input pins. The SAGLVL register is used to set the threshold for a line voltage sag event. The SAGF bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set if the line voltage stays below the level set in the SAGLVL register for the number of line cycles set in the SAGCYC register, - see Line Voltage Sag Detection section. Setting the ESAG bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

USING THE POWER SUPPLY FEATURES

In an energy meter application, V_{DD}, the 3.3V power supply, is typically generated from the ac line voltage and regulated to 3.3V by a voltage regulator IC. The pre-regulated DC voltage, typically 5V to 12V, can be connected to V_{DCIN} through a resistor divider. A 3.6V battery can be connected to V_{BAT}. Figure 11 shows how the ADE75XX/ADE71XX power supply inputs would be set up in this application.

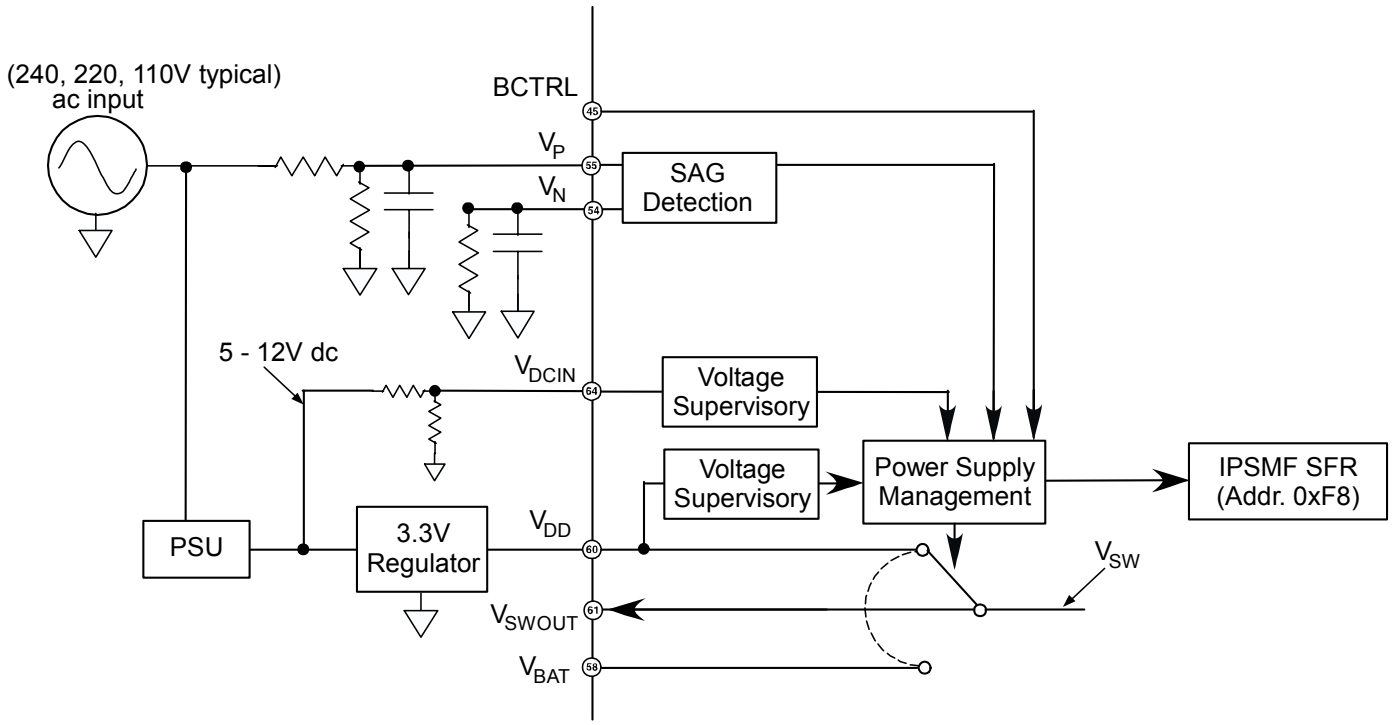


Figure 11. Power Supply Management for Energy Meter Application

Figure 12 shows the sequence of events that will be generated for the power meter application in Figure 11 if the main power supply generated by the PSU starts to fail. The sag detection can provide the earliest warning of a potential problem on V_{DD}. When a sag event occurs, the user code can be configured to backup data and prepare for battery switchover if desired. The relative spacing of these interrupts will depend on the design of the power supply.

Figure 13 shows the sequence of events that will be generated for the power meter application shown in Figure 11 if the main power supply starts to fail, with battery switchover on low V_{DCIN} or low V_{DD} enabled.

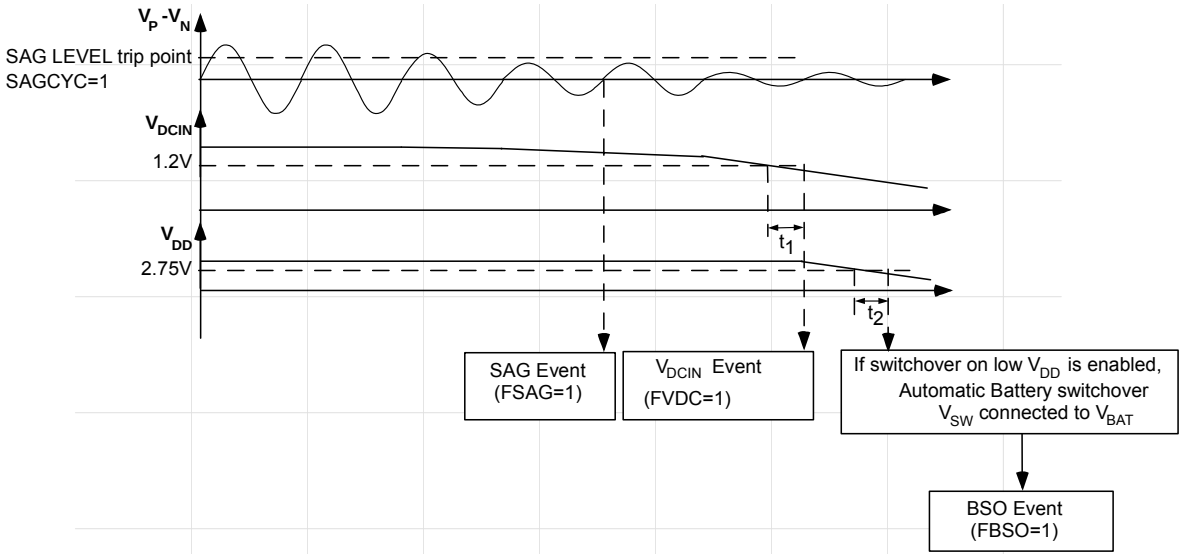


Figure 12: Power Supply Management Interrupts and Battery Switchover with only V_{DD} enabled for battery switchover

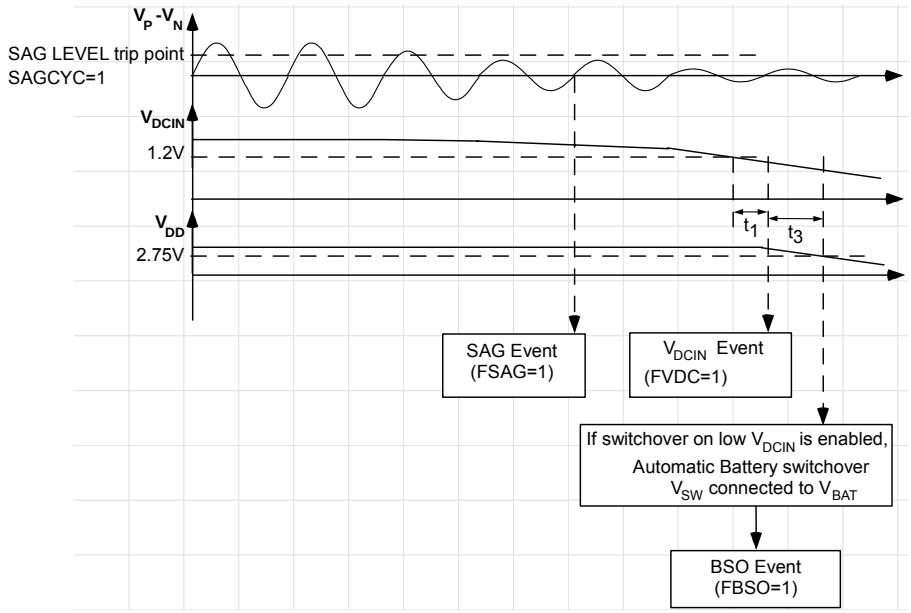


Figure 13: Power Supply Management Interrupts and Battery Switchover with V_{DD} or V_{DCIN} enabled for battery switchover

	Time	Comment
t_1	TBD	Time between when V_{DCIN} goes below 1.2 V and when FVDCIN is raised.
t_2	TBD	Time between when V_{DD} falls below TBD V and when battery switchover occurs.
t_3	TBD	Time between when V_{DCIN} falls below 1.2 V and when battery switchover occurs, if V_{DCIN} is enabled to cause battery switchover. VDCIN_OPT[1:0] in the Battery Switchover Configuration SFR (BATPR, 0xF5) sets this timeout

Table 23: Power Supply Event Timings Operating Modes

Finally, the transition between V_{DD} and V_{BAT} and the different Power Supply Modes (see Operating modessection) is represented in Figure 15.

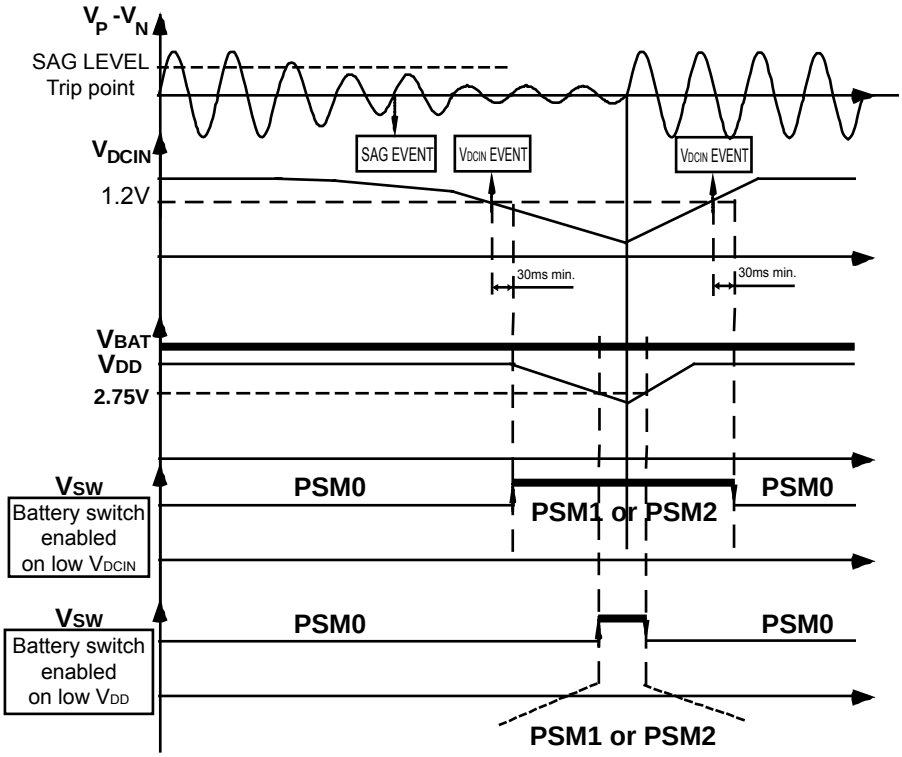


Figure 14: Power Supply Management transitions between modes

OPERATING MODES

PSM0 (NORMAL MODE)

In PSM0, normal operating mode, V_{SW} is connected to V_{DD}. All of the analog and digital circuitries powered by V_{INTD} and V_{INTA} are enabled by default. The default clock frequency for PSM0, F_{core}, established during a power-on-reset or software reset, is TBD MHz.

PSM1 (BATTERY MODE)

In PSM1, V_{SW} is connected to V_{BAT}. In this operating mode, the 8052 core and all of the digital circuitry are enabled by default. The analog circuitry for the ADE energy metering DSP powered by V_{INTA} is disabled. This analog circuitry will automatically start up again once the V_{DD} supply is above TBD V if the PWRDN bit in the MODE1 register (0x0B) is cleared. The default F_{core} for PSM1, established during a power-on-reset or software reset, is 1.024 MHz.

PSM2 (SLEEP MODE)

PSM2 is a low power consumption sleep mode for use in battery operation. In this mode, V_{SW} is connected to V_{BAT}. All of the 2.5V digital and analog circuitry powered through V_{INTA} and V_{INTD} is disabled, including the MCU core, resulting in the following:

1. The RAM in the MCU is no longer valid.
2. The program counter for the 8052, also held in volatile memory, becomes invalid when the 2.5V supply is shut down. Therefore, the program will not resume from where it left off but will always start from the power on reset vector when the ADE75XX/ADE71XX comes out of PSM2.

The 3.3V peripherals Temperature ADC, V_{BAT} ADC, V_{DCIN} ADC, RTC and LCD are active in PSM2. They can be enabled or disabled to reduce power consumption and are configured for PSM2 operation when the MCU core is active—see the individual peripherals for more information on their PSM2 configuration. The ADE75XX/ADE71XX remains in PSM2 until an event occurs to wake it up.

In PSM2, the ADE75XX/ADE71XX provides 4 scratch pad RAM SFR that are maintained during this mode. These SFRs can be used to save data from PSM0 or PSM1 modes when entering PSM2 modes - see Table 16 to Table 20.

In PSM2, the ADE75XX/ADE71XX maintains some SFRs – see Table 24. The SFRs that are not listed in this table should be restored when the part enters PSM0 or PSM1 frm PSM2 mode.

Table 24. SFR maintained in PSM2

I/O configuration	Power Supply monitoring
Interrupt pins configuration SFR (INTPR, 0xFF) Peripheral Configuration SFR (PERIPH, 0xF4) Port 0 Weak pull-up enable SFR (PINMAP0, 0xB2) Port 1 Weak pull-up enable SFR (PINMAP1, 0xB3) Port 2 Weak pull-up enable SFR (PINMAP2, 0xB4) Scratch Pad 1 SFR (SCRATCH1, 0xFB) Scratch Pad 2 SFR (SCRATCH2, 0xFC) Scratch Pad 3 SFR (SCRATCH3, 0xFD) Scratch Pad 4 SFR (SCRATCH4, 0xFE)	Battery detection threshold SFR (BATVTH, 0xFA) Battery Switchover Configuration SFR (BATPR, 0xF5) Battery ADC value SFR (BATADC, 0xDF) Peripheral ADC Strobe Period SFR (STRBPER, 0xF9) Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3) VDCIN ADC value SFR (VDCINADC, 0xEF) Temperature ADC value SFR (TEMPADC, 0xD7)
Peripherals – RTC	**Peripherals - LCD**
RTC Nominal Compensation SFR (RTCCOMP, 0xF6) RTC Temperature Compensation SFR (TEMPCAL, 0xF7) RTC Configuration SFR (TIMECON, 0xA1) Hundredths of a Second Counter SFR (HTHSEC, 0xA2) Seconds Counter SFR (SEC, 0xA3) Minutes Counter SFR (MIN, 0xA4) Hours Counter SFR (HOUR, 0xA5) Alarm Interval SFR (INTVAL, 0xA6)	LCD Segment Enable 2 SFR (LCDSEGE2, 0xED) LCD Configuration Y SFR (LCDCONY, 0xB1) LCD Configuration X SFR (LCDCONX, 0x9C) LCD Configuration SFR (LCDCON, 0x95) LCD Clock SFR (LCDCLK, 0x96) LCD Segment Enable SFR (LCDSEGE, 0x97)

3.3V PERIPHERALS AND WAKEUP EVENTS

Some of the 3.3V peripherals are capable of waking the ADE75XX/ADE71XX from PSM2. The events that can cause the ADE75XX/ADE71XX to wake from PSM2 are listed in the Wakeup Events column in Table 25.

Table 25. 3.3V Peripherals and Wakeup Events

3.3V Peripheral	Wakeup Event	Wakeup Enable Bits	Flag	Interrupt Vector	Comments
Temperature ADC	ΔT	Maskable	-	ITADC	The temperature ADC can wake-up the 8052 if the ITADC flag is set . This flag is set according to the description in the Temperature measurement section. This wakeup event can be disabled by disabling temperature measurements in the Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3) in PSM2.
V_{DCIN} ADC	ΔV	Maskable	FVADC	IPSM	The V_{DCIN} measurement can wake-up the 8052. The FVADC is set according to the description in the External Voltage Measurement section. This wakeup event can be disabled by clearing the EVADC in the Power Management Interrupt Enable SFR (IPSME, 0xEC).
Power Supply Management	PSR	Non-maskable	PSR	IPSM	The 8052 will wake up if the power supply is restored (if V_{SW} switches to be connected to V_{DD}). The VSWSOURCE flag, bit 6 of the Peripheral Configuration SFR (PERIPH, 0xF4) SFR, is set to indicate that V_{SW} is connected to V_{DD}. This is a nonmaskable wakeup event.
RTC	Midnight	Non-maskable	Midnight	IRTC	The ADE75XX/ADE71XX will wake up at midnight every day to update its calendar. This event is a nonmaskable wakeup event.
	Alarm	Maskable	Alarm	IRTC	Set an alarm to wake the ADE75XX/ADE71XX after the desired amount of time. The RTC Alarm is enabled by setting the alarm bit in the RTC Configuration SFR (TIMECON, 0xA1).
I/O Ports	All I/O pins are treated as inputs. The weak pull-up on each I/O pin can be disabled individually in the Port 0 Weak pull-up enable SFR (PINMAP0, 0xB2), Port 1 Weak pull-up enable SFR (PINMAP1, 0xB3) and Port 2 Weak pull-up enable SFR (PINMAP2, 0xB4) to decrease current consumption and also avoid powering up disabled peripheral through the internal pull-up through the I2C port for example. The interrupts can be enabled/disabled.				
	$\overline{INT0}$	INT0PROG =1	-	IE0	The edge of the interrupt is selected by TCON.IT0 The IE0 flag bit in the TCON register will not be affected.
	$\overline{INT1}$	INT1PROG [2:0]= 11X	-	IE1	The edge of the interrupt is selected by TCON.IT1 The IE1 flag bit in the TCON register will not be affected.
	RX Edge	RXPROG [1:0] = 11	PERIPH.7 (RXFG)	-	An RX Edge event will occur if a rising or falling edge is detected on the RX line
External Reset	RESET	Non-maskable	-	-	If the RESET pin is brought low while the ADE75XX/ADE71XX is in PSM2, it will wake up to PSM1.
LCD	-	-	-	-	The LCD can be enabled/disabled in PSM2. The LCD data memory will remain intact.
Scratchpad	-	-	-	-	The 4 SCRATCHx registers will remain intact in PSM2.

TRANSITIONING BETWEEN OPERATING MODES

The operating mode of the ADE75XX/ADE71XX is determined by the power supply connected to V_{SW}. Therefore a change in the power supply such as when V_{SW} switches from V_{DD} to V_{BAT} or when V_{SW} switches to V_{DD} changes the operating mode. This section describes events that change the operating mode.

Automatic Battery Switchover (PSM0 to PSM1)

If any of the enabled battery switchover events occur (see the Battery Switchover section), V_{SW} switches to V_{BAT}. This switchover results in a transition from the PSM0 to PSM1

operating mode. When battery switchover occurs, the analog circuitry used in the ADE energy measurement DSP is disabled. To reduce power consumption, the user code can initiate a transition to PSM2.

Entering Sleep Mode (PSM1 to PSM2)

To reduce power consumption when V_{SW} is connected to V_{BAT}, user code can initiate sleep mode, PSM2, by setting bit 4 in the Power Control SFR (POWCON, 0xC5) to shut down the MCU core. Events capable of waking the MCU can be enabled—see the 3.3V Peripherals and Wakeup Events section.

Servicing Wakeup Events (PSM2 to PSM1)

The ADE75XX/ADE71XX may need to wake up from PSM2 to service wakeup events – see the 3.3V Peripherals and Wakeup Events section. PSM1 code execution will begin at the power on reset vector. After servicing the wakeup event, the ADE75XX/ADE71XX can return to PSM2 by setting bit 4 in the Power Control SFR (POWCON, 0xC5) to shut down the MCU core.

Automatic Switch to V_{DD} (PSM2 to PSM0)

If the conditions to switch V_{SW} from V_{BAT} to V_{DD} occur (see the Battery Switchover section), the operating mode will switch to PSM0. When this switch occurs, the MCU core and the analog circuitry used in the ADE energy measurement DSP will start up again automatically. PSM0 code execution will begin at the power on reset vector.

Automatic Switch to V_{DD} (PSM1 to PSM0)

If the conditions to switch V_{SW} from V_{BAT} to V_{DD} occur (see the Battery Switchover section), the operating mode will switch to PSM0. When this switch occurs, the analog circuitry used in the ADE energy measurement DSP will start up automatically. Note that code execution will continue normally. A software reset can be performed to start PSM0 code execution at the power on reset vector.

USING THE POWER MANAGEMENT FEATURES

Since program flow is different for each operating mode, the status of V_{SW} must be known at all times. The VSWSOURCE bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) indicates what V_{SW} is connected to. This bit can be used to control program flow on wakeup. Since code execution always starts at the power on reset vector, bit 6 of the Peripheral Configuration SFR (PERIPH, 0xF4) can be tested to determine which power supply is being used and to branch to normal code execution or to wakeup event code execution. Power supply events can also occur when the MCU core is active. To be aware of events that change what V_{SW} is connected to:

- Enable the battery switchover interrupt (EBSO) if V_{SW}=V_{DD} at power up.
- Enable the power supply restored interrupt (EPSR) if V_{SW}=V_{BAT} at power up.

An early warning that battery switchover is about to occur is provided by SAG detection and possibly low V_{DCIN} detection—see the Battery Switchover section.

For a user controlled battery switchover, enable automatic battery switchover on low V_{DD} only. Then enable the low V_{DCIN} event to generate the PSM interrupt. When a low V_{DCIN} event occurs, start data backup. Upon completion of the data backup, enable battery switchover on low V_{DCIN}. Then battery switchover will occur TBDms later.

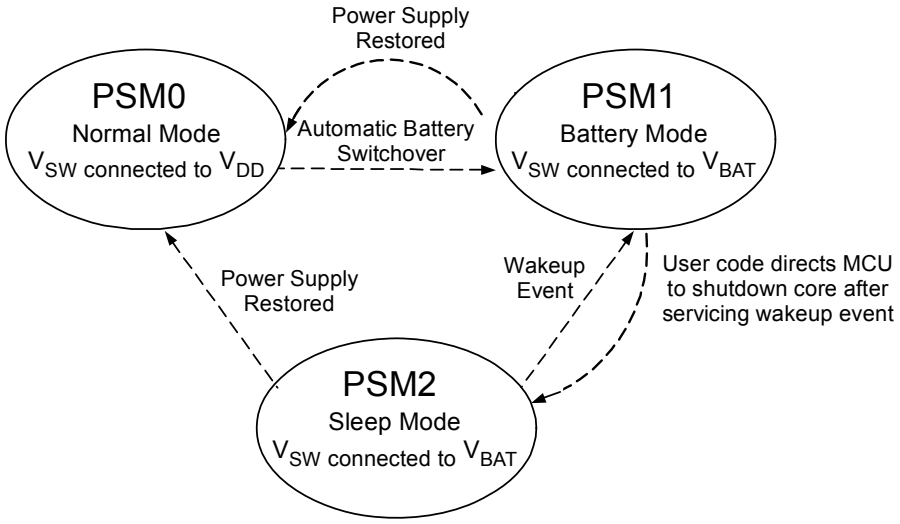


Figure 15: Transitioning between Operating Modes

ENERGY MEASUREMENT

The ADE75xx/ADE71xx provides a fixed function energy measurement Digital Processing core that provides all the information needed to measure energy in a single phase energy meters. The ADE75xx/ADE71xx provides two ways to access the energy measurements: Direct access through SFR for time sensitive information and indirect access through address and data SFR registers for the majority of the energy measurements. The IRMS, VRMS, interrupts and waveform registers are readily available through SFRs as shown in Table 26. Other energy measurement information is mapped to a page of memory that is accessed indirectly through. The address and data registers act as pointers to the energy measurement internal registers.

ACCESS TO ENERGY MEASUREMENT SFR

Access to the energy measurement SFRs is achieved by reading or writing to the SFR addresses detailed in Table 27. The internal data for the MIRQx SFRs are latched byte by byte into the SFR when the SFR is read.

The WAV1x, WAV2x, VRMSx and IRMSx registers are all 3 bytes SFRs. The 24-bit data is latched into these SFRs when the High byte is read. Reading the Low or Medium byte before the High byte results in reading the date from the previous latched sample.

Sample 8051 code to read the VRMS register is shown below:

```
MOV    R1, VRMSH   //latches data in VrmsH, VrmsM and
                   VrmsL SFR
MOV    R2, VRMSM
MOV    R3, VRMSL
```

ACCESS TO INTERNAL ENERGY MEASUREMENT REGISTERS

Access to the internal energy measurement registers is achieved by writing to the Energy Measurement pointer address (SFR address 91h). The MADDPT register selects the energy measurement register to be accessed and determines if a read or a write is performed—see Table 26.

Table 26. Energy Measurement pointer address SFR (MADDPT, 0x91)

Bit	7	6	5	4	3	2	1	0
Description	1: Write 0: Read	Energy Measurement internal register address						

Writing to Internal energy measurement registers

When bit7 of MADDPT SFR is set, the content of the MDATA SFRs (MDATL, MDATM and MDATH) is transferred to the internal energy measurement register designated by the address in MADDPT SFR. If the internal register is one byte long, only MDATL SFR content is copied to the internal register while MDATM and MDATH SFR contents are ignored.

The energy measurement core functions with an internal clock of 4.096 MHz/5 or 819.2 kHz. As the 8052 core functions with another clock, 4.096MHz / 2^{CD}, synchronization between the two clock environments when CD = 0 or 1 is an issue. When data is written to the internal energy measurement a small wait period need to be implemented before another read or write to these registers is implemented.

Sample 8051 code to write 0x0155 to the two bytes SAGLVL register, located at 14h in the energy measurement memory space is shown below:

```
MOV    MDATM,#01h
MOV    MDATL,#55h
MOV    MADDPT,#SAGLVL_W  (address 0x94)
MOV    A,  #05h
DJNZ   ACC, $
       ;Next Write or read to Energy Measurement SFR can
       be done after this.
```

Reading Internal energy measurement registers

When bit7 of MADDPT SFR is cleared, the content of the internal energy measurement register designated by the address in MADDPT is transferred to the MDATA SFRs (MDATL, MDATM and MDATH). If the internal register is one byte long, only the MDATL SFR content is updated with a new value while MDATM and MDATH SFR content are reset to 00h.

The energy measurement core functions with an internal clock of 4.096 MHz/5 or 819.2 kHz. As the 8052 core functions with another clock, 4.096MHz / 2^{CD}, synchronization between the two clock environments when CD = 0 or 1 is an issue. When data is read from the internal energy measurement, a small wait period need to be implemented before the MDATx SFRs are transferred to another SFR.

Sample 8051 code to read the peak voltage in the 2-byte VPKLVL register, located at 0x16, into the data pointer is shown below:

```
MOV    MADDPT,#VPKLVL_R (address 0x16)
MOV    A,  #05h
DJNZ   ACC, $
MOV    DPH, MDATM
MOV    DPL, MDATL
```

Table 27. Energy measurement SFRs

SFR address (hex)	R/W	Name	Description
0x91	R/W	MADDPT	Energy Measurement Pointer Address
0x92	R/W	MDATL	Energy Measurement Pointer Data LSByte
0x93	R/W	MDATM	Energy Measurement Pointer Data Middle byte
0x94	R/W	MDATH	Energy Measurement Pointer Data MSByte
0xD1	R	VRMSL	Vrms measurement LSByte
0xD2	R	VRMSM	Vrms measurement Middle byte
0xD3	R	VRMSH	Vrms measurement MSByte
0xD4	R	IRMSL	Irms measurement LSByte
0xD5	R	IRMSM	Irms measurement Middle byte
0xD6	R	IRMSH	Irms measurement MSByte
0xD9	R/W	MIRQENL	Energy measurement interrupt enable LSByte
0xDA	R/W	MIRQENM	Energy measurement interrupt enable Middle byte
0xDB	R/W	MIRQENH	Energy measurement interrupt enable MSByte
0xDC	R/W	MIRQSTL	Energy measurement interrupt status LSByte
0xDD	R/W	MIRQSTM	Energy measurement interrupt status Middle byte
0xDE	R/W	MIRQSTH	Energy measurement interrupt status MSByte
0xE2	R	WAV1L	Selection 1 sample LSByte
0xE3	R	WAV1M	Selection 1 sample Middle byte
0xE4	R	WAV1H	Selection 1 sample MSByte
0xE5	R	WAV2L	Selection 2 sample LSByte
0xE6	R	WAV2M	Selection 2 sample Middle byte
0xE7	R	WAV2H	Selection 2 sample MSByte

ENERGY MEASUREMENT REGISTERS

Table 28. Energy Measurement Register List

Address MADDPT[6:0]	Name	R/W	Length	Signed /Unsigned	Default Value	Description
0x00	Reserved	-	-	-	-	-
0x01	WATTHR	R	24	S	0	Read Watt-hour accumulator without reset
0x02	RWATTHR	R	24	S	0	Read Watt-hour accumulator with reset
0x03	LWATTHR	R	24	S	0	Read Watt-hour accumulator synchronous to line cycle

Address MADDPT[6:0]	Name	R/W	Length	Signed /Unsigned	Default Value	Description
0x04	VARHR	R	24	S	0	Read VAR-hour accumulator without reset[3]
0x05	RVARHR	R	24	S	0	Read VAR-hour accumulator with reset[1]
0x06	LVARHR	R	24	S	0	Read VAR-hour accumulator synchronous to line cycle[1]
0x07	VAHR	R	24	S	0	Read VA-hour accumulator without reset
0x08	RVAHR	R	24	S	0	Read VA-hour accumulator with reset
0x09	LVAHR	R	24	S	0	Read VA-hour accumulator synchronous to line cycle
0x0A	PER_FREQ	R	16	U	0	Read Line Period or Frequency register depending on Mode2 register
0x0B	MODE1	R/W	8	U	0x06	Set basic configuration of energy measurement – see Table 29
0x0C	MODE2	R/W	8	U	0x40	Set basic configuration of energy measurement – see Table 30
0x0D	WAVMODE	R/W	8	U	0	Set configuration of waveform sample 1 and waveform sample 2 – see Table 31
0x0E	NLMODE	R/W	8	U	0	Set level of energy no-load thresholds - Table 32
0x0F	ACCMODE	R/W	8	U	0	Set configuration of Watt, VAR accumulation and various tamper alarms – see Table 33
0x10	PHCAL	R/W	8	S	0x40	Set phase calibration register – see Phase Compensation section
0x11	ZXTOUT	R/W	12		0x0FFF	Set time out for Zero-crossing time out detection – see Zero-Crossing Timeout
0x12	LINCYC	R/W	16	U	0xFFFF	Set number of half line cycles for LWATTHR, LVARHR and LVAHR accumulators
0x13	SAGCYC	R/W	8	U	0xFF	Set number of half line cycles for SAG detection – see Line Voltage Sag Detection
0x14	SAGLVL	R/W	16	U	0	Set detection level for SAG detection - see Line Voltage Sag Detection
0x15	IPKLVL	R/W	16	U	0xFFFF	Set peak detection level for current peak detection – see Peak Detection
0x16	VPKLVL	R/W	16	U	0xFFFF	Set peak detection level for voltage peak detection– see Peak Detection
0x17	IPEAK	R	24	U	0	Read current peak level without reset – see Peak Detection
0x18	RSTIPEAK	R	24	U	0	Read current peak level with reset – see Peak Detection
0x19	VPEAK	R	16	U	0	Read voltage peak level without reset – see Peak Detection
0x1A	RSTVPEAK	R	16	U	0	Read voltage peak level with reset – see Peak Detection
0x1B	GAIN	R/W	8	U	0	Set PGA gain of analog inputs – see Table 34
0x1C	IBGAIN[4]	R/W	12	S	0	Set Matching Gain for IB current input
0x1D	WGAIN	R/W	12	S	0	Set Watt gain register
0x1E	VARGAIN	R/W	12	S	0	Set VAR gain register
0x1F	VAGAIN	R/W	12	S	0	Set VA gain register
0x20	WATTOS	R/W	16	S	0	Set Watt offset register
0x21	VAROS	R/W	16	S	0	Set VAR offset register
0x22	IRMSOS	R/W	12	S	0	Set current rms offset register
0x23	VRMSOS	R/W	12	S	0	Set voltage rms offset register
0x24	WDIV	R/W	8	U	0	Set Watt energy scaling register

[3] This function is not available in ADE7566 and ADE7166 products.
[4] This function is not available in ADE7566 and ADE7569 products.

Address MADDPT[6:0]	Name	R/W	Length	Signed /Unsigned	Default Value	Description
0x25	VARDIV	R/W	8	U	0	Set VAR energy scaling register
0x26	VADIV	R/W	8	U	0	Set VA energy scaling register
0x27	CF1NUM	R/W	16	U	0	Set CF1 numerator register
0x28	CF1DEN	R/W	16	U	0x003F	Set CF1 denominator register
0x29	CF2NUM	R/W	16	U	0	Set CF2 numerator register
0x2A	CF2DEN	R/W	16	U	0x003F	Set CF2 denominator register
0x3D	CALMODE	R/W	8	U	0	Set Calibration Mode

ENERGY MEASUREMENT INTERNAL REGISTERS DETAILS

Table 29. MODE1 register (0x0B)

Bit Location	Bit Mnemonic	Default Value	Description
7	SWRST	0	Setting this bit will reset all of the energy measurement registers to their default values
6	DISZXLPF	0	Setting this bit disables the zero-crossing lowpass filter
5	INTE[1]	0	Setting this bit enables the digital integrator for use with a di/dt sensor
4	SWAPBITS	0	Setting this bit swaps CH1 & CH2 ADCs
3	PWRDN	0	Setting this bit powers down voltage and current ADC's
2	DISCF2	1	Setting this bit disables Frequency output CF2
1	DISCF1	1	Setting this bit disables Frequency output CF1
0	DISHPF	0	Setting this bit disables the HPFs in voltage and current channels

Table 30. MODE2 register (0x0C)

Bit Location	Bit Mnemonic	Default Value	Description
7-6	CF2SEL[1:0]	01	Configuration bits for CF2 output CF2SEL[1:0] Source 00 CF2 frequency is proportional to active power 01 CF2 frequency is proportional to reactive power[5] 1x CF2 frequency is proportional to apparent power or IRMS
5-4	CF1SEL[1:0]	00	Configuration bits for CF1 output CF1SEL[1:0] Source 00 CF1 frequency is proportional to active power 01 CF1 frequency is proportional to reactive power[1] 1x CF1 frequency is proportional to apparent power or IRMS
3	VARMSCFCON	0	Configuration bits for apparent power or IRMS for CF1 and CF2 outputs 0 If CF1SEL[1:0]=1x, CF1 is proportional to VA If CF2SEL[1:0]=1x, CF2 is proportional to VA 1 If CF1SEL[1:0]=1x, CF1 is proportional to IRMS If CF2SEL[1:0]=1x, CF2 is proportional to IRMS Note that CF1 cannot be proportional to VA if CF2 is proportional to IRMS and vice versa
2	ZXRMS	0	Logic one enables update of RMS values synchronously to voltage ZX
1	FREQSEL	0	Configuration bits to select PERIOD or FREQUENCY measurement for PER_FREQ register (0Ah) 0 PER_FREQ register holds a period measurement

[5] This function is not available in ADE7566 and ADE7166 products.

			1 PER_FREQ register holds a frequency measurement
0	Reserved	1	This bit should be kept to one

Table 31. WAVMODE register (0x0D)

Bit Location	Bit Mnemonic	Default Value	Description
7-5	WAV2SEL[2:0]	0	Waveform 2 selection for samples mode WAV2SEL[2:0] Source 000 Current 001 Voltage 010 Active Power multiplier output 011 Reactive Power multiplier output[6] 100 VA multiplier output 101 IRMS LPF output others Reserved
4-2	WAV1SEL[2:]	0	Waveform 1 selection for samples mode WAV1SEL[2:0] Source 000 Current 001 Voltage 010 Active Power multiplier output 011 Reactive Power multiplier output[1] 100 VA multiplier output 101 IRMS LPF output (low 24-bit) others Reserved
1-0	DTRT[1:0]	0	Waveform samples output data rate DTRT[1:0] Update rate (clock=MCLK/5=819.2kHz) 00 25.6Ksps(clock/32) 01 12.8Ksps(clock/64) 10 6.4Ksps(clock/128) 11 3.2Ksps(clock/256)

Table 32. NLMODE register (0x0E)

Bit Location	Bit Mnemonic	Default Value	Description
7	DISVARCMP[1]	0	Setting this bit disables fundamental VAR gain compensation over line frequency
6	IRMSNOLOAD	0	Logic one enables IRMS no-load thresold detection. The level is defined by the setting of the VANOLOADbits.
5-4	VANOLOAD[1:0]	0	Apparent Power No-load threshold [1:0] 00 No-load detection disabled 01 No-load enabled with threshold = 0.030% of Full scale 10 No-load enabled with threshold = 0.015% of Full scale 11 No-load enabled with threshold = 0.0075% of Full scale
3-2	VARNOLOAD[1:0] [1]	0	Reactive Power No-load threshold [1:0] 00 No-load detection disabled 01 No-load enabled with threshold = 0.015% of Full scale 10 No-load enabled with threshold = 0.0075% of Full scale 11 No-load enabled with threshold = 0.0037% of Full scale
1-0	APNOLOAD[1:0]	0	Active Power No-load threshold

[6] This function is not available in ADE7566 and ADE7166 products.

			[1:0] 00 No-load detection disabled 01 No-load enabled with threshold = 0.015% of Full scale 10 No-load enabled with threshold = 0.0075% of Full scale 11 No-load enabled with threshold = 0.0037% of Full scale

Table 33. ACCMODE register (0x0F)

Bit Location	Bit Mnemonic	Default Value	Description
7	ICHANNEL[7]	0	This bit indicate the current channel used to measure energy in anti-tampering mode. 0 – Channel A 1 – Channel B
6	FAULTSIGN[1]	0	Configuration bit to select event that will trigger a Fault interrupt 0 – FAULT interrupt occurs when part enters Fault Mode 1 – FAULT interrupt occurs when part enters Normal Mode
5	VARSIGN[8]	0	Configuration bit to select event that will trigger an reactive power sign interrupt 0 – VARSIGN interrupt occurs when reactive power changes from positive to negative 1 - VARSIGN interrupt occurs when reactive power changes from negative to positive
4	APSIGN	0	Configuration bit to select event that will trigger an active power sign interrupt 0 – APSIGN interrupt occurs when active power changes from positive to negative 1 - APSIGN interrupt occurs when active power changes from negative to positive
3	ABSVARM[2]	0	Logic one enables absolute value accumulation of Reactive power in energy register and pulse output
2	SAVARM[2]	0	Logic one enables reactive power accumulation depending on the sign of the active power: If Active Power is positive, VAR is accumulated as it is; If Active Power is negative, the sign of the VAR is reversed for the accumulation. This accumulation mode affects both the VAR registers and the VARCF output.
1	POAM	0	Logic one enables positive only accumulation of Active power in energy register and pulse output
0	ABSAM	0	Logic one enables absolute value accumulation of Active power in energy register and pulse output

Table 34. GAIN register (0x1B)

Bit Location	Bit Mnemonic	Default Value	Description
7 - 5	PGA2[2:0]	0	These bits define the voltage channel input gain [2:0] 000 Gain = 1 001 Gain = 2 010 Gain = 4 011 Gain = 8

[7] This function is not available in ADE7566 and ADE7569 products.
[8] This function is not available in ADE7566 and ADE7166 products.

			100 Gain = 16
4	Reserved	0	Reserved
3	CFSIGN_OPT	0	This bit defines where the CF change of sign, APSIGN or VARSIGN, detection is implemented. 0 Filtered power signal 1 On a per CF pulse basis
2 - 0	PGA1[2:0]	0	These bits define the current channel input gain [2:0] 000 Gain = 1 001 Gain = 2 010 Gain = 4 011 Gain = 8 100 Gain = 16

Table 35. CALMODE register (0x3D)

Bit Location	Bit Mnemonic	Default Value	Description
7 – 6	Reserved	0	These bits should be kept cleared for proper operation
5 - 4	SEL_I_CH[1:0][9]	0	These bits define the current channel used for energy measurements [1:0] 00 Current channel automatically selected by the tampering condition 01 Current channel connected to I_A 10 Current channel connected to I_B 11 Current channel automatically selected by the tampering condition
3	V_CH_SHORT	0	Logic one short voltage channel to ground
2	I_CH_SHORT	0	Logic one short Current channels to ground
1 - 0	Reserved		

Table 36. Interrupt Status Register 1 SFR (MIRQSTL, 0xDC)

Bit Location	Interrupt Flag	Description
7	ADEIRQFLAG	This bit is set if any of the ADE status flags that are enabled to generate an ADE interrupt are set. This bit is automatically cleared when all of the enabled ADE status flags are cleared.
6	Reserved	Reserved.
5	FAULTSIGN[1]	Logic one indicates that the Fault mode has changed according to the configuration of the ACCMODE register
4	VARSIGN[10]	Logic one indicates that the reactive power sign changed according to the configuration of ACCMODE register
3	APSIGN	Logic one indicates that the active power sign changed according to the configuration of ACCMODE register
2	VANOLOAD	Logic one indicates that an interrupt was caused by apparent power no-load detected. This interrupt is also used to reflect the part entering the IRMS No load mode.
1	RNOLOAD[2]	Logic one indicates that an interrupt was caused by reactive power no-load detected.
0	APNOLOAD	Logic one indicates that an interrupt was caused by active power no-load detected.

Table 37. Interrupt Status Register 2 SFR (MIRQSTM, 0xDD)

Bit Location	Interrupt Flag	Description

[9] This function is not available in ADE7566 and ADE7569 products.
[10] This function is not available in ADE7566 and ADE7166 products.

7	CF2	Logic one indicates that a pulse on CF2 has been issued. The flag is set even if CF2 pulse output is not enabled by clearing bit 2 of MODE1 register.
6	CF1	Logic one indicates that a pulse on CF1 has been issued. The flag is set even if CF1 pulse output is not enabled by clearing bit 1 of MODE1 register.
5	VAEOF	Logic one indicates that the VAHR register has overflowded
4	REOF[11]	Logic one indicates that the VARHR register has overflowded
3	AEOF	Logic one indicates that the WATTHR register has overflowded
2	VAEHF	Logic one indicates that the VAHR register is half full
1	REHF[1]	Logic one indicates that the VARHR register is half full
0	AEHF	Logic one indicates that the WATTHR register is half full

Table 38. Interrupt Status Register 3 SFR (MIRQSTH, 0xDE)

Bit Location	Interrupt Flag	Description
7	RESET	Indicates the end of a reset (for both sofware or hardware reset).
6	-	Reserved
5	WFSM	Logic one indicates that new data is present in the Waveform Registers
4	PKI	Logic one indicates that current channel has exceeded the IPKLVL value
3	PKV	Logic one indicates that voltage channel has exceeded the VPKLVL value.
2	CYCEND	Logic one indicates the end of the energy accumulation over an integer number of half line cycles.
1	ZXTO	Logic one indicates that no zero crossing on the line voltage happened for the last ZXTOUT half line cycles.
0	ZX	Logic one indicates detection of a zero crossing in the voltage channel.

Table 39. Interrupt Enable Register 1 SFR (MIRQENL, 0xD9)

Bit Location	Interrupt Flag	Description
7-6	Reserved	Reserved.
5	FAULTSIGN[12]	When this bit is set, the FAULTSIGN bit set creates a pending ADE interrupt to the 8052 core.
4	VARSIGN[1]	When this bit is set, the VARSIGN bit set creates a pending ADE interrupt to the 8052 core.
3	APSIGN	When this bit is set, the APSIGN bit set creates a pending ADE interrupt to the 8052 core.
2	VANOLOAD	When this bit is set, the VANOLOAD bit set creates a pending ADE interrupt to the 8052 core.
1	RNOLOAD[1]	When this bit is set, the RNOLOAD bit set creates a pending ADE interrupt to the 8052 core.
0	APNOLOAD	When this bit is set, the APNOLOAD bit set creates a pending ADE interrupt to the 8052 core.

Table 40. Interrupt Enable Register 2 SFR (MIRQENM, 0xDA)

Bit Location	Interrupt Flag	Description
7	CF2	When this bit is set, a CF2 pulse issued creates a pending ADE interrupt to the 8052 core.
6	CF1	When this bit is set, a CF1 pulse issued creates a pending ADE interrupt to the 8052 core.
5	VAEOF	When this bit is set, the VAEOF flag set creates a pending ADE interrupt to the 8052 core.
4	REOF[1]	When this bit is set, the REOF flag set creates a pending ADE interrupt to the 8052 core.
3	AEOF	When this bit is set, the AEOF flag set creates a pending ADE interrupt to the 8052 core.
2	VAEHF	When this bit is set, the VAEHF flag set creates a pending ADE interrupt to the 8052 core.
1	REHF[1]	When this bit is set, the REHF flag set creates a pending ADE interrupt to the 8052 core.

[11] This function is not available in ADE7566 and ADE7166 products.
[12] This function is not available in ADE7566 and ADE7569 products.

0	AEHF	When this bit is set, the AEHF flag set creates a pending ADE interrupt to the 8052 core.

Table 41. Interrupt Enable Register 3 SFR (MIRQENH, 0xDB)

Bit Location	Interrupt Flag	Description
7-6	-	Reserved
5	WFSM	When this bit is set, the WFSM flag set creates a pending ADE interrupt to the 8052 core.
4	PKI	When this bit is set, the PKI flag set creates a pending ADE interrupt to the 8052 core.
3	PKV	When this bit is set, the PKV flag set creates a pending ADE interrupt to the 8052 core..
2	CYCEND	When this bit is set, the CYCEND flag set creates a pending ADE interrupt to the 8052 core.
1	ZXTO	When this bit is set, the ZXTO flag set creates a pending ADE interrupt to the 8052 core.
0	ZX	When this bit is set, the ZX flag set creates a pending ADE interrupt to the 8052 core.

ANALOG INPUTS

The ADE75XX/ADE71XX has two fully differential voltage input channels. The maximum differential input voltage for input pairs VP/VN and IP/IN are ±0.5 V. In addition, the maximum signal level on analog inputs for VP/VN and IP/ IN is ±0.5 V with respect to AGND.

Each analog input channel has a PGA (programmable gain amplifier) with possible gain selections of 1, 2, 4, 8, and 16. The gain selections are made by writing to the GAIN register in the Energy Measurement Register List—see Table 34 and

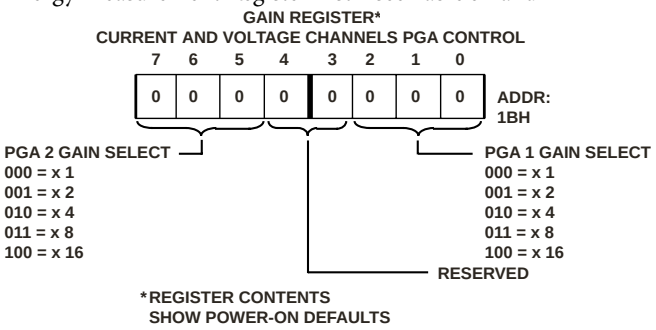


Figure 17. Bits 0 to 2 select the gain for the PGA in the current channel, and the gain selection for the PGA in voltage channel is made via Bits 5 to 7. Figure 16 shows how a gain selection for the current channel is made using the gain register.

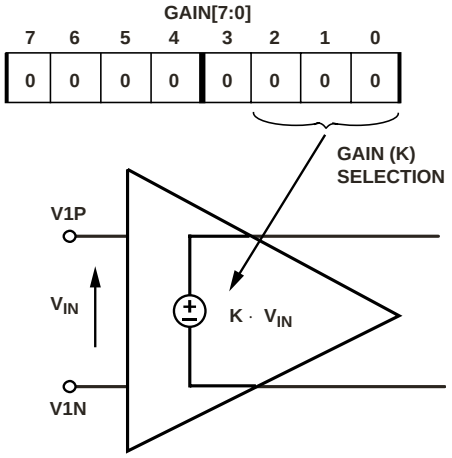


Figure 16. PGA in current channel

In addition to the PGA, Channel 1 also has a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register—see

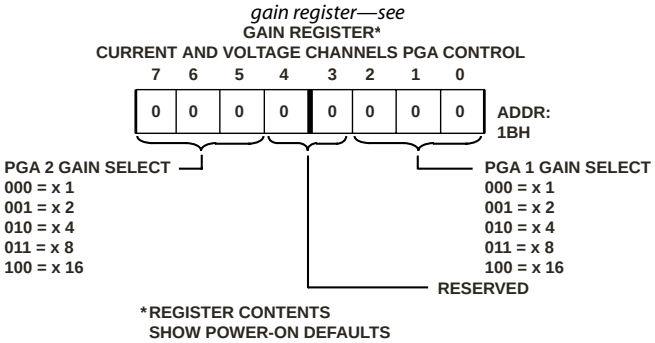


Figure 17. As mentioned previously, the maximum differential input voltage is 0.5 V.

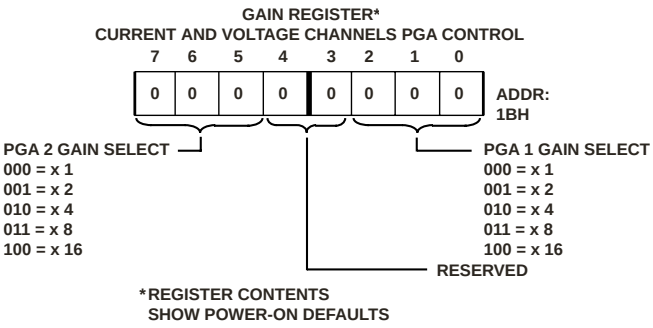


Figure 17. ADE75XX/ADE71XX Analog Gain Register

ANALOG TO DIGITAL CONVERSION

The ADE75XX/ADE71XX has two sigma-delta Analog to Digital Converters (ADC). The outputs of these ADCs are mapped directly to waveform sampling SFRs (address 0xE2 to 0xE7) and are used for the energy measurement internal digital signal processing. In PSM1 (Battery mode)and PSM2 (Sleep mode), the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 18 shows a first-order Σ-Δ ADC. The converter is made up of the Σ-Δ modulator and the digital low-pass filter.

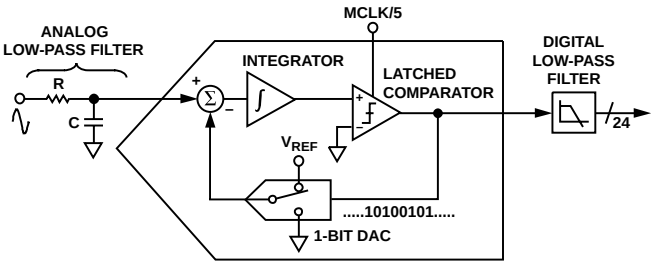


Figure 18. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE75xx/ADE71xx, the sampling clock is equal to MCLK/5. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency), which is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE75xx/ADE71xx is MCLK/5 (819.2 kHz) and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered — see Figure 19. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 19.

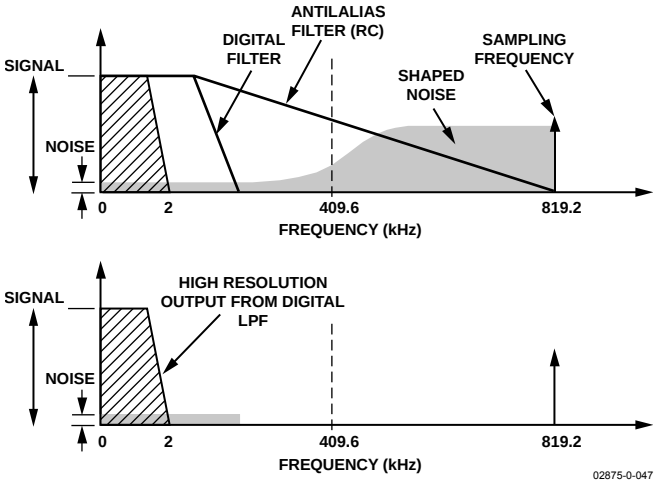


Figure 19. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Anti-aliasing Filter

Figure 18 also shows an analog low-pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Figure 20 illustrates the effect. Frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency, i.e., 409.6 kHz) are imaged or folded back down below 409.6 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 819.2 kHz, move into the band of interest for metering, i.e., 40 Hz to 2 kHz. This allows the use of a very simple LPF (low-pass filter) to attenuate high frequency (near 819.2 kHz) noise, and prevents distortion in the band of interest. For conventional current sensors, a simple RC filter (single-pole LPF) with a

corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 819.2 kHz — see Figure 20. The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the –20 dB per decade attenuation produced by one simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade two RC filters to produce the –40 dB per decade attenuation needed.

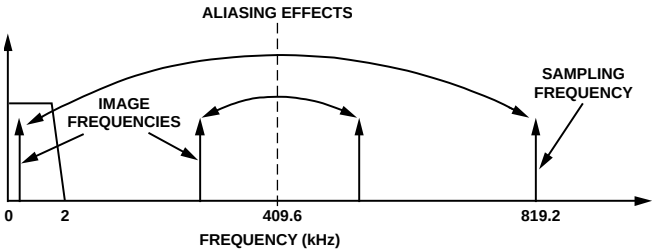


Figure 20. ADC and Signal Processing in current channel Outline Dimensions

ADC Transfer Function

Both ADCs in the ADE75xx/ADE71xx are designed to produce the same output code for the same input signal level. With a full-scale signal on the input of 0.5 V and an internal reference of 1.2 V, the ADC output code is nominally 2,684,354 or 28F5C2h. The maximum code from the ADC is ±4,194,304; this is equivalent to an input signal level of ±0.794 V. However, for specified performance, it is recommended that the full-scale input signal level of 0.5 V not be exceeded.

Current Channel ADC

Figure 21 shows the ADC and signal processing chain for the current channel. In waveform sampling mode, the ADC outputs a signed twos complement 24-bit data-word at a maximum of 25.6 kSPS (MCLK/160). With the specified full-scale analog input signal of 0.5 V (or 0.25 V or 0.125 V—see the Analog Inputs section) the ADC produces an output code that is approximately between 0x28F5C2 (+2,684,354d) and 0xD70A3E (–2,684,354d)—see Figure 21.

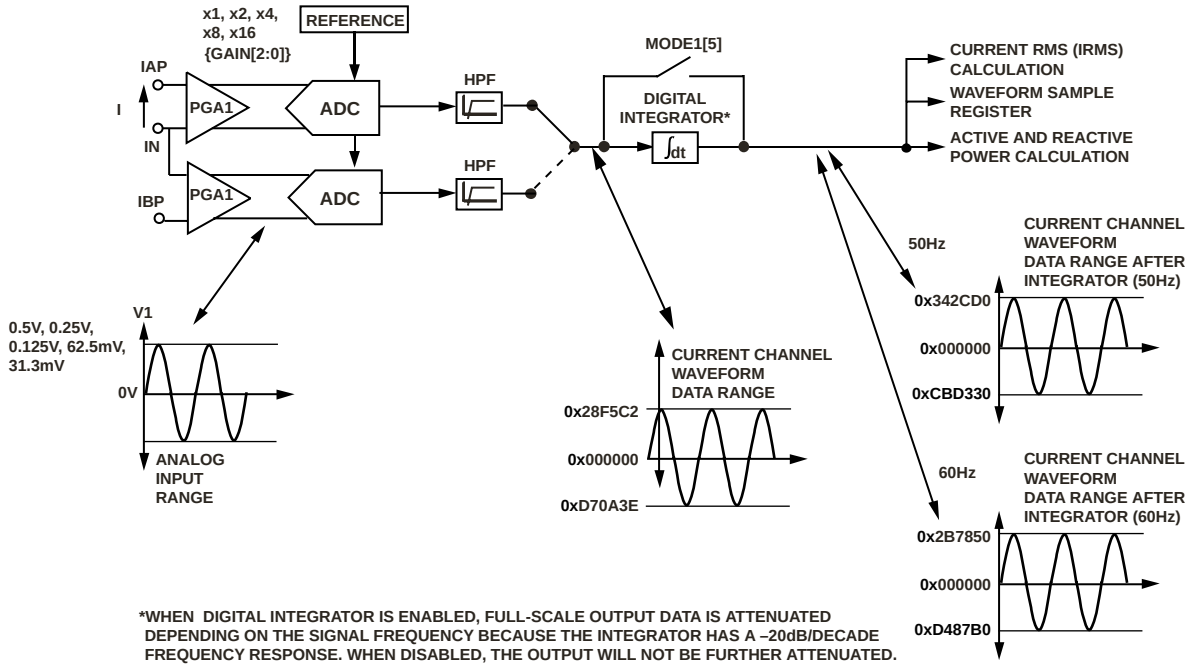


Figure 21. ADC and Signal Processing in Current Channel

Voltage Channel ADC

Figure 21 shows the ADC and signal processing chain for the Voltage Channel. In waveform sampling mode, the ADC outputs a signed twos complement 24-bit data-word at a maximum of 25.6 kSPS (MCLK/160). The ADC produces an output code that is approximately between 0x28F5 (+10,485d) and 0xD70B (–10,485d)—see Figure 22.

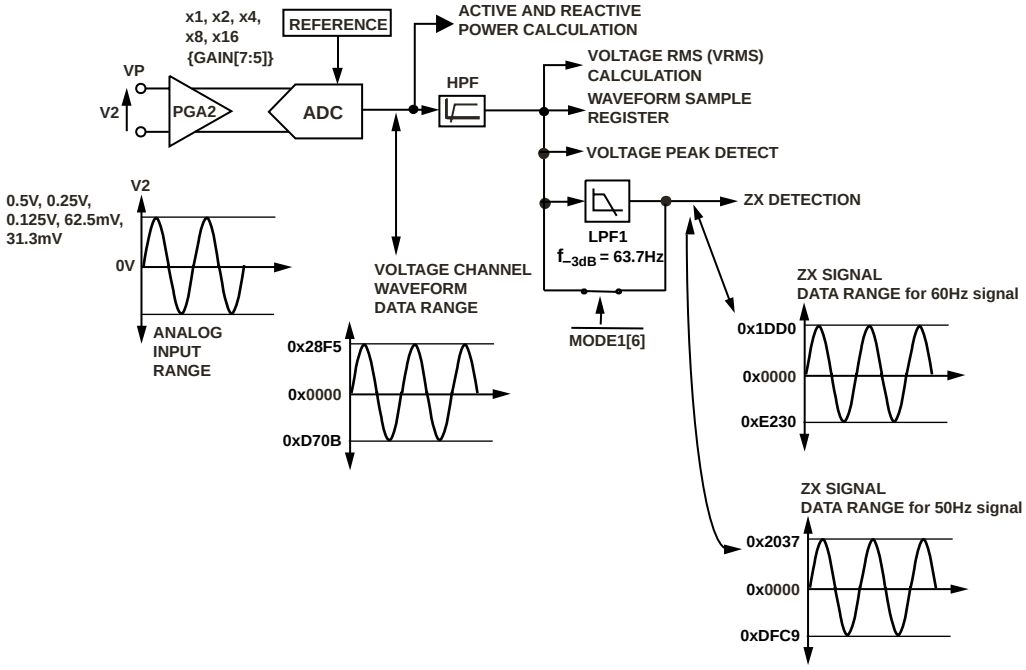


Figure 22. ADC and Signal Processing in Voltage Channel

Channel Sampling

The waveform samples of the current ADC and voltage ADC can also be routed to the waveform registers to be read by the MCU core. The active, reactive, apparent power, and energy calculation remain uninterrupted during waveform sampling.

When in waveform sampling mode, one of four output sample rates can be chosen by using Bits 0 and 1 of the WAVMODE register (WAVSEL1,0). The output sample rate can be 25.6 kSPS, 12.8kSPS, 6.4 kSPS, or 3.2 kSPS—see Table 31. If the WFSM enable bit is set in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt. The sampled signals selected in the WAVMODE register will be latched into the Waveform SFRs when the waveform high byte (WAV1H or WAV2H) is read.

The ADE interrupt stays active until the WFSM status bit is cleared—see Energy measurement interrupts section.

FAULT DETECTION[13]

The ADE75xx/ADE71xx incorporates a fault detection scheme that warns of fault conditions and allows the ADE75xx/ADE71xx to continue accurate measurement during a fault event. The ADE75xx/ADE71xx does this by continuously monitoring both current inputs (IA and IB). These currents will be referred for ease of understanding as phase and neutral (return) currents. In the ADE75xx/ADE71xx, a fault condition is defined when the difference between I_A and I_B is greater than 6.25% of the active channel. If a fault condition is detected and the inactive channel is larger than the active channel, the ADE75xx/ADE71xx automatically switches to current measurement to the inactive channel. During a fault, the active, reactive, current rms and apparent powers are generated using the larger of the two currents. On power-up, I_A is the current input selected for Active, Reactive, and Apparent power and Irms calculations.

To prevent false alarm, averaging is done for the fault detection and a fault condition is detected approximately 1 second after the event. The fault detection is automatically disabled when the voltage signal is less than 0.3% of the full-scale input range. This eliminates false detection of a fault due to noise at light loads.

Because the ADE75xx/ADE71xx looks for a difference between the voltage signals on I_A and I_B, it is important that both current transducers be closely matched.

Channel selection Indication

The current channel selected for measurement is indicated by bit 7 (ICHANNEL) in the ACCMODE register (0x0F). When this bit is cleared, I_A is selected and when it is set, I_B is selected. The ADE75xx/ADE71xx automatically switches from one channel to the other and reports the channel configuration in the ACCMODE register (0x0F).

The current channel selected for measurement can also be forced. Setting one of the SELCH1A and SELCH1B bits in the CALMODE register (0x3D) selects I_A and I_B respectively. When

[13] This function is not available in ADE7566 and ADE7569 products.

both bits are cleared or set, the current channel used for measurement is selected automatically based on the Fault detection.

Fault Indication

The ADE75xx/ADE71xx provides an indication of the part going in or out of a fault condition. The new fault condition is indicated by the FAULTSIGN flag (bit5) in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC).

When FAULTSIGN bit (bit 6) of ACCMODE register (0x0F) is cleared, the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when the part is entering fault condition.

When FAULTSIGN bit (bit 6) of ACCMODE register (0x0F) is set, the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when the part is entering normal condition.

When the FAULTSIGN bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), and the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set, the 8052 core has a pending ADE interrupt.

Fault with Active Input Greater than Inactive Input

If I_A is the active current input (that is, being used for billing), and the voltage signal on I_B (inactive input) falls below 93.75% of I_A, and the FAULTSIGN bit (bit 6) of ACCMODE register (0x0F) is cleared, the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set. Both analog inputs are filtered and averaged to prevent false triggering of this logic output. As a consequence of the filtering, there is a time delay of approximately 3 s on the logic output after the fault event. The FAULTSIGN flag is independent of any activity. Because I_A is the active input and it is still greater than I_B, billing is maintained on I_A, that is, no swap to the I_B input occurs. I_A remains the active input.

Fault with Inactive Input Greater than Active Input

If the difference between I_B, the inactive input, and I_A, the active input (that is, being used for billing), becomes greater than 6.25% of I_B, and the FAULTSIGN bit (bit 6) of ACCMODE register (0x0F) is cleared, the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set. The analog input I_B becomes the active input. Again, a time constant of about 3 s is associated with this swap. I_A does not swap back to the active channel until I_A is greater than I_B and the difference between I_A and I_B—in this order—becomes greater than 6.25% of I_B. However, if FAULTSIGN bit (bit 6) of ACCMODE register (0x0F) is set, the FAULTSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set as soon as I_A is within 6.25% of I_B. This threshold eliminates potential chatter between I_A and I_B.

Calibration Concerns

Typically, when a meter is being calibrated, the voltage and current circuits are separated as shown in Figure 23. This means that current passes through only the phase or neutral circuit. Figure 23 shows current being passed through the phase circuit. This is the preferred option, because the ADE75xx/ADE71xx starts billing on the input I_A on power-up. The phase circuit CT is connected to I_A in the diagram. As the current sensors are not perfectly matched, it is important to match current inputs. The ADE75xx/ADE71xx provides a gain calibration register for I_B, IBGAIN (address 0x1C). IBGAIN is a 12-bit signed 2-complement register that provides a gain resolution of 0.0244%/LSB.

For calibration, a first measurement should be done on I_A by setting SEL_I_CH bits to 0b01 in the CALMODE register (0x3D). This measurement should be compared to the measurement on I_B. Measuring I_B can be forced by setting SEL_I_CH bits to 0b10 in the CALMODE register (0x3D). The Gain error between these two measurements can be evaluated using: $Error(\%) = \frac{Measurement(I_B) - Measurement(I_A)}{Measurement(I_A)}$

The two channels I_A and I_B can then be matched by writing: – Error(%) / (1 + Error (%)) * 2^{12} to IBGAIN register. This matching adjustment will be valid for all energy measurements, Active power, reactive power, Irms, and Apparent power, made by the ADE75xx/ADE71xx.

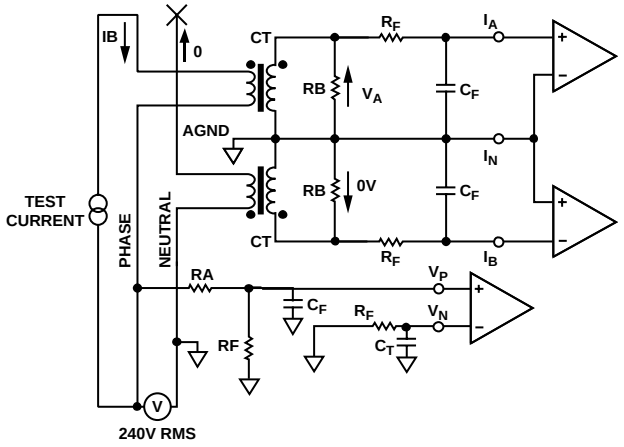


Figure 23. Fault Conditions for Inactive Input Greater than Active Input

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR[14]

A di/dt sensor detects changes in magnetic field caused by ac current. Figure 24 shows the principle of a di/dt current sensor.

[14] This function is not available in ADE7566 and ADE7166 products.

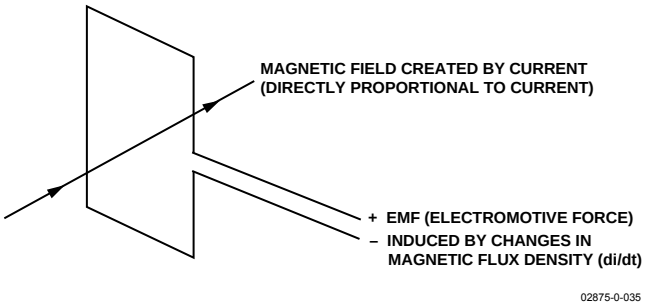


Figure 24. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal, which is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current-carrying conductor and the di/dt sensor. The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE75xx/ADE71xx has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on the Current Channel is switched off by default when the ADE75xx/ADE71xx is powered up. Setting INTE bit in the MODE1 register (0x0B) turns on the integrator. Figure 25 to Figure 28 show the magnitude and phase response of the digital integrator.

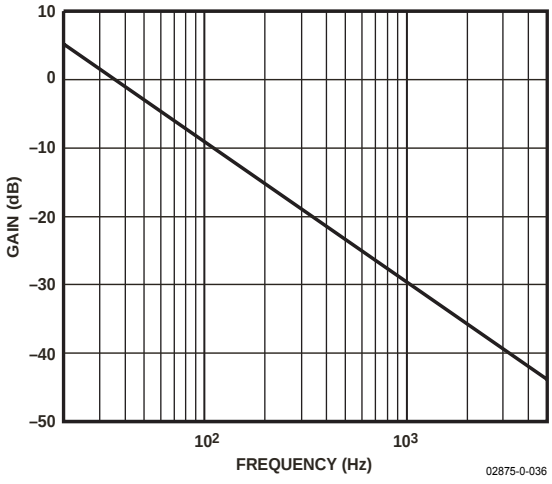


Figure 25. Combined Gain Response of the Digital Integrator and Phase Compensator

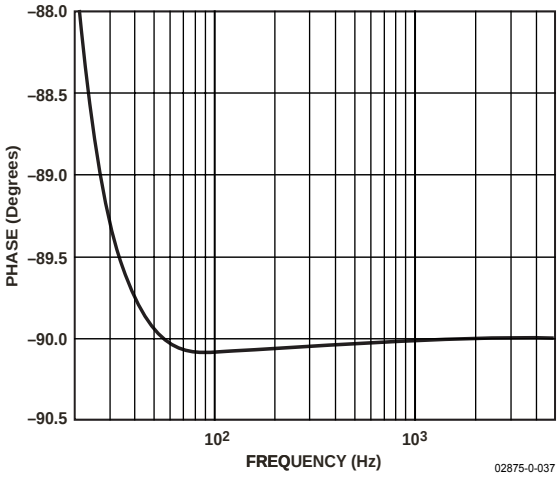


Figure 26. Combined Phase Response of the Digital Integrator and Phase Compensator

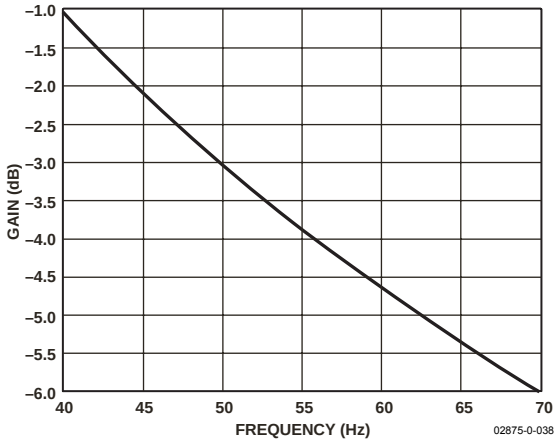


Figure 27. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

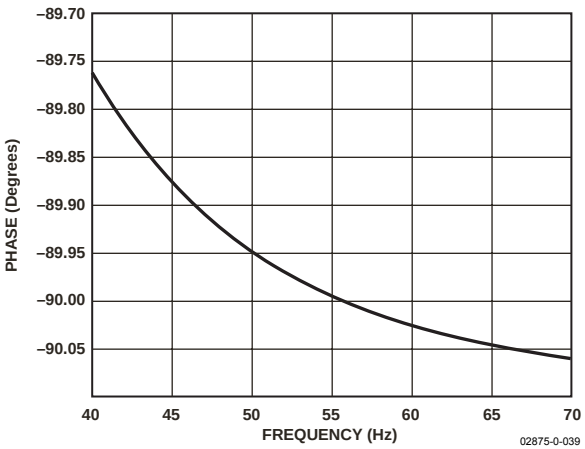


Figure 28. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

Note that the integrator has a –20 dB/dec attenuation and an approximately –90° phase shift. When combined with a di/dt

sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. The di/dt sensor has a 20 dB/dec gain associated with it. It also generates significant high frequency noise, therefore a more effective anti-aliasing filter is needed to avoid noise due to aliasing—see the Anti-aliasing Filter section.

When the digital integrator is switched off, the ADE75xx/ADE71xx can be used directly with a conventional current sensor such as a current transformer (CT) or with a low resistance current shunt.

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE75xx/ADE71xx has a zero-crossing detection circuit on the voltage channel. This zero crossing is used to produce an external zero-crossing signal (ZX), and it is also used in the calibration mode.

The zero-crossing is generated, by default, from the output of LPF1. As explained in the following paragraph, this filter has a low cut-off frequency and is intended for use for 50 and 60Hz system. If needed this filter can be disabled to allow a higher frequency signal to be detected or to limit the group delay of the detection. If the voltage input fundamental frequency is below 60Hz and a time delay in ZX detection is acceptable, it is recommended to enable LPF1. Enabling LPF1 will limit the variability in the ZX detection by eliminating the high frequency components.

Figure 29 shows how the zero-crossing signal is generated.

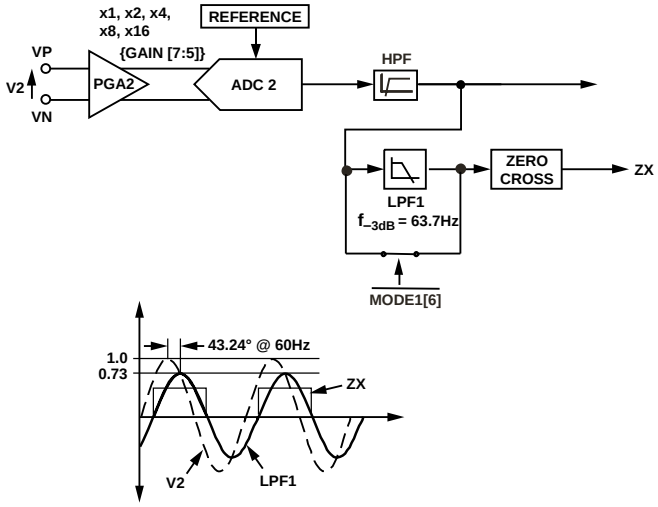


Figure 29. Zero-Crossing Detection on Voltage channel

The zero-crossing signal ZX is generated from the output of LPF1 (bypassed or not). LPF1 has a single pole at 63.7 Hz (at MCLK = 4.096 MHz). As a result, there is a phase lag between the analog input signal V2 and the output of LPF1. The phase lag response of LPF1 results in a time delay of approximately 2 ms (@ 60 Hz) between the zero crossing on the analog inputs of the voltage channel and ZX detection.

The zero-crossing detection also drives the ZX flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE). If the ZX bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt.

The ADE interrupt stays active until the ZX status bit is cleared—see Energy measurement interrupts section.

Zero-Crossing Timeout

The zero-crossing detection also has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB) every 160/MCLK seconds. The register is reset to its user programmed full-scale value every time a zero crossing is detected on the voltage channel. The default power on value in this register is 0xFFF. If the internal register decrements to 0 before a zero crossing is detected and the ZXTOUT flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE) is set. If the ZXTO bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt.

The ADE interrupt stays active until the ZXTO status bit is cleared—see Energy measurement interrupts section.

The ZXOUT register (Address 0x11) can be written or read by the user—see Energy Measurement Register List. The resolution of the register is 160/MCLK seconds per LSB. Thus the maximum delay for an interrupt is 0.16 second ($128/MCLK \times 2^{12}$) when MCLK = 4.096MHz.

Figure 30 shows the mechanism of the zero-crossing timeout detection when the line voltage stays at a fixed dc level for more than CLKIN/160 × ZXTOUT seconds.

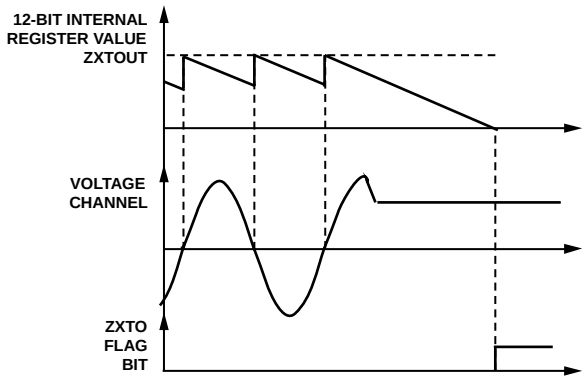


Figure 30. Zero-Crossing Timeout Detection

Period or Frequency Measurements

The ADE75XX/ADE71XX provides the period or frequency measurement of the line. The period or frequency measurement is selected by clearing or setting FREQSEL bit in the MODE2 register (0x0C). The period/frequency register is an unsigned 16-bit register and is updated every period. If LPF1 is enabled, a settling time of 1.8 seconds is associated with this filter before the measurement is stable.

When the period measurement is selected, the measurement has a 2.44 µs/LSB (MCLK/10) when MCLK = 4.096 MHz, which represents 0.014% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately 0d6827. The length of the register enables the measurement of line frequencies as low as 12.5 Hz. The period register is stable at ±1 LSB when the line is established and the measurement does not change.

When the frequency measurement is selected, the measurement has a 0.0625 Hz/LSB resolution when MCLK = 4.096MHz which represents 0.104% when the line frequency is 60Hz. When the line frequency is 60Hz, the value of the frequency register is 0d960. The frequency register is stable at ±4 LSB when the line is established and the measurement does not change.

Line Voltage Sag Detection

In addition to the detection of the loss of the line voltage signal (zero crossing), the ADE75XX/ADE71XX can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value for a number of line cycles. This condition is illustrated in Figure 31.

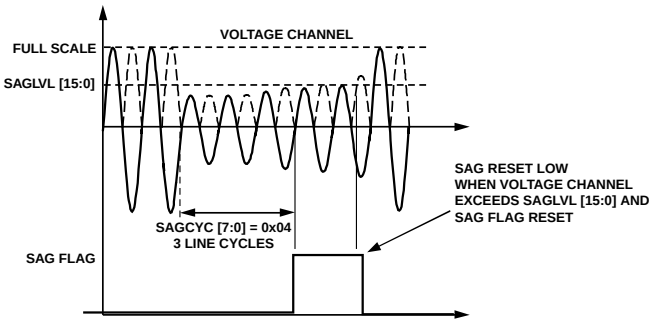


Figure 31. ADE75XX/ADE71XX Sag Detection

Figure 31 shows the line voltage falling below a threshold that is set in the sag level register (SAGLVL[15:0]) for three line cycles. The quantities 0 and 1 are not valid for the SAGCYC register, and the contents represent one more than the desired number of full line cycles. For example, when the sag cycle (SAGCYC[7:0]) contains 0x04, the SAG flag in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set at the end of the third line cycle for which the line voltage falls below the threshold. If the SAG enable bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) is set the 8052 core has a pending Power Supply Monitoring interrupt. The PSM interrupt stays active until the SAG status bit is cleared—see Power Supply Monitor Interrupt (PSM) section.

On Figure 31, the SAG flag is set as soon as the fifth line cycle from the time when the signal on the Voltage channel first dropped below the threshold level.

Sag Level Set

The contents of the sag level register (2 bytes) are compared to the absolute value of the output from LPF1. Therefore, when LPF1 is enabled, writing 0x2038 to the SAG level register puts the sag detection level at full scale – see Figure 22. Writing 0x00 or 0x01 puts the sag detection level at 0. The SAG level register is compared to the input of the ZX detection and detection is made when the contents of the sag level register are greater.

Peak Detection

The ADE75XX/ADE71XX can also be programmed to detect when the absolute value of the voltage or current channel exceeds a specified peak value. Figure 32 illustrates the behavior of the peak detection for the voltage channel. Both Voltage and Current Channels are monitored at the same time.

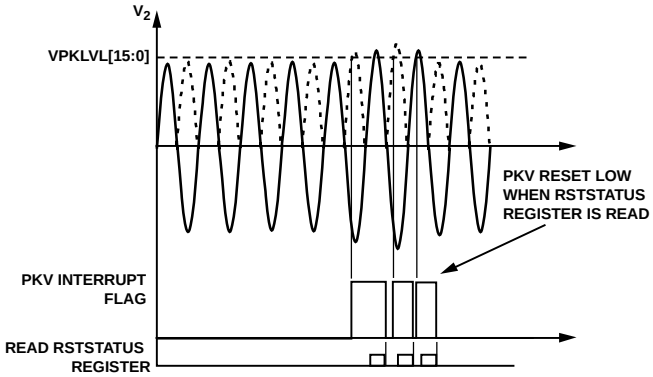


Figure 32. ADE75XX/ADE71XX Peak Level Detection

Figure 32 shows a line voltage exceeding a threshold that is set in the voltage peak register (VPKLVL[15:0]). The voltage peak event is recorded by setting the PKV flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE). If the PKV enable bit is set in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt. Similarly, the current peak event is recorded by setting the PKI flag in Interrupt Status Register 3 SFR (MIRQSTH, 0xDE). The ADE interrupt stays active until the PKV or PKI status bits are cleared—see Energy measurement interrupts section.

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are respectively compared to the absolute value of the voltage and current channels two most significant bytes. Thus, for example, the nominal maximum code from the Current Channel ADC with a full-scale signal is 0x28F5C2—see the Current Channel ADC section. Therefore, writing 0x28F5 to the IPKLVL register, for example, puts the current channel peak detection level at full scale and sets the current peak detection to its least sensitive value. Writing 0x00 puts the Current channel detection level at 0. The detection is done by comparing the contents of the IPKLVL register to the incoming Current channel sample. The PKI flag indicates that the peak level is exceeded if the PKI or

PKV bits are set in Interrupt Enable Register 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt.

Peak Level Record

The ADE75XX/ADE71XX records the maximum absolute value reached by the voltage and current channels in two different registers—IPEAK and VPEAK, respectively. VPEAK and IPEAK are 16-bit unsigned registers. These registers are updated each time the absolute value of the waveform sample from the corresponding channel is above the value stored in the VPEAK or IPEAK register. The contents of the VPEAK register correspond to the maximum absolute value observed on the voltage channel input. The contents of IPEAK and VPEAK represent the maximum absolute value observed on the Current and Voltage input respectively. Reading the RSTVPEAK and RSTIPEAK registers clears their respective contents after the read operation.

PHASE COMPENSATION

The ADE75XX/ADE71XX must work with transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE75XX/ADE71XX provides a means of digitally calibrating these small phase errors. The ADE75XX/ADE71XX allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is in time, this technique should be used only for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[7:0]) is a twos complement signed single-byte register that has values ranging from 0x82 (–126d) to 0x68 (104d).

The register is centered at 0x40, so that writing 0x40 to the register gives 0 delay. By changing the PHCAL register, the time delay in the Voltage channel signal path can change from –231.93 µs to +48.83 µs (MCLK = 4.096 MHz). One LSB is equivalent to 1.22 µs (MCLK/5) time delay or advance. A line frequency of 60 Hz gives a phase resolution of 0.026° at the fundamental (i.e., 360° × 1.22 µs × 60 Hz)) or 0.00732% of the line period. Similarly, a line frequency of 50Hz gives a phase resolution of 0.022° at the fundamental or 0.0061% of the line period. Figure 33 illustrates how the phase compensation is used to remove a 0.1° phase lead in Current channel due to the external transducer. To cancel the lead (0.1°) in Current channel, a phase lead must also be introduced into Voltage channel. The resolution of the phase adjustment allows the introduction of a phase lead in increment of 0.026°. The phase lead is achieved by introducing a time advance into Voltage channel. A time advance of 4.88 µs is made by writing –4 (0x3C) to the time delay block, thus reducing the amount of time delay by 4.88 µs, or equivalently, a phase lead of approximately 0.1° at line frequency of 60 Hz. 0x3C represents –4 because the register is centered with 0 at 0x40.

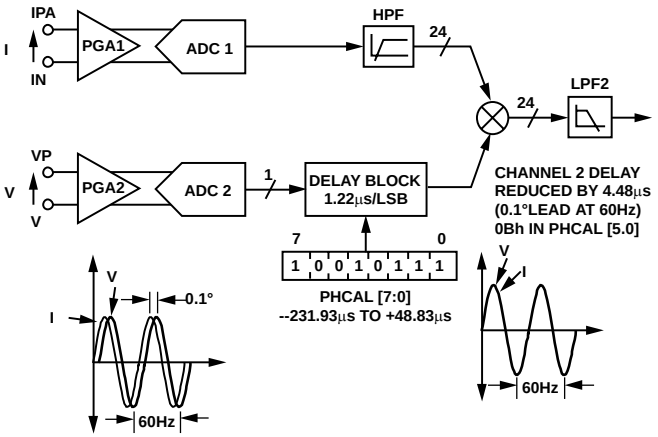


Figure 33. Phase Calibration

ADE75XX/ADE71XX RMS CALCULATION

Root mean square (rms) value of a continuous signal V(t) is defined as

$$VRMS = V_{rms} = \sqrt{\frac{1}{T}\times\int_{0}^{T} V^2(t)dt} \quad (2)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average and obtaining the square root. The ADE75XX/ADE71XX implements this method by serially squaring the input, averaging them and then taking the root square of the average. The averaging part of this signal processing is done by implementing a Low Pass filter (LPF3 in Figure 35 and Figure 36). This LPF has a -3dB cut-off frequency of 2Hz when MCLK = 4.096MHz.

$V(t) = \sqrt{2}\times V\sin(\omega t)$ where: V is the rms voltage.

$$V^2(t) = V^2 - V^2\cos(2\omega t)$$

When this signal goes through LPF3, the cos(2ωt) term is attenuated and only the DC term V_{rms}^2 goes through – see Figure 34.

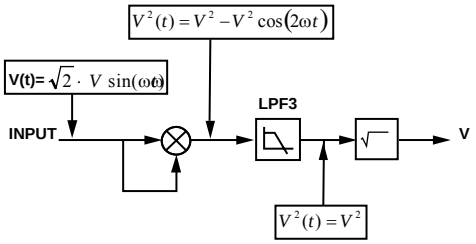


Figure 34. ADE75XX/ADE71XX RMS Signal Processing

The rms signals can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS.

Important: When the current input is larger than 40% of Full scale, the Irms waveform sample register does not represent the true rms value processed. The rms value processed with this level of input is larger than the 24 bit read by the waveform register making the value read truncated on the high end.

Current Channel RMS Calculation

The ADE75XX/ADE71XX simultaneously calculates the rms values for the Current and Voltage channel in different registers. The current channel rms calculation is done on the channel selected by SEL_I_CH bits in the CALMODE register (0x3D). Figure 35 shows the detail of the signal processing chain for the rms calculation on the current channel. The current channel rms value is processed from the samples used in the current channel waveform sampling mode. The current channel rms value is stored in an unsigned 24-bit register (IRMS). One LSB of the current channel rms register is equivalent to one LSB of a current channel waveform sample.

The update rate of the current channel rms measurement is MCLK/5. To minimize noise in the reading of the register, the Irms register can also be configured to be updated only with the zero crossing of the voltage input. This configuration is done by setting ZXRMS bit in the MODE2 register (0x0C).

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±0d2,684,354—see the Current Channel ADC section. The equivalent rms value of a full-scale ac signal is 0d1,898,124 (0x1CF68C). The current rms measurement provided in the ADE75XX/ADE71XX is accurate to within 0.5% for signal input between full scale and full scale/1000. The conversion from the register value to amps must be done externally in the microprocessor using an amps/LSB constant.

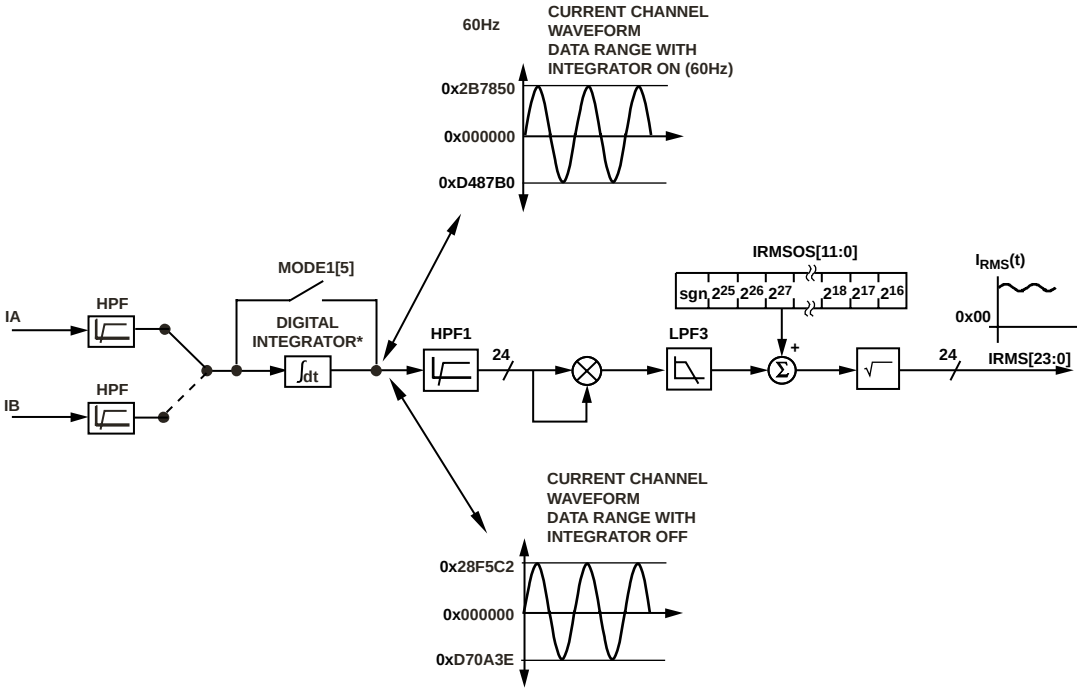


Figure 35. Current channel RMS Signal Processing

Current channel RMS Offset Compensation

The ADE75XX/ADE71XX incorporates a current channel rms offset compensation register (IRMSOS). This is a 12-bit signed register that can be used to remove offset in the current channel rms calculation. An offset could exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The offset calibration allows the content of the IRMS register to be maintained at 0 when no input is present on current channel.

One LSB of the current channel rms offset is equivalent to 16,384 LSB of the square of the current channel rms register. Assuming that the maximum value from the current channel rms calculation is 0d1,898,124 with full-scale ac inputs, then 1

LSB of the current channel rms offset represents 0.23% of measurement error at –60 dB down of full scale.

$$IRMS = \sqrt{IRMS_0^{\,2} + IRMSOS \times 32768} \quad (4)$$

where $IRMS_0$ is the rms measurement without offset correction.

Voltage channel RMS Calculation

Figure 36 shows the details of the signal processing chain for the rms calculation on Voltage channel. The Voltage channel rms value is processed from the samples used in the Voltage channel waveform sampling mode. Voltage channel rms value is stored in the unsigned 24-bit VRMS register.

The update rate of the Voltage channel rms measurement is MCLK/5. To minimize noise in the reading of the register, the Vrms register can also be configured to be updated only with the zero crossing of the voltage input. This configuration is done by setting ZXRMS bit in the MODE2 register (0x0C).

With the specified full-scale ac analog input signal of 0.5 V, the output from the LPF1 swings between 0x28F5 and 0xD70B at 60 Hz—see the Voltage Channel ADC section. The equivalent rms value of this full-scale ac signal is approximately 0d1,898,124 (0x1CF68C) in the VRMS register. The voltage rms measurement provided in the ADE75XX/ADE71XX is accurate to within ±0.5% for signal input between full scale and full scale/20. The conversion from the register value to volts must be done externally in the microprocessor using a volts/LSB constant.

Voltage channel RMS Offset Compensation

The ADE75XX/ADE71XX incorporates a voltage channel rms offset compensation register (VRMSOS). This is a 12-bit signed register that can be used to remove offset in the voltage channel rms calculation. An offset could exist in the rms calculation due to input noises and dc offset in the input samples. The offset calibration allows the contents of the VRMS register to be maintained at 0 when no voltage is applied. One LSB of the voltage channel rms offset is equivalent to 64 LSB of the rms register. Assuming that the maximum value from the voltage channel rms calculation is 0d1,898,124 with full-scale ac inputs, then one LSB of the voltage channel rms offset represents 3.37% of measurement
error at –60 dB down of full scale.

$$VRMS = VRMS_0 + 64 \text{ x } VRMSOS \quad (6)$$

where $VRMS_0$ is the rms measurement without offset correction.

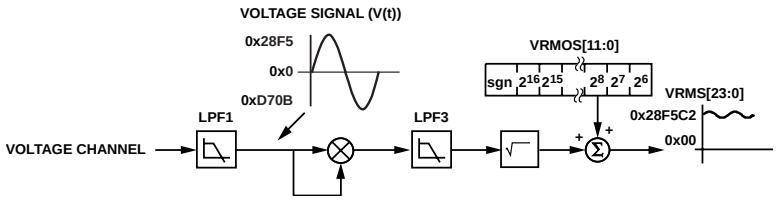


Figure 36. Voltage channel RMS Signal Processing

ACTIVE POWER CALCULATION

Active power is defined as the rate of energy flow from source to load. It is defined as the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 9 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2} \times V \sin(\omega t) \quad (7)$$

$$i(t) = \sqrt{2} \times I \sin(\omega t) \quad (8)$$

where:

V is the rms voltage.
I is the rms current.

$$p(t) = v(t) \times i(t)$$

$$p(t) = VI - VI\cos(2\omega t) \quad (9)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 10.

$$P = \frac{1}{nT}\int_0^{nT} p(t)dt = VI \quad (10)$$

where:

T is the line cycle period.
P is referred to as the active or real power.

Note that the active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 9, i.e., VI. This is the relationship used to calculate active power in the ADE75XX/ADE71XX. The instantaneous power signal $p(t)$ is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. This process is illustrated in Figure 37.

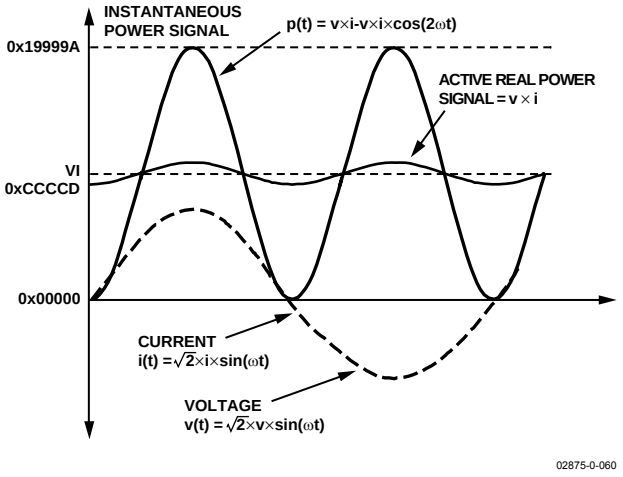


Figure 37. Active Power Calculation

Since LPF2 does not have an ideal "brick wall" frequency response—see Figure 38, the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated to calculate energy—see the Active Energy Calculation section.

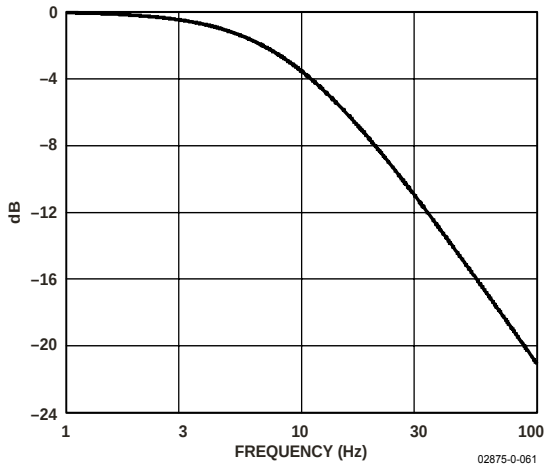


Figure 38. Frequency Response of LPF2

Active power gain calibration

Figure 39 shows the signal processing chain for the active power calculation in the ADE75XX/ADE71XX. As explained, the active power is calculated by low-pass filtering the instantaneous power signal. Note that when reading the waveform samples from the output of LPF2, the gain of the active energy can be adjusted by using the multiplier and watt gain register (WGAIN[11:0]). The gain is adjusted by writing a twos complement 12-bit word to the watt gain register. Equation 11 shows how the gain adjustment is related to the contents of the watt gain register:

$$Output\ WGAIN = \left(Active\ Power \times \left\{ 1 + \frac{WGAIN}{2^{12}} \right\} \right) \quad (11)$$

For example, when 0x7FF is written to the watt gain register, the power output is scaled up by 50%. 0x7FF = 2047d, $2047/2^{12}$ = 0.5. Similarly, 0x800 = –2048d (signed twos complement) and power output is scaled by –50%. Each LSB scales the power output by 0.0244%. The minimum output range is given when the watt gain register contents are equal to 0x800, and the maximum range is given by writing 0x7FF to the watt gain register. This can be used to calibrate the active power (or energy) calculation in the ADE75XX/ADE71XX.

Active power offset calibration

The ADE75XX/ADE71XX also incorporates an active power offset register (WATTOS[15:0]). This is a signed twos complement 16-bit register that can be used to remove offsets in the active power calculation—see Figure 37. An offset could exist in the power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed.

The 256 LSBs (WATTOS = 0x0100) written to the active power offset register are equivalent to 1 LSB in the waveform sample register. Assuming the average value, output from LPF2 is 0xCCCCD (838,861d) when inputs on the voltage and current channels are both at full scale. At –60 dB down on the current channel (1/1000 of the current channel full-scale input), the average word value output from LPF2 is 838.861 (838,861/1,000). One LSB in the LPF2 output has a measurement error of 1/838.861 × 100% = 0.119% of the average value. The active power offset register has a resolution equal to 1/256 LSB of the waveform register, therefore the power offset correction resolution is 0.000464%/LSB (0.119%/256) at –60 dB.

Active power sign detection

The ADE75XX/ADE71XX detects a change of sign in the active power. A sign change can be monitored on the filtered active power signal or on a per CF pulse basis, depending on the configuration of the CFSIGN_OPT bit in the GAIN register (0x1B). The APSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) record when a change of sign according to bit APSIGN in the ACCMODE register (0x0F) has occurred. If the APSIGN bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APSIGN status bit is cleared—see Energy measurement interrupts section.

When APSIGN in the ACCMODE register (0x0F) is cleared (default), the APSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when a transition from positive to negative active power has occurred.

When APSIGN in the ACCMODE register (0x0F) is set, the APSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when a transition from negative to positive active power has occurred.

Active power no-Load detection

The ADE75XX/ADE71XX includes a no-load threshold feature on the active energy that eliminates any creep effects in the meter. The ADE75XX/ADE71XX accomplishes this by not accumulating energy if the multiplier output is below the no-load threshold. When the active power is below the no-load threshold, the APNOLOAD flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set. If the APNOLOAD bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APNOLOAD status bit is cleared—see Energy measurement interrupts section.

The No-load threshold level is selectable by setting bits APNOLOAD in the NLMODE register (0x0E). Setting these bits to 0b00 disable the no-load detection and setting them to 0b01, 0b10 or 0b11 set the no-load detection threshold to 0.015%, 0.0075% and 0.0037% of the full-scale output frequency of the multiplier respectively. The IEC62053-21 specification, states that the meter must start up with a load equal to or less than 0.4% Ib. If the nominal voltage input and the maximum current represent 50% of the full scale ADC input and Imax = 400% of Ib, the ADE75XX/ADE71XX no-load threshold options translate to 0.24% of Ib, 0.12% of Ib and 0.06% of Ib respectively.

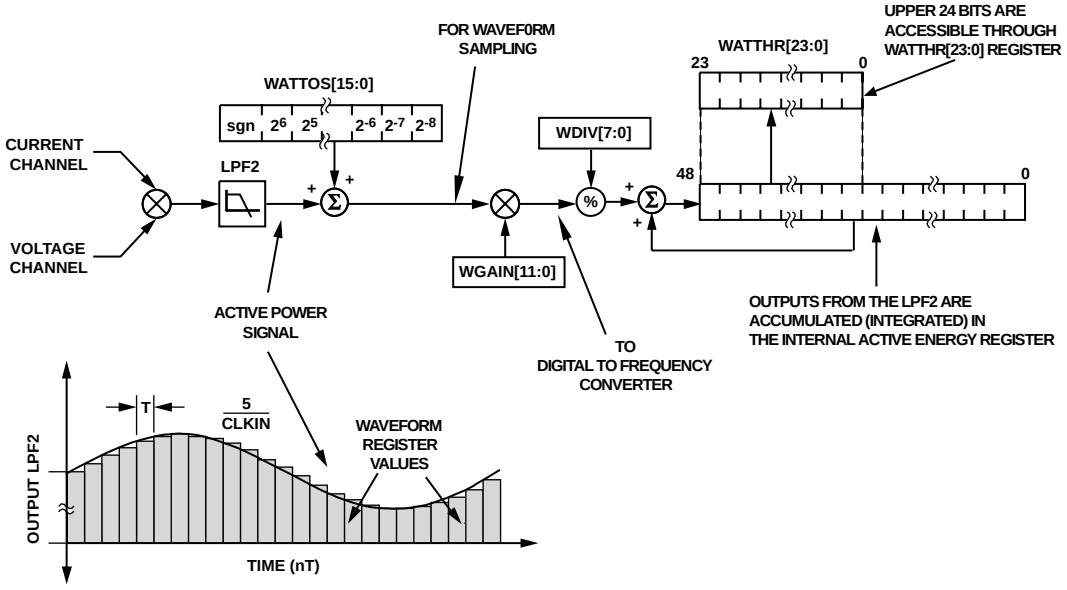


Figure 39. ADE75XX/ADE71XX Active Energy Calculation

Active Energy Calculation

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically in Equation 12.

$$P = \frac{dE}{dt} \tag{12}$$

where:

P is power.
E is energy.

Conversely, energy is given as the integral of power.

$$E = \int P dt \tag{13}$$

The ADE75XX/ADE71XX achieves the integration of the active power signal by continuously accumulating the active power signal in an internal non-readable 49-bit energy register. The active energy register (WATTHR[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 14 expresses the relationship.

$$E = \int p(t)dt = \underset{t \to 0}{Lim} \left\{ \sum_{n=1}^{\infty} p(nT) \times T \right\} \tag{14}$$

where:

n is the discrete time sample number.
T is the sample period.

The discrete time sample period (*T*) for the accumulation register in the ADE75XX/ADE71XX is 1.22µs (5/MCLK). As

well as calculating the energy, this integration removes any sinusoidal components that might be in the active power signal. Figure 39 shows this discrete time integration or accumulation. The active power signal in the waveform register is continuously added to the internal active energy register.

The Active Energy accumulation depends on the setting of the POAM and ABSAM bits in the ACCMODE register (0x0F). When both bits are cleared, the addition is signed and therefore negative energy is subtracted from the active energy contents. When both bits are set, the ADE75XX/ADE71XX is set to be in the more restrictive mode, the Positive Only Accumulation mode.

When POAM bit in the ACCMODE register (0x0F) is set, only positive power contributes to the active energy accumulation — see the Watt positive-only accumulation mode section.

When ABSAM bit in the ACCMODE register (0x0F) is set, the absolute active power is used for the active energy accumulation — see the Watt absolute accumulation mode section.

The output of the multiplier is divided by WDIV. If the value in the WDIV register is equal to 0, then the internal active energy register is divided by 1. WDIV is an 8-bit unsigned register. After dividing by WDIV, the active energy is accumulated in a 49-bit internal energy accumulation register. The upper 24 bits of this register are accessible through a read to the active energy register (WATTHR[23:0]). A read to the RWATTHR register returns the content of the WATTHR register and the upper 24 bits of the internal register are cleared. As shown in Figure 39, the active power signal is accumulated in an internal 49-bit signed register. The active power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS.

Figure 40 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three curves displayed illustrate the minimum period of time it takes the energy register to roll over when the active power gain register contents are 0x7FF, 0x000, and 0x800. The watt gain register is used to carry out power calibration in the ADE75XX/ADE71XX. As shown, the fastest integration time occurs when the watt gain register is set to maximum full scale, i.e., 0x7FF.

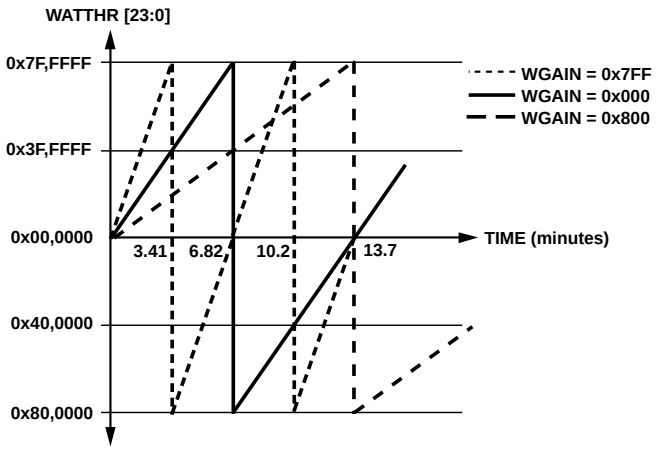


Figure 40. Energy Register Rollover Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the energy register contents rolls over to full-scale negative (0x800000) and continues to increase in value when the power or energy flow is positive—see Figure 40. Conversely, if the power is negative, the energy register underflows to full-scale positive (0x7FFFFF) and continues to decrease in value.

By using the interrupt enable register, the ADE75XX/ADE71XX can be configured to issue an ADE interrupt to the 8052 core when the active energy register is half-full (positive or negative) or when an overflow or underflow occurs.

Integration time under steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/CLKIN). With full-scale sinusoidal signals on the analog inputs and the WGAIN register set to 0x000, the average word value from each LPF2 is 0xCCCCD—see Figure 37. The maximum positive value that can be stored in the internal 49-bit register is 2^{48} or 0xFFFF,FFFF,FFFF before it overflows. The integration time under these conditions with WDIV = 0 is calculated as follows:

$$Time = \frac{0\,\text{xFFFF,FFFF,FFFF}}{0\,\text{xCCCCD}} \times 1.22\ \mu\text{s} = 409.6\ \text{s} = 6.82\ \text{min} \quad (15)$$

When WDIV is set to a value different from 0, the integration time varies, as shown in Equation 16.

$$Time = Time_{WDIV=0} \times WDIV \quad (16)$$

Active energy accumulation modes

Watt signed accumulation mode

The ADE75XX/ADE71XX active energy default accumulation mode is a signed accumulation based on the active power information.

Watt positive-only accumulation mode

The ADE75XX/ADE71XX is placed in positive-only accumulation mode by setting the POAM bit in the

ACCMODE register (0x0F). In positive-only accumulation mode, the energy accumulation is done only for positive power, ignoring any occurrence of negative power above or below the no-load threshold, as shown in Figure 41. The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Detection of the transitions in the direction of power flow, and no-load threshold are active in this mode.

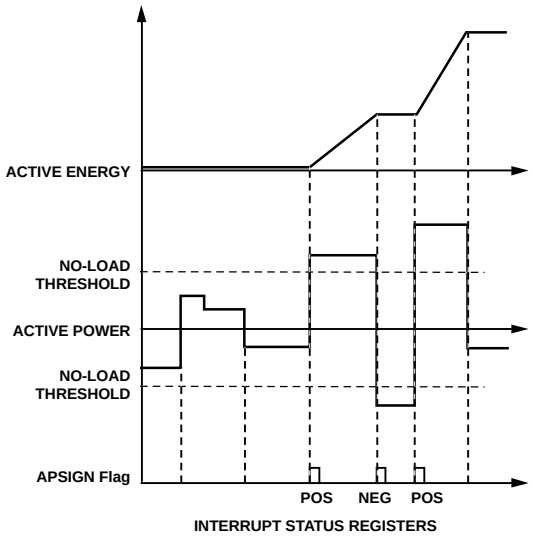


Figure 41. Energy Accumulation in Positive-Only Accumulation Mode

Watt absolute accumulation mode

The ADE75XX/ADE71XX is placed in absolute accumulation mode by setting the ABSAM bit in the ACCMODE register (0x0F). In absolute accumulation mode, the energy accumulation is done using the absolute active power, ignoring any occurrence of power below the no-load threshold, as shown in Figure 42. The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Detection of the transitions in the direction of power flow, and no-load threshold are active in this mode.

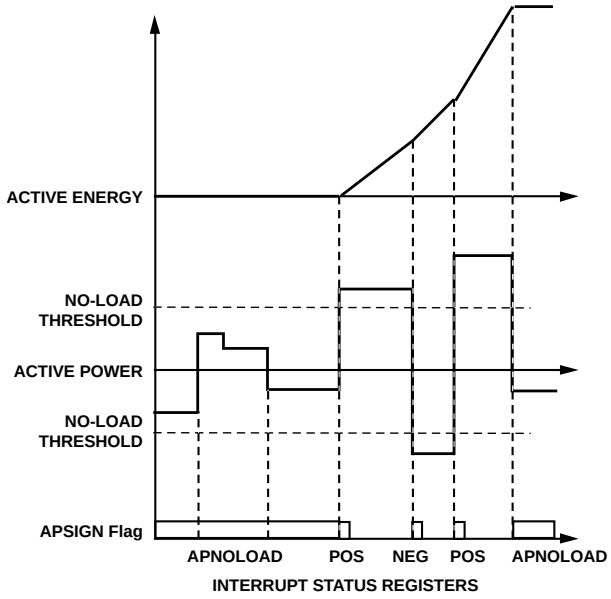


Figure 42. Energy Accumulation in Absolute Accumulation Mode

Active energy Pulse output

ADE75XX/ADE71XX also provides all the circuitry to have a pulse output that frequency is proportional to Active power – see Active Power Calculation section. This pulse frequency output uses the calibrated signal after WGAIN and its behavior is consistent with the setting of the active energy accumulation mode in the ACCMODE register (0x0F). The pulse output is active low and should be preferably connected to an LED as shown on *Figure 53*.

Line cycle active energy accumulation mode

In line cycle energy accumulation mode, the energy accumulation of the ADE75XX/ADE71XX can be synchronized to the voltage channel zero crossing so that active energy can be accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and in a shorter time because the integration period can be shortened. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation mode, the ADE75XX/ADE71XX accumulates the active power signal in the LWATTHR register for an integral number of line cycles, as shown in Figure 44. The number of half line cycles is specified in the LINCYC register. The ADE75XX/ADE71XX can accumulate active power for up to 65,535 half line cycles. Because the active power is integrated on an integral number of line cycles, at the end of a line cycle energy accumulation cycle the CYCEND flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE) is set. If the CYCEND enable bit in the Interrupt Enable Register 3 SFR (MIRQENH,

0xDB) is set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CYCEND status bit is cleared—see Energy measurement interrupts section. Another calibration cycle will start as soon as the CYCEND flag is set. If the LWATTHR register is not read before a new CYCEND flag is set, the LWATTHR register will be overwritten by a new value.

When a new half line cycles is written in LINECYC register, the LWATTHR register is reset and a new accumulation start at the next zero-crossing. The number of half line cycles is then counted until LINCYC is reached . This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register – see Figure 43. The line active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two registers is equivalent.

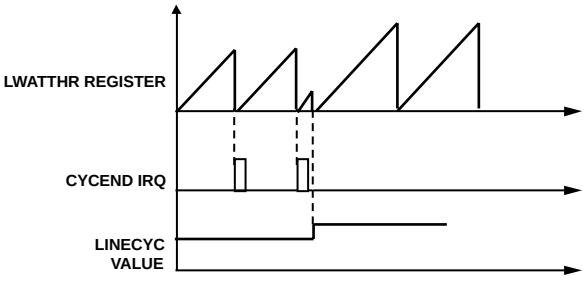


Figure 43. Energy Accumulation when LINECYC changed

From Equations 13 and 18,

$$E(t) = \int_0^{nT} VI\,dt - \left\{ \frac{VI}{\sqrt{1+\left(\frac{f}{8.9}\right)^2}} \right\} \int_0^{nT} \cos(2\pi ft)\,dt \quad (20)$$

where:

n is an integer.
T is the line cycle period.

Since the sinusoidal component is integrated over an integer number of line cycles, its value is always 0. Therefore,

$$E = \int_0^{nT} VI\,dt + 0 \quad (21)$$

$$E(t) = VInT \quad (22)$$

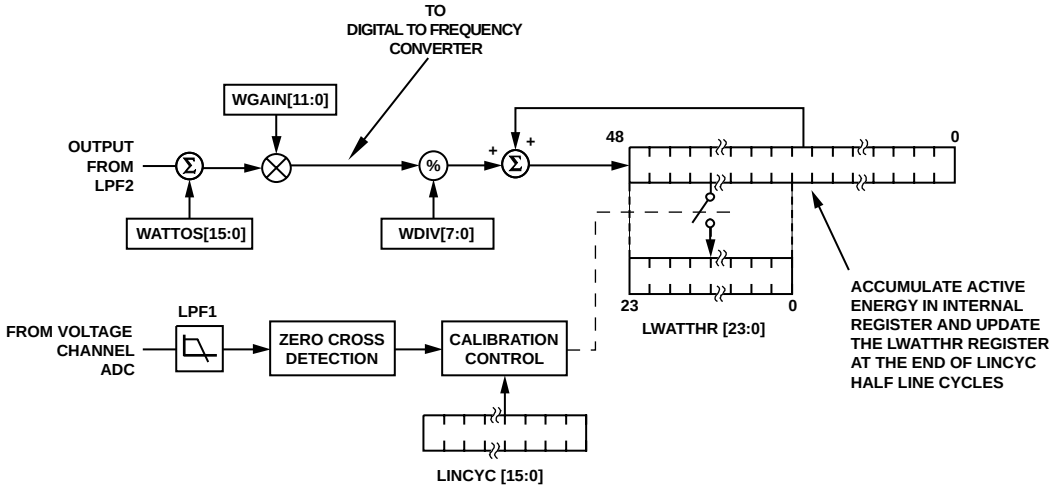


Figure 44. Line Cycle Active Energy Accumulation

Note that in this mode, the 16-bit LINCYC register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration over 65,535 half line cycles. At 60 Hz line frequency, it translates to a total duration of 65,535/120 Hz = 546 seconds.

REACTIVE POWER CALCULATION[15]

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase-shifted by 90°. The resulting waveform is called the instantaneous reactive power signal. Equation 25 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sqrt{2}V \sin(\omega t + \theta) \quad (23)$$
$$i(t) = \sqrt{2}I \sin(\omega t)$$

$$i'(t) = \sqrt{2}\ I \sin\left(\omega t + \frac{\pi}{2}\right) \quad (24)$$

where:

θ is the phase difference between the voltage and current channel.
V is the rms voltage.
I is the rms current.

$$q(t) = v(t) \times i'(t) \quad (25)$$

$$q(t) = VI \sin(\theta) + VI \sin(2\omega t + \theta)$$

The average reactive power over an integral number of lines (n) is given in Equation 26.

$$Q = \frac{1}{nT}\int_0^{nT} q(t)dt = VI \sin(\theta) \quad (26)$$

where:

T is the line cycle period.
q is referred to as the reactive power.

Note that the reactive power is equal to the dc component of the instantaneous reactive power signal q*(t)* in Equation 25. This is the relationship used to calculate reactive power in the ADE75XX/ADE71XX. The instantaneous reactive power signal q*(t)* is generated by multiplying Voltage and Current channels. In this case, the phase of Current channel is shifted by +90°. The dc component of the instantaneous reactive power signal is then extracted by a low-pass filter in order to obtain the reactive power information – see Figure 45.

In addition, the phase shifting filter has a non-unity magnitude response. Because the phase-shift filter has a large attenuation at high frequency, the reactive power is primarily for the calculation at line frequency. The effect of harmonics is largely ignored in the reactive power calculation. Note that because of the magnitude characteristic of the phase shifting filter, the weight of the reactive power is slightly different from the active power calculation – see Energy register scaling.

The frequency response of the LPF in the reactive signal path is identical to that of the LPF2 used in the average active power calculation. Since LPF2 does not have an ideal "brick wall" frequency response—see Figure 38, the reactive power signal has some ripple due to the instantaneous reactive power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the reactive power signal is integrated to calculate energy—see the Reactive Power Calculation section.

The reactive power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS.

Reactive gain automatic compenstation

The ADE75XX/ADE71XX reactive power calculation has a 20dB/decade attenuation over frequency. In order to attenuate this effect for the line frequency, the ADE75XX/ADE71XX has a dynamic compensation of the line frequency to maintain a constant gain over the fundamental line frequency between 45 and 65Hz. However, this automatic compensation can be disabled by setting bit 7 of the NLMODE register (0x0E).

Reactive power gain calibration

Figure 45 shows the signal processing chain for the reactive power calculation in the ADE75XX/ADE71XX. As explained, the reactive power is calculated by low-pass filtering the instantaneous reactive power signal. Note that when reading the waveform samples from the output of LPF2, the gain of the reactive energy can be adjusted by using the multiplier and var gain register (VARGAIN[11:0]). The gain is adjusted by writing a twos complement 12-bit word to the var gain register. Equation 11 shows how the gain adjustment is related to the contents of the watt gain register:

$$Output\ VARGAIN = \left(\text{Re}\,active\ Power \times \left\{1 + \frac{VARGAIN}{2^{12}}\right\}\right) \quad (11)$$

The resolution of the VARGAIN register is the same as the WGAIN register – see Active power gain calibration section. VARGAIN can be used to calibrate the reactive power (or energy) calculation in the ADE75XX/ADE71XX.

Reactive power offset calibration

The ADE75XX/ADE71XX also incorporates a reactive power offset register (VAROS[15:0]). This is a signed twos complement 16-bit register that can be used to remove offsets in the reactive power calculation—see Figure 45. An offset could exist in the reactive power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the reactive power register to be

[15] This function is not available in ADE7566 and ADE7166products

maintained at 0 when no power is being consumed.

The 256 LSBs (VAROS = 0x100) written to the reactive power offset register are equivalent to 1 LSB in the waveform sample register.

Sign of Reactive Power Calculation

Note that the average reactive power is a signed calculation. The phase shift filter has –90° phase shift when the integrator is enabled, and +90° phase shift when the integrator is disabled. Table 42 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting VAR calculation.

Table 42. Sign of Reactive Power Calculation

Angle	Integrator	Sign
Between 0° to 90°	Off	Positive
Between –90° to 0°	Off	Negative
Between 0° to 90°	On	Positive
Between –90° to 0°	On	Negative

Reactive power sign detection

The ADE75XX/ADE71XX detects a change of sign in the reactive power. A sign change can be monitored on the filtered reactive power signal or on a per CF pulse basis, depending on the configuration of the CFSIGN_OPT bit in the GAIN register (0x1B). The VARSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) record when a change of sign according to bit VARSIGN in the ACCMODE register (0x0F) has occurred. If the VARSIGN bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the VARSIGN status bit is cleared—see Energy measurement interrupts section.

When VARSIGN in the ACCMODE register (0x0F) is cleared (default), the VARSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when a transition from positive to negative reactive power has occurred.

When VARSIGN in the ACCMODE register (0x0F) is set, the VARSIGN flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) will be set when a transition from negative to positive reactive power has occurred.

Reactive power no-Load detection

The ADE75XX/ADE71XX includes a no-load threshold feature on the reactive energy that eliminates any creep effects in the meter. The ADE75XX/ADE71XX accomplishes this by not accumulating reactive energy if the multiplier output is below the no-load threshold. When the reactive power is below the no-load threshold, the RNOLOAD flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set. If the RNOLOAD bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the RNOLOAD status bit is cleared—see Energy measurement interrupts section.

The No-load threshold level is selectable by setting bits RNOLOAD in the NLMODE register (0x0E). Setting these bits to 0b00 disable the no-load detection and setting them to 0b01, 0b10 or 0b11 set the no-load detection threshold to 0.015%, 0.0075% and 0.0037% of the full-scale output frequency of the multiplier respectively.

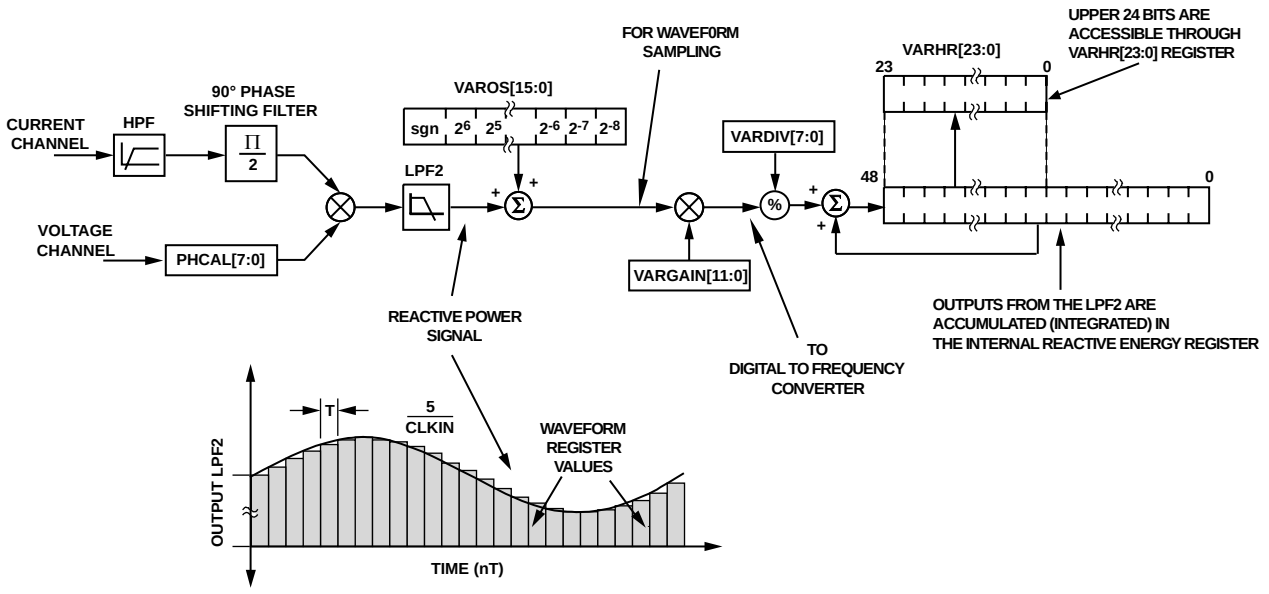


Figure 45. ADE75XX/ADE71XX Reactive Energy Calculation

Reactive Energy Calculation

As for active energy, the ADE75XX/ADE71XX achieves the integration of the reactive power signal by continuously accumulating the reactive power signal in an internal non-readable 49-bit energy register. The reactive energy register (VARHR[23:0]) represents the upper 24 bits of this internal register.

The discrete time sample period (*T*) for the accumulation register in the ADE75XX/ADE71XX is 1.22µs (5/MCLK). As well as calculating the energy, this integration removes any sinusoidal components that might be in the active power signal. Figure 45 shows this discrete time integration or accumulation. The reactive power signal in the waveform register is continuously added to the internal reactive energy register.

The reactive Energy accumulation depends on the setting of the SAVARM and ABSVARM bits in the ACCMODE register (0x0F). When both bits are cleared, the addition is signed and therefore negative energy is subtracted from the reactive energy contents. When both bits are set, the ADE75XX/ADE71XX is set to be in the more restrictive mode, the Absolute Accumulation mode.

When SAVARM bit in the ACCMODE register (0x0F) is set, the reactive power is accumulated depending on the sign of the active power. When active power is positive, the reactive power is added as it is to the reactive energy register. When active power is negative, the reactive power is subtracted to the reactive energy accumulator – see VAR anti-tamper accumulation mode.

When ABSVARM bit in the ACCMODE register (0x0F) is set, the absolute reactive power is used for the reactive energy accumulation—see the VAR absolute accumulation mode section.

The output of the multiplier is divided by VARDIV. If the value in the VARDIV register is equal to 0, then the internal reactive energy register is divided by 1. VARDIV is an 8-bit unsigned register. After dividing by VARDIV, the reactive energy is accumulated in a 49-bit internal energy accumulation register. The upper 24 bits of this register are accessible through a read to the reactive energy register (VARHR[23:0]). A read to the RVARHR register returns the content of the VARHR register and the upper 24 bits of the internal register are cleared. As shown in Figure 45, the reactive power signal is accumulated in an internal 49-bit signed register. The reactive power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS.

Figure 40 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. These curves also apply for the reactive energy accumulation

Note that the energy register contents rolls over to full-scale negative (0x800000) and continues to increase in value when the power or energy flow is positive. Conversely, if the power is negative, the energy register underflows to full-scale positive (0x7FFFFF) and continues to decrease in value.

By using the interrupt enable register, the ADE75XX/ADE71XX can be configured to issue an ADE interrupt to the 8052 core when the reactive energy register is half-full (positive or negative) or when an overflow or underflow occurs.

Integration time under steady Load

As mentioned in the active energy section, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/CLKIN). With full-scale sinusoidal signals on the analog inputs and the VARGAIN and VARDIV registers set to 0x000, the integration time before the reactive energy register overflows is calculated as follows:

$$Time = \frac{0\,\text{xFFFF,FFFF,FFFF}}{0\,\text{xCCCCD}} \times 1.22\ \mu\text{s} = 409.6\ \text{s} = 6.82\ \text{min} \quad (15)$$

When VARDIV is set to a value different from 0, the integration time varies, as shown in Equation 16.

$$Time = Time_{WDIV=0} \times VARDIV \quad (16)$$

Reactive energy accumulation modes

VAR signed accumulation mode

The ADE75XX/ADE71XX reactive energy default accumulation mode is a signed accumulation based on the reactive power information.

VAR anti-tamper accumulation mode

The ADE75XX/ADE71XX is placed in VAR anti-tamper accumulation mode by setting the SAVARM bit in the ACCMODE register (0x0F). In this mode, the reactive power is accumulated depending on the sign of the active power. When active power is positive, the reactive power is added as it is to the reactive energy register. When active power is negative, the reactive power is subtracted to the reactive energy accumulator – see Figure 46. The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Transitions in the direction of power flow, and no-load threshold are active in this mode.

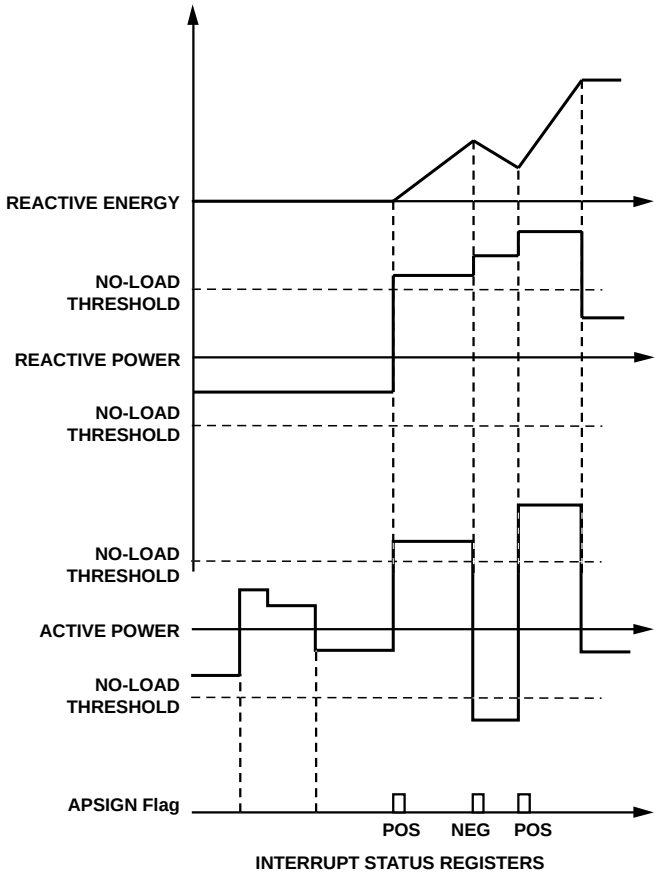


Figure 46. Reactive Energy Accumulation in Anti-tamper Accumulation Mode

VAR absolute accumulation mode

The ADE75XX/ADE71XX is placed in absolute accumulation mode by setting the ABSVARM bit in the ACCMODE register (0x0F). In absolute accumulation mode, the reactive energy accumulation is done using the absolute reactive power, ignoring any occurrence of power below the no-load threshold, as shown in Figure 42 for the active energy. The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Transitions in the direction of power flow, and no-load threshold are active in this mode.

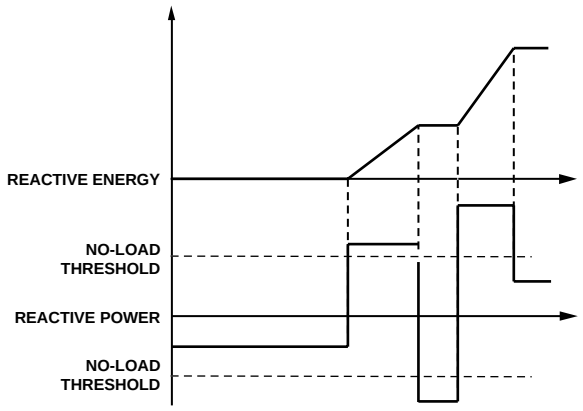


Figure 47. Reactive Energy Accumulation in Absolute Accumulation Mode

Reactive energy Pulse output

ADE75XX/ADE71XX also provides all the circuitry to have a pulse output those frequency is proportional to reactive power – see Energy-to-Frequency Conversion section. This pulse frequency output uses the calibrated signal after VARGAIN and its behavior is consistent with the setting of the reactive energy accumulation mode in the ACCMODE register (0x0F). The pulse output is active low and should be preferably connected to an LED as shown on *Figure 53*.

Line cycle reactive energy accumulation mode

In line cycle energy accumulation mode, the energy accumulation of the ADE75XX/ADE71XX can be synchronized to the voltage channel zero crossing so that reactive energy can be accumulated over an integral number of half line cycles. The advantage of this mode is similar to the ones explained in the Active energy Line cycle accumulation mode – see Line cycle active energy accumulation mode section. In line cycle energy accumulation mode, the ADE75XX/ADE71XX accumulates the reactive power signal in the LVARHR register for an integral number of line cycles, as shown in Figure 48. The number of half line cycles is specified in the LINCYC register. The ADE75XX/ADE71XX can accumulate active power for up to 65,535 half line cycles. Because the reactive power is integrated on an integral number of line cycles, at the end of a line cycle energy accumulation cycle the CYCEND flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE). If the CYCEND enable bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CYCEND status bit is cleared—see Energy measurement interrupts section. Another calibration cycle will start as soon as the CYCEND flag is set. If the LVARHR register is not read before a new CYCEND flag is set, the LVARHR register will be overwritten by a new value.

As for LWATTHR, when a new half line cycles is written in LINCYC register, the LVARHR register is reset and a new accumulation start at the next zero-crossing. The number of half line cycles is then counted until LINCY is reached. This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register. The line reactive energy accumulation uses the same signal path as the reactive energy accumulation. The LSB size of these two registers is equivalent.

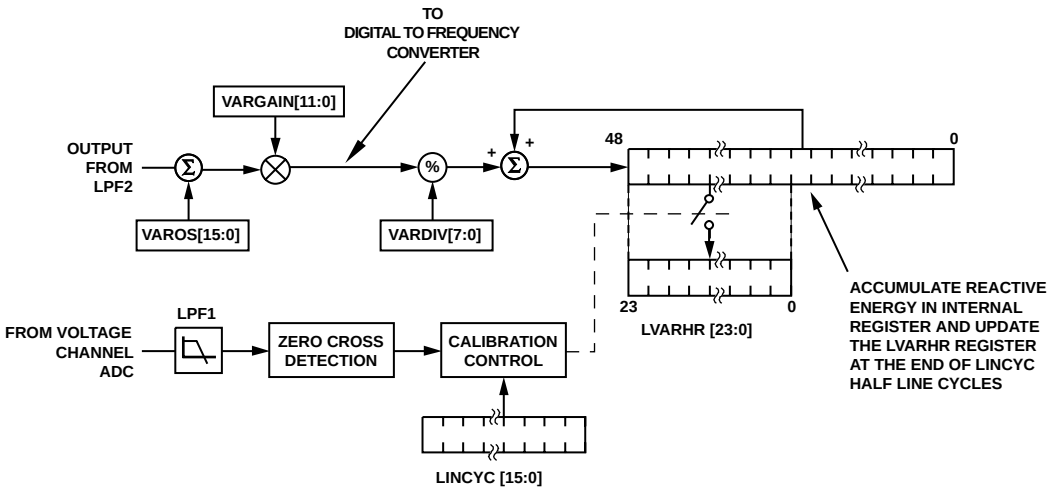


Figure 48 Line Cycle . Reactive Energy Accumulation Mode

APPARENT POWER CALCULATION

The apparent power is defined as the maximum power that can be delivered to a load. V_{rms} and I_{rms} are the effective voltage and current delivered to the load; the apparent power (AP) is defined as $V_{rms} \times I_{rms}$. Equation 28 gives an expression of the instantaneous power signal in an ac system with a phase shift.

$$v(t) = \sqrt{2}\, V_{rms} \sin(\omega t)$$

$$i(t) = \sqrt{2}\, I_{rms} \sin(\omega t + \theta) \quad (27)$$

$$p(t) = v(t) \times i(t)$$

$$p(t) = V_{rms} I_{rms} \cos(\theta) - V_{rms} I_{rms} \cos(2\omega t + \theta) \quad (28)$$

The apparent power is defined as $V_{rms} \times I_{rms}$. This expression is independent from the phase angle between the current and the voltage.

Figure 49 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE75XX/ADE71XX.

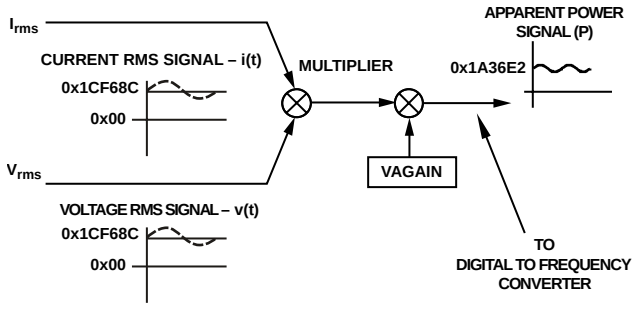


Figure 49. Apparent Power Signal Processing

The apparent power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform date is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS.

The gain of the apparent energy can be adjusted by using the multiplier and VAGAIN register (VAGAIN[11:0]). The gain is adjusted by writing a twos complement, 12-bit word to the VAGAIN register. Equation 29 shows how the gain adjustment is related to the contents of the VAGAIN register.

$$OutputVAGAIN = \left(Apparent\ Power \times \left\{ 1 + \frac{VAGAIN}{2^{12}} \right\} \right) \quad (29)$$

For example, when 0x7FF is written to the VAGAIN register, the power output is scaled up by 50%. 0x7FF = 2047d, $2047/2^{12}$ = 0.5. Similarly, 0x800 = –2047d (signed twos complement) and power output is scaled by –50%. Each LSB represents 0.0244% of the power output. The apparent power is calculated with the current and voltage rms values obtained in the rms blocks of the ADE75XX/ADE71XX.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value—see Current Channel RMS Calculation and Voltage channel RMS Calculation sections. The voltage and current channels rms values are then multiplied together in the apparent power signal processing. Since no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement is done by calibrating each individual rms measurement.

Apparent Energy Calculation

The apparent energy is given as the integral of the apparent power.

$$Apparent\ Energy = \int Apparent\ Power(t)\ dt \quad (30)$$

The ADE75XX/ADE71XX achieves the integration of the apparent power signal by continuously accumulating the apparent power signal in an internal 48-bit register. The apparent energy register (VAHR[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 31 expresses the relationship

$$Apparent\ Energy = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} Apparent\ Power(nT) \times T \right\} \quad (31)$$

where:

n is the discrete time sample number.
T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE75XX/ADE71XX is 1.22 µs (5/MCLK).

Figure 50 shows this discrete time integration or accumulation. The apparent power signal is continuously added to the internal register. This addition is a signed addition even if the apparent energy remains theoretically always positive.

The 49 bits of the internal register are divided by VADIV. If the value in the VADIV register is 0, then the internal apparent energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24 bits are then written in the 24-bit apparent energy register (VAHR[23:0]). RVAHR register (24 bits long) is provided to read the apparent energy. This register is reset to 0 after a read operation.

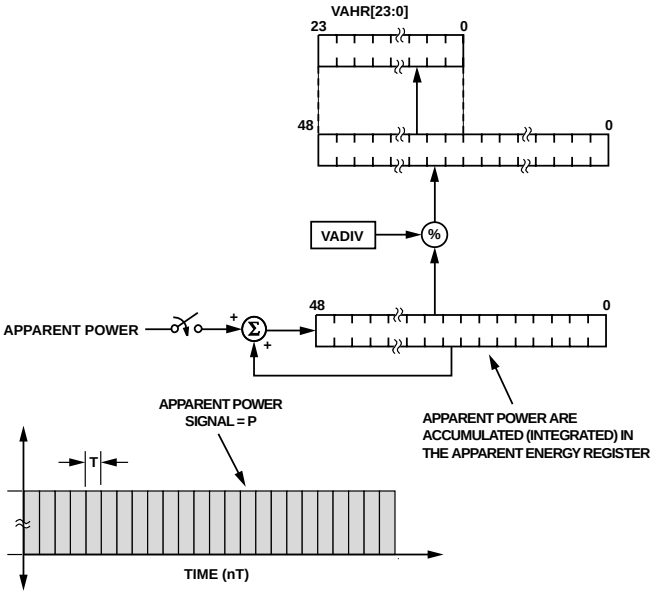


Figure 50. ADE75XX/ADE71XX Apparent Energy Calculation

Note that the apparent energy register is unsigned. By setting the VAEHF and VAEOF bits in the Interrupt Enable Register 2 SFR (MIRQENM, 0xDA), the ADE75XX/ADE71XX can be configured to issue an ADE interrupt to the 8052 core when the apparent energy register is half full or when an overflow occurs. The half full interrupt for the unsigned apparent energy register is based on 24 bits as opposed to 23 bits for the signed active energy register.

Integration Times under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/MCLK). With full-scale sinusoidal signals on the analog inputs and the VAGAIN register set to 0x000, the average word value from apparent power stage is 0x1A36E2—see the section. The maximum value that can be stored in the apparent energy register before it overflows is 2^{24} or 0xFF,FFFF. The average word value is added to the internal register, which can store 2^{48} or 0xFFFF,FFFF,FFFF before it overflows. Therefore, the integration time under these conditions with VADIV = 0 is calculated as follows:

$$Time = \frac{0\text{xFFFF,FFFF,FFFF}}{0\text{xD055}} \times 1.22\ \mu s = 199\ s = 3.33\ min \quad (32)$$

When VADIV is set to a value different from 0, the integration time varies, as shown in Equation 33.

$$Time = Time_{WDIV=0} \times VADIV \quad (33)$$

Apparent energy Pulse output

ADE75XX/ADE71XX also provides all the circuitry to have a pulse output those frequency is proportional to apparent power – see Energy-to-Frequency Conversion section. This pulse frequency output uses the calibrated signal after VAGAIN. This output can also be used to output a pulse those frequency is proportional to Irms.

The pulse output is active low and should be preferably connected to an LED as shown on *Figure 53*.

Line Apparent Energy Accumulation

The ADE75XX/ADE71XX is designed with a special apparent energy accumulation mode, which simplifies the calibration process.
By using the on-chip zero-crossing detection, the ADE75XX/ADE71XX accumulates the apparent power signal in the LVAHR register for an integral number of half cycles, as shown in Figure 51. The line apparent energy accumulation mode is always active.

The number of half line cycles is specified in the LINCYC register, which is an unsigned 16-bit register. The ADE75XX/ADE71XX can accumulate apparent power for up to 65535 combined half cycles. Because the apparent power is integrated on the same integral number of line cycles as the line

active and reactive energy register, these values can be compared easily. The energies are calculated more accurately because of this precise timing control and provide all the information needed for reactive power and power factor calculation. At the end of an energy calibration cycle, the CYCEND flag in the Interrupt Status Register 3 SFR (MIRQSTH, 0xDE) is set. If the CYCEND enable bit in the Interrupt Enable Register 3 SFR (MIRQENH, 0xDB) is enabled, the 8052 core has a pending ADE interrupt.

As for LWATTHR, when a new half line cycles is written in LINECYC register, the LVAHR register is reset and a new accumulation start at the next zero-crossing. The number of half line cycles is then counted until LINCY is reached. This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register. The line apparent energy accumulation uses the same signal path as the apparent energy accumulation. The LSB size of these two registers is equivalent.

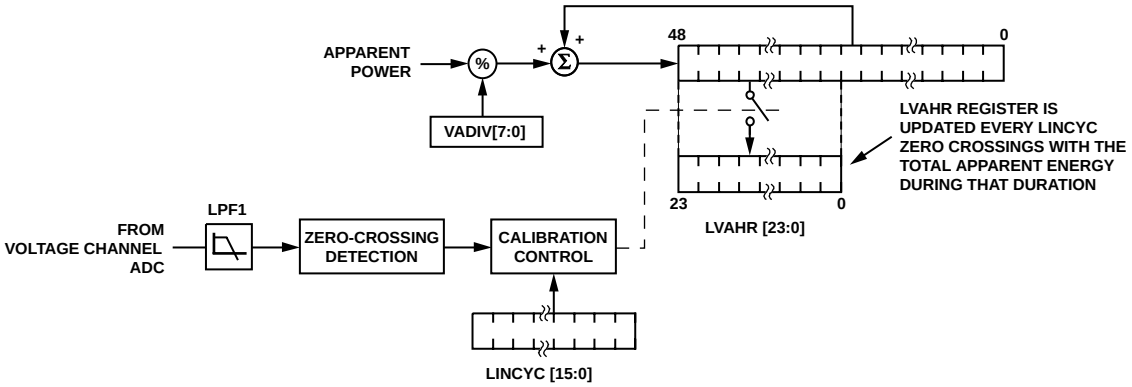


Figure 51. ADE75XX/ADE71XX Line cycle Apparent Energy Accumulation

Apparent power no-Load detection

The ADE75XX/ADE71XX includes a no-load threshold feature on the apparent energy that eliminates any creep effects in the meter. The ADE75XX/ADE71XX accomplishes this by not accumulating energy if the multiplier output is below the no-load threshold. When the apparent power is below the no-load threshold, the VANOLOAD flag in the Interrupt Status Register 1 SFR (MIRQSTL, 0xDC) is set. If the VANOLOAD bit is set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APNOLOAD status bit is cleared—see Energy measurement interrupts section.

The No-load threshold level is selectable by setting bits VANOLOAD in the NLMODE register (0x0E). Setting these bits to 0b00 disable the no-load detection and setting them to 0b01, 0b10 or 0b11 set the no-load detection threshold to 0.030%, 0.015% and 0.0075% of the full-scale output frequency of the multiplier respectively.

This no-load threshold can also be applied to the Irms pulse output when selected. The level of no-load threshold is the same as for the Apparent energy in this case.

ENERGY-TO-FREQUENCY CONVERSION

ADE75XX/ADE71XX also provides two energy-to-frequency conversions for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency, which is proportional to the active, reactive, apparent power or Irms under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 52 illustrates the energy-to-frequency conversion in the ADE75XX/ADE71XX.

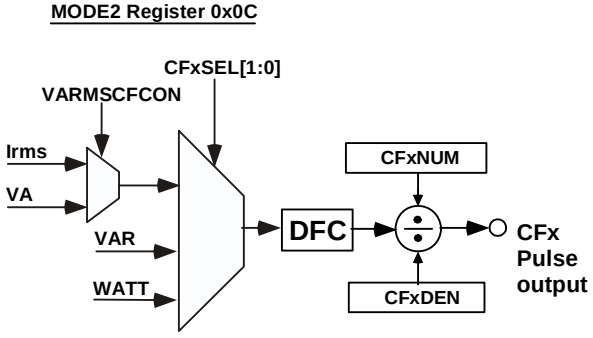


Figure 52. ADE75XX/ADE71XX Energy-to-Frequency Conversion

Two digital-to-frequency converters (DFC) are used to generate

the pulsed outputs. When WDIV =0 or 1, the DFC generates a pulse each time 1 LSB in the energy register is accumulated. An output pulse is generated when CFxDEN/CFxNUM number of pulses are generated at the DFC output. Under steady load conditions, the output frequency is proportional to the active, reactive, Apparent power or Irms depending on the CFxSEL bit in the MODE2 register (0x0C).

Both pulse outputs can be enabled or disabled by clearing or setting respectively bits DISCF1 and DISCF2 in the MODE1 register (0x0B).

Both pulse outputs set a separate flag in the Interrupt Status Register 2 SFR (MIRQSTM, 0xDD), CF1 and CF2. If CF1 and CF2 enable bits in the Interrupt Enable Register 2 SFR (MIRQENM, 0xDA) are set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CF1 or CF2 status bits are cleared—see Energy measurement interrupts section.

Pulse output configuration

The two pulse outputs circuitry have separate configuration bits in the MODE2 register (0x0C). Setting CFxSEL bits to 0b00, 0b01 or 0b1x configure the DFC to create a pulse output proportional to Active power, reactive power, or Apparent/Irms respectively.

The selection between Irms and Apparent power is done by the VARMSCFCON bit in the MODE2 register (0x0C). With this selection, CF2 cannot be proportional to apparent power if CF1 is proportional to Irms and vice-versa.

Pulse output characteristic

The pulse output for both DFC stays low for 90ms if the pulse period is larger than 180ms (5.56Hz). If the pulse period is smaller than 180ms, the duty cycle of the pulse output is 50%. The pulse output is active low and should be preferably connected to an LED as shown on *Figure 53*.

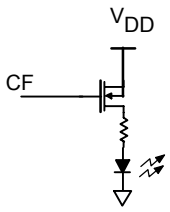


Figure 53. CF Pulse output

The maximum output frequency, with ac input signals at full scale and CFxNUM = 0x00 and CFxDEN = 0x00, is approximately 21.1 kHz.

The ADE75XX/ADE71XX incorporates two registers, CFxNUM[15:0] and CFxDEN[15:0] per DFC, to set the CFx frequency. These are unsigned 16-bit registers, which can be used to adjust the CFx frequency to a wide range of values. These frequency-scaling registers are 16-bit registers, which can scale the output frequency by $1/2^{16}$ to 1 with a step of $1/2^{16}$.

If the value 0 is written to any of these registers, the value 1 would be applied to the register. The ratio CFxNUM / CFxDEN should be smaller than 1 to ensure proper operation. If the ratio of the registers CFxNUM / CFxDEN is greater than 1, the register values would be adjusted to a ratio of 1. For example, if the output frequency is 1.562 kHz while the contents of CFxDEN are 0 (0x000), then the output frequency can be set to 6.1 Hz by writing 0xFF to the CFxDEN register.

ENERGY REGISTER SCALING

The ADE75XX/ADE71XX provides measurements of active, reactive, and apparent energies that use separate paths and filtering for calculation. The difference in data paths can result in small differences in LSB weight between active, reactive and apparent energy registers. These measurements are internally compensated so the scaling is nearly one to one. The relationship between the registers is show in Table 43. In Table 44, the relationship between WATTGAIN, VARGAIN and VAGAIN is given. These relationships can be used for calibration and simplify the adjustment of VAR and VA gains. As VAR and VA gains can be deducted from WGAIN, there is no need to do reactive or apparent gai adjustment.

Table 43. Energy Registers scaling

Line Frequency = 50Hz	**Line Frequency = 60Hz**
Integrator OFF	
VAR = 0.9952 × WATT	VAR = 0.9949 × WATT
VA = 0.9978 × WATT	VA = 1.0015 × WATT
Integrator ON[16]	
VAR = 0.9997 × WATT	VAR = 0.9999 × WATT
VA = 0.9977 × WATT	VA = 1.0015 × WATT

Table 44. Gain compensation adjustments

Line Frequency = 50Hz	**Line Frequency = 60Hz**
Integrator OFF	
VARGAIN = 19.76 + WGAIN/0.9952	VARGAIN = 21 + WGAIN/0.9949
VAGAIN = 9.03 + WGAIN/0.9978	VAGAIN = -60.53 + WGAIN/1.0015
Integrator ON[1]	
VARGAIN = 1.23 +	VARGAIN = 0.41 +

[16] This function is not available in ADE7166 and ADE7566 products

WGAIN/0.9997	WGAIN/0.9999
VAGAIN = 9.44 + WGAIN/0.9977	VAGAIN = -60.53 + WGAIN/1.0015

ENERGY MEASUREMENT INTERRUPTS

The Energy Measurement part of the ADE75XX/ADE71XX has its own interrupt vector for the 8052 core – Vector address 0x004B – see Interrupt Vectors section. The bits set in the Interrupt Enable Register 1 SFR (MIRQENL, 0xD9), Interrupt Enable Register 2 SFR (MIRQENM, 0xDA), and Interrupt Enable Register 3 SFR (MIRQENH, 0xDB) enables the energy measurement interrupts that are allowed to interrupt the 8052 core. If an event is not enabled, it cannot create a system interrupt.

The ADE interrupt stays active until the status bit that has created the interrupt is cleared. A status bit of the ADE irq status register (1, 2 or 3) is cleared when a zero is written the bit to clear and acknowledge the event.

TEMPERATURE, BATTERY AND EXTERNAL VOLTAGE MEASUREMENTS

The ADE75XX/ADE71XX includes temperature measurements as well as battery and an external voltage measurements. These measurements enable many forms of compensation. The temperature measurements can be used to compensate external circuitry. The RTC can be calibrated over temperature to ensure that it doesn't drift. External voltage measurements allow the VDCIN voltage to be monitored, which is especially useful if the VDCIN voltage tracks the bulk voltage. Battery measurements allow low battery detection to be performed. All ADC measurements are configured through the SFR detailed in Table 45.

The temperature, battery and external voltage measurements can be configured to still be functional in PSM1 and PSM2. This is done bit setting bit RTCEN in the RTC Configuration SFR (TIMECON, 0xA1). Maintaining the temperature measurement active ensures that it is not necessary to wait for the temperature measurement to settle before using it for compensation.

Table 45. Temperature, Battery and External voltage measurement SFRs

SFR address (hex)	R/W	Name	Description
0xF9	R/W	STRBPER	Strobing period configuration
0xF3	R/W	DIFFPROG	Temperature and supply Delta configuration
0xD8	R/W	ADCGO	ADC start configuration
0xFA	R/W	BATVTH	Battery threshold configuration
0xEF	R/W	VDCINADC	VDCIN ADC value
0xDF	R/W	BATADC	Battery ADC value
0xD7	R/W	TEMPADC	Temperature ADC value

Table 46. Peripheral ADC Strobe Period SFR (STRBPER, 0xF9)

Note: The strobing option only work when the RTCEN bit in RTC Configuration SFR (TIMECON, 0xA1) is set.

Bit Location	Bit Mnemonic	Default Value	Description		
7-6	Reserved	-	Reserved		
5-4	VDCIN_PERIOD[1:0]	0	Period for background external voltage measurements		
			VDCIN_PERIOD[1:0]		
			0	0	No VDCIN measurement
			0	1	8 minutes
			1	0	2 minutes
			1	1	1 minute
3-2	BATT_PERIOD[1:0]	0	Period for background battery level measurements		
			BATT_PERIOD[1:0]		
			0	0	No Battery measurement
			0	1	16 minutes
			1	0	4 minutes
			1	1	1 minute
1-0	TEMP_PERIOD[1:0]	0	Period for background temperature measurements		
			TEMP_PERIOD[1:0]		
			0	0	No Temperature measurements
			0	1	8 minutes

			1	0	2 minutes
			1	1	1 minute

Table 47. Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3)

Bit Location	Bit Mnemonic	Default Value	Description			
7-6	Reserved	0	Reserved			
5-3	TEMP_DIFF[2:0]	0	Difference threshold between last temperature measurement interrupting 8052 and new temperature measurement that should interrupt 8052			
			TEMP_DIFF[2:0]			
			0	0	0	No Interrupt
			0	0	1	1 LSB (≈ 0.8°C)
			0	1	0	2 LSB (≈ 1.6°C)
			0	1	1	3 LSB (≈ 2.4°C)
			1	0	0	4 LSB (≈ 3.2°C)
			1	0	1	5 LSB (≈ 4.0°C)
			1	1	0	6 LSB (≈ 4.8°C)
			1	1	1	Every Temperature measurement
2-0	VDCIN_DIFF[2:0]	0	Difference threshold between last external voltage measurement interrupting 8052 and new external voltage measurement that should interrupt 8052			
			VDCIN_DIFF[2:0]			
			0	0	0	No Interrupt
			0	0	1	1 LSB (≈ 120 mV)
			0	1	0	2 LSB (≈ 240 mV)
			0	1	1	3 LSB (≈ 360 mV)
			1	0	0	4 LSB (≈ 480 mV)
			1	0	1	5 LSB (≈ 600 mV)
			1	1	0	6 LSB (≈ 720 mV)
			1	1	1	Every VDCIN measurement

48. Start ADC Measurement SFR (ADCGO, 0xD8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0xDF	PLLACK	0	Set this bit to clear the PLL fault bit, PLL_FLT in the PERIPH register. A PLL fault is generated if a reset was caused because the PLL lost lock.
6-3	0xDE – 0xDB	Reserved	0	Reserved
2	0xDA	VADC	0	Set this bit to initiate an externalvoltage measurement. This bit will be cleared when the measurement request is received by the ADC.
1	0xD9	TADC	0	Set this bit to initiate a temperature measurement. This bit will be cleared when the measurement request is received by the ADC.
0	0xD8	BTADC	0	Set this bit to initiate a battery measurement. This bit will be cleared when the measurement request is received by the ADC.

Table 49. Battery detection threshold SFR (BATVTH, 0xFA)

Bit	Bit	Default Value	Description

Location	Mnemonic		
7-0	BATVTH	0	The battery ADC value is compared to this register, the battery threshold register. If BATADC is lower than the threshold, an interrupt is generated.

Table 50. VDCIN ADC value SFR (VDCINADC, 0xEF)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	VDCINADC	0	The external voltage ADC value in this register is updated when a VDCINADC interrupt occurs.

Table 51. Battery ADC value SFR (BATADC, 0xDF)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	BATADC	0	The battery ADC value in this register is updated when a BATADC interrupt occurs.

Table 52. Temperature ADC value SFR (TEMPADC, 0xD7)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TEMPADC	0	The temperature ADC value in this register is updated when a TEMPADC interrupt occurs.

TEMPERATURE MEASUREMENT

To provide a digital temperature measurement, the ADE75XX/ADE71XX includes a dedicated ADC. An 8-bit Temperature ADC value SFR (TEMPADC, 0xD7) holds the results of the temperature conversion. The resolution of the temperature measurement is TBD˚C/LSB. There are two ways to initiate a temperature conversion:

- Single Temperature Measurement

- Background Temperature Measurements

Single Temperature Measurement

Set the TADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8) to get a temperature measurement. An interrupt will be generated when the conversion is done and the temperature measurement is available in the Temperature ADC value SFR (TEMPADC, 0xD7).

Background Temperature Measurements

Background temperature measurements are disabled by default. To configure the background temperature measurement mode, set a temperature measurement interval in the Peripheral ADC Strobe Period SFR (STRBPER, 0xF9). Then temperature measurements will be performed periodically in the background – see Table 46. When a temperature conversion completes, the new temperature ADC value is compared to the last temperature ADC value that created an interrupt. If the absolute difference between the two values is greater than the setting in the TEMP_DIFF bits in the Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3), a TEMPADC interrupt is generated. This allows temperature measurements to take place completely in the background, only requiring MCU activity if the temperature has changed more than a configurable delta.

To set up background temperature measurements:

1. Initiate a single temperature measurement by setting the TADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8).

2. Upon completion of this measurement, configure the TEMP_DIFF[2:0] bits to establish the change in temperature that will trigger an interrupt.

3. Set up the interval for background temperature measurements by configuring the TEMP_PERIOD[1:0] bits.

Temperature ADC in PSM1 and PSM2

Depending on the operating mode of the ADE75XX/ADE71XX, a temperature conversion is initiated only by certain actions:

PSM0: In this operating mode, the 8052 is active. Temperature measurements are available in the background measurement mode and by initiating a single measurement.

PSM1: In this operating mode, the 8052 is active and the part is powered from battery. Single temperature measurements can be

initiated by setting the TADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8). Background temperature measurements are not available.

PSM2: In this operating mode, the 8052 is not active. Temperature conversions are available through the background measurement mode only.

The Temperature ADC value SFR (TEMPADC, 0xD7) is updated with a new value only when a temperature ADC interrupt occurs.

Temperature ADC interrupt

The temperature ADC can generate an ADC interrupt when at least one of the following conditions occurs:

- The difference between the new temperature ADC value and the last temperature ADC value generating an ADC interrupt is larger than the value set in the TEMP_DIFF bits.

- The Temperature ADC conversion, initiated by setting TADC in the Start ADC Measurement SFR (ADCGO, 0xD8), is finished.

When the ADC interrupt occurs, a new value is available in the Temperature ADC value SFR (TEMPADC, 0xD7). Note that there is no flag associated with this interrupt.

BATTERY MEASUREMENT

To provide a digital battery measurement, the ADE75XX/ADE71XX includes a dedicated ADC. The battery measurement is available in an 8-bit SFR (Battery ADC value SFR (BATADC, 0xDF). The battery measurement has a resolution of 15 mV/LSB. A battery conversion can be initiated by two methods:

- Single Battery Measurement

- Background Battery Measurements

Single Battery Measurement

Set the BTADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8) to get a battery measurement. An interrupt will be generated when the conversion is done and the battery measurement is available in the Battery ADC value SFR (BATADC, 0xDF).

Background Battery measurements

To configure background measurements for the battery, establish a measurement interval in the Peripheral ADC Strobe Period SFR (STRBPER, 0xF9). Then battery measurements will be performed periodically in the background – see Table 46. When a battery conversion completes, the battery ADC value is compared to the low battery threshold, established in the Battery detection threshold SFR (BATVTH, 0xFA). If it is below this threshold, a low battery flag is set. This low battery flag is the BATTFLAG bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8), used for power supply monitoring. This low battery flag can be enabled to generate the PSM interrupt by setting the EBATT bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC). This method allows battery measurements to take place completely in the background, only requiring MCU activity if the battery drops below a user specified threshold.

To set up background battery measurements:

1. Configure the Battery detection threshold SFR (BATVTH, 0xFA) to establish a low battery threshold. If the BATADC measurement is below this threshold, the BATTFLAG in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) will be set.

2. Set up the interval for background battery measurements by configuring the BATT_PERIOD[1:0] bits.

Battery ADC in PSM1 and PSM2

Depending on the operating mode, a battery conversion is initiated only by certain actions:

PSM0: In this operating mode, the 8052 is active. Battery measurements are available in the background measurement mode and by initiating a single measurement.

PSM1: In this operating mode, the 8052 is active and the part is powered from battery. Single battery measurements can be initiated by setting the BTADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8). Background battery measurements are not available.

PSM2: In this operating mode, the 8052 is not active. Battery conversions are available through the background measurement mode only.

Battery ADC interrupt

The battery ADC can generate an ADC interrupt when at least one of the following conditions occurs:

- The new battery ADC value is smaller than the value set in the Battery detection threshold SFR (BATVTH, 0xFA), indicating a battery voltage loss.

- A single battery measurement, initiated by setting the BATT_ADC_GO bit, is finished.

When the battery flag is set in the Power Management Interrupt Flag SFR (IPSMF, 0xF8), a new ADC value is available in the Battery ADC value SFR (BATADC, 0xDF). This battery flag can be enabled as a source of the PSM interrupt to generate a PSM interrupt every time the battery drops below a set voltage threshold or after a single conversion initiated by setting the BATT_ADC_GO bit is ready.

The Battery ADC value SFR (BATADC, 0xDF) is updated with a

new value only when the Battery flag is set in the Power Management Interrupt Flag SFR (IPSMF, 0xF8).

EXTERNAL VOLTAGE MEASUREMENT

The ADE75XX/ADE71XX includes a dedicated ADC to provide a digital measurement of an external voltage, on the V_{DCIN} pin. An 8-bit SFR (Table 50. VDCIN ADC value SFR (VDCINADC, 0xEF)) holds the results of the conversion. The resolution of the external voltage measurement is TBD V/LSB. There are two ways to initiate an external voltage conversion:

- Single External Voltage Measurement

- Background ExternalVoltage Measurements

Single External voltage Measurement

Set the VADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8) to get an external voltage measurement. An interrupt will be generated when the conversion is done and the external voltage measurement is available in the Table 50. VDCIN ADC value SFR (VDCINADC, 0xEF).

Background External Voltage Measurements

Background external voltage measurements are disabled by default. To configure the background external voltage measurement mode, set an external voltage measurement interval in the Peripheral ADC Strobe Period SFR (STRBPER, 0xF9). Then external voltage measurements will be performed periodically in the background – see Table 46. When an external voltage conversion completes, the new external voltage ADC value is compared to the last external voltage ADC value that created an interrupt. If the absolute difference between the two values is greater than the setting in the VDCIN_DIFF bits in the Temperature and Voltage ADC Delta SFR (DIFFPROG, 0xF3), a VDCIN ADC flag is set. This VDCIN ADC flag is the FVADC in the Power Management Interrupt Flag SFR (IPSMF, 0xF8), used for power supply monitoring. This VDCIN ADC flag can be enabled to generate a PSM interrupt by setting the EVADC bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC). This method allows external voltage measurements to take place completely in the background, only requiring MCU activity if the external voltage has changed more than a configurable delta.

To set up background external voltage measurements:

1. Initiate a single external voltage measurement by setting the VADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8).
2. Upon completion of this measurement, configure the VDCIN_DIFF[2:0] bits to establish the change in voltage that will set the FVADC in the Power Management Interrupt Flag SFR (IPSMF, 0xF8).
3. Set up the interval for background external voltage measurements by configuring the VDCIN_PERIOD[1:0] bits.

External voltage ADC in PSM1 and PSM2

Depending on the operating mode of the ADE75XX/ADE71XX, an external voltage conversion is initiated only by certain actions:

PSM0: In this operating mode, the 8052 is active. External voltage measurements are available in the background measurement mode and by initiating a single measurement.

PSM1: In this operating mode, the 8052 is active and the part is powered from battery. Single external voltage measurements can be initiated by setting the VADC bit in the Start ADC Measurement SFR (ADCGO, 0xD8). Background external voltage measurements are not available.

PSM2: In this operating mode, the 8052 is not active. External voltage conversions are available through the background measurement mode only.

The external voltage ADC, VDCIN ADC value SFR (VDCINADC, 0xEF), is updated with a new value only when an external voltage ADC interrupt occurs.

External voltage ADC interrupt

The external voltage ADC can generate an ADC interrupt when at least one of the following conditions occurs:

- The difference between the new external voltage ADC value and the last external voltage ADC value generating an ADC interrupt is larger than the value set in the VDCIN_DIFF bits.

- The External voltage ADC conversion, initiated by setting TEMP_ADC_GO, is finished.

When the ADC interrupt occurs, a new value is available in the VDCIN ADC value SFR (VDCINADC, 0xEF). Note that there is no flag associated with this interrupt.

8052 MCU CORE ARCHITECTURE

The ADE75XX/ADE71XX has an 8052 MCU core and uses the 8051 instruction set. Some of the standard 8052 peripherals, such as the UART, have been enhanced. This section describes the standard 8052 core and enhancements that have been made to it in the ADE75XX/ADE71XX.

The special function register (SFR) space is mapped into the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADE75XX/ADE71XX via the SFR area is shown in Figure 54.

All registers except the program counter (PC), instruction register (IR) and the four general-purpose register banks reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

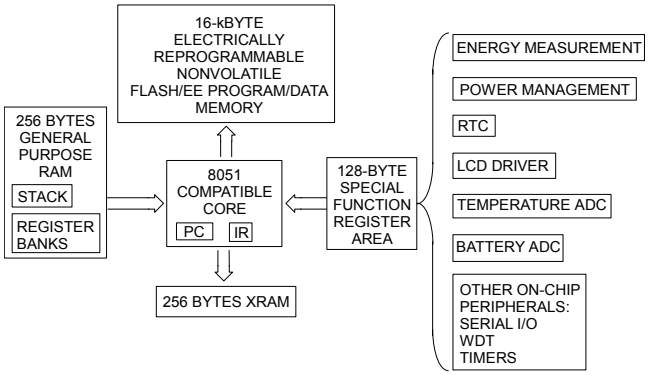


Figure 54: ADE75XX/ADE71XX Block Diagram

MCU REGISTERS

The registers used by the MCU are summarized hereafter.

Table 53. 8051 SFRs

SFR	Address	Bit Addressable	Description
A	0xE0	Yes	Accumulator
B	0xF0	Yes	Auxiliary Math register
PSW	0xD0	Yes	Program status word - see Table 54
PCON	0x87	No	Power Control register – see Table 55
DPL	0x82	No	Data pointer LSByte – see Table 56
DPH	0x83	No	Data pointer MSbyte – see Table 57
SP	0x81	No	Stack pointer LSB byte – see Table 58
CFG	0xAF	No	Configuration register – see Table 59

Table 54. Program Status Word SFR (PSW, 0xD0)

Bit Location	Bit Addr.	Bit Name	Description		
7	0xD7	CY	Carry Flag. Modified by ADD, ADDC, SUBB, MUL, and DIV instructions.		
6	0xD6	AC	Auxiliary Carry Flag. Modified by ADD, and ADDC instructions.		
5	0xD5	F0	General-Purpose Flag availble to the user		
4-3	0xD4, 0xD3	RS1, RS0	Register Bank Select Bits.		
			RS1	RS0	Selected Bank
			0	0	0
			0	1	1
			1	0	2
			1	1	3
2	0xD2	OV	Overflow Flag. Modified by ADD, ADDC, SUBB, MUL and DIV instructions.		
1	0xD1	F1	General-Purpose Flag availble to the user.		
0	0xD0	P	Parity Bit. The number of bits set in the Accumulator added to the value of the parity bit will always be an even number.		

Table 55. Program Control SFR (PCON, 0x87)

Bit Location	Default	Description
7	0	Double baud rate control
6-0	0	Reserved, should be left cleared

Table 56. Data Pointer Low SFR (DPL, 0x82)

Bits	Default	Description
7-0	0	Contain the low byte of the data pointer

Table 57. Data Pointer High SFR (DPH, 0x83)

Bits	Default	Description
7-0	0	Contain the high byte of the data pointer

Table 58. Stack Pointer SFR (SP, 0x81)

Bits	Default	Description
7-0	7	Contain the 8 LSB of the pointer for the stack

Table 59. Configuration SFR (CFG, 0xAF)

Bit Location	Bit Mnemonic		
7	Reserved.. This bit should be left set for proper operation.		
6	EXTEN	Enhanced UART enable bit	
		0	Standard 8052 UART without enhanced error checking features
		1	Enhanced UART with enhanced error checking—see the UART additional features section.
5	SCPS	Synchronous communication selection bit	
		0	I2C port is selected for control of the shared I2C/SPI pins and SFRs
		1	SPI port is selected for control of the shared I2C/SPI pins and SFRs
4	MOD38EN	38kHz modulation enable bit	
		0	38kHz modulation is disabled.
		1	38kHz modulation is enabled on the pins selected by the MOD38[7:0] bits in the EP_CFG SFR.
3-2	Reserved		
1-0	XREN[1:0]	XREN[1] OR XREN[0] =1	Enable MOVX instruction to use 256 bytes of Extended RAM.
		XREN[1] AND XREN[0] =0	Disable MOVX instruction

BASIC 8052 REGISTERS

Program Counter (PC): The Program Counter holds the two byte address of the next instruction to be fetched. The PC is initialized with 0x00 at Reset and is incremented after each instruction is performed. Note that the amount that is added to the PC depends on the number of bytes in the instruction, so the increment can range from one to three bytes. The program counter is not directly accessible to the user but can be directly modified by CALL and JMP instructions that change which part of the program is active.

Instruction Register (IR): The Instruction Register holds the opcode of the instruction being executed. The opcode is the binary code that results from assembling an instruction. This register is not directly accessible to the user.

Register Banks: There are four banks containing 8 byte-wide registers each, for a total of 32 bytes of registers. These registers are convenient for temporary storage of mathematical operands. An instruction involving the accumulator and a register can be executed in 1 clock cycle as opposed to 2 clock cycles to perform an instruction involving the accumulator and a literal or a byte of general purpose RAM. The register banks are located in the first 32 bytes of RAM.

The active register bank is selected by the RS0 and RS1 bits in the Program Status Word SFR (PSW, 0xD0).

Accumulator: The accumulator is a working register, storing the results of many arithmetic or logical operations. The accumulator is used in more than half of the 8052 instructions where it is usually referred to as A. The status register (PSW) constantly monitors the number of bits that are set in the accumulator to determine if it has even or odd parity. The accumulator is stored in the SFR space - see Table 53.

B Register: The B register is used by the multiply and divide instructions, MUL AB and DIV AB to hold one of the operands. Since it isn't used for many instructions, it can be used as a scratchpad register like those in the register banks. The B register is stored in the SFR space - see Table 53.

Program Status Word (PSW): The PSW register reflects the status of arithmetic and logical operations through carry, auxiliary carry and overflow flags. The parity flag reflects the parity of the contents of the accumulator, which can be helpful for communication protocols. The PSW bits are described in Table 54. The Program Status Word SFR (PSW, 0xD0) is bit addressable.

Data Pointer (DPTR): The data pointer is made up of two 8-bit registers: DPH (high byte), and DPL (low byte). These provide memory addresses for internal code and data access. The DPTR can be manipulated as a 16-bit register (DPTR = DPH, DPL), or as two independent 8-bit registers (DPH, DPL) – see Table 56 and Table 57.

The ADE75XX/ADE71XX supports dual data pointers. See the Dual Data Pointers section.

Stack Pointer (SP): The Stack Pointer keeps track of the current address of the top of the stack. To push a byte of data onto the stack, the stack pointer is incremented and the data is moved to the new top of the stack. To pop a byte of data off of the stack, the top byte of data is moved into the awaiting address and the stack pointer is decremented. The stack is a last in first out (LIFO) method of data storage because the most recent addition to the stack is the first to come off it.

The stack is utilized during CALL and RET instructions to keep track of the address to move into the PC when returning from the function call. The stack is also manipulated when vectoring for interrupts, to keep track of the prior state of the PC.

The stack resides into the extended internal RAM and the SP register holds the address of the stack into the externded RAM. The advantage of this solution is that the stack is segregated to the extended internal RAM. The use of the general purpose RAM can be limited to data storing and the use of the extended internal RAM limited to the stack pointer. This separation limits the chance of corruption of the data RAM with the stack pointer overflowing in data RAM.
Data can still be stored in extended RAM by using the MOVX command.

To change the default starting address for the stack, move a value into the stack pointer, SP. For example, to enable the extended stack pointer and initialize it at the beginning of the XRAM space, use this code:

```
MOV     SP,#00H
```

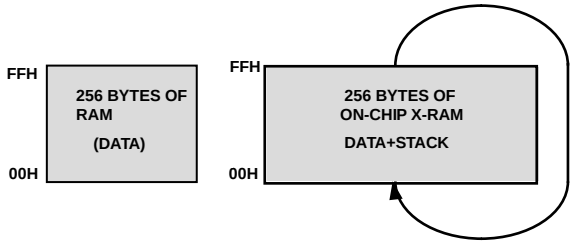


Figure 55. Extended Stack Pointer Operation

STANDARD 8052 SFRS

The standard 8052 special function registers include the Accumulator, B, PSW, DPTR and SP SFRs described in the Basic 8052 Registers section. The 8052 also defines standard timers, serial port interface, interrupts, I/O ports and power down modes.

Timer SFRs: The 8052 contains 3 16-bit timers, the identical Timer0 and Timer1 as well as a Timer2. These timers can also function as event counters. Timer2 has a capture feature where the value of the timer can be captured in two 8-bit registers upon the assertion of an external input signal - see Table 96 and Timers section.

Serial Port SFRs: The full-duplex serial port peripheral requires two registers, one for setting up the baud rate and other communication parameters, and another byte for the transmit/receive buffer. The ADE75XX/ADE71XX also provides

enhanced serial port functionality with a dedicated timer for baud rate generation with a fractional divisor and additional error detection. See Table 121 and UART serial interface section.

Interrupt SFRs: There is a two-tiered interrupt system standard in the 8052 core. The priority level for each interrupt source is individually selectable as high or low. The ADE75XX/ADE71XX **enhances this interrupt system** by creating in essence a third interrupt tier for a highest priority power supply management interrupt, PSM - See Interrupt System section.

I/O Port SFRs: The 8052 core supports four I/O ports, P0 through P3 where Ports 0 and 2 are typically used for access to external code and data spaces. The ADE75XX/ADE71XX, unlike standard 8052 products, provides internal nonvolatile Flash memory so that an external code space is unnecessary. The on-chip LCD driver requires many pins, some of which are dedicated for LCD functionality and others that can be configured at LCD or general purpose I/O. Due to the limited number of I/O pins, the ADE75XX/ADE71XX does not allow access to external code and data spaces.

The ADE75XX/ADE71XX provides 20 pins that can be used for general purpose I/O. These pins are mapped to Ports 0, 1 and 2 and are accessed through three bit-addressable 8052 SFRs P0, P1 and P2. Another enhanced feature of the ADE75XX/ADE71XX is that the weak pull-ups standard on 8052 Ports 1, 2 and 3 can be disabled to make open drain outputs, as is standard on Port 0. The weak pull-ups can be enabled on a pin by pin basis. See the I/O Ports section.

Power Control Register (PCON, 0x87): The 8052 core defines two power down modes; power down and idle. The ADE75XX/ADE71XX **enhances the power control** capability of the traditional 8052 MCU with additional power management functions. The POWCON register is used to define power control specific functionality for the ADE75XX/ADE71XX. The Program Control SFR (PCON, 0x87) is not bit addressable. See the Power Management section.

The ADE75XX/ADE71XX provides many other peripherals not standard to the 8052 core.

- ADE Energy Measurement DSP
- RTC
- LCD driver
- Battery Switchover/Power Management
- Temperature ADC
- Battery ADC
- SPI/I²C communication
- Flash Memory controller
- Watchdog Timer

MEMORY OVERVIEW

The ADE75XX/ADE71XX contains three memory blocks:

- 16 kbytes of on-chip Flash/EE program and data memory
- 256 bytes of general-purpose RAM
- 256 bytes of internal extended RAM (XRAM)

The 256 bytes of general-purpose RAM shares the upper 128 bytes of its address space with Special Function Registers. All of the memory spaces are shown in Figure 54. The addressing mode specifies which memory space to access.

General Purpose RAM: General purpose RAM resides in memory locations 0x00 through 0xFF. It contains the register banks.

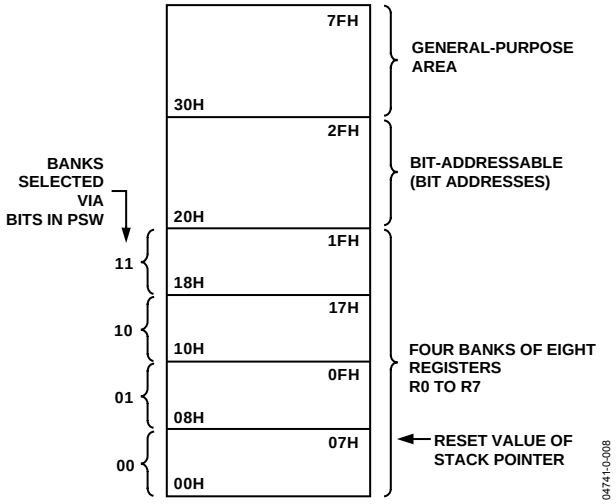


Figure 56. Lower 128 Bytes of Internal Data Memory

Addresses 0x80 through 0xFF of General Purpose RAM are shared with the Special Function Registers. The mode of addressing determines which memory space is accessed as shown in Figure 57.

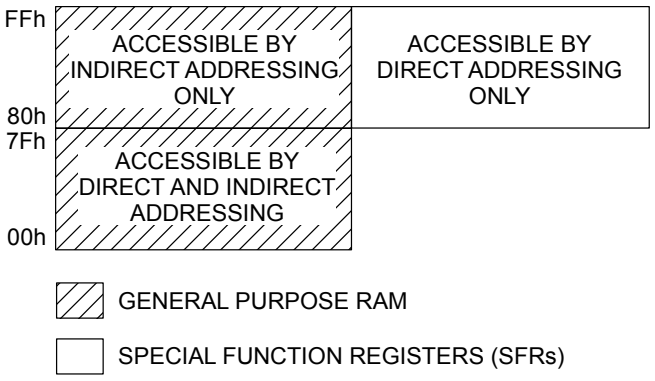


Figure 57: General Purpose RAM and SFR memory address overlap

Both direct and indirect addressing can be used to access General Purpose RAM from 0x00 through 0x7F but indirect addressing must be used to access General Purpose RAM with addresses in the range from 0x80 through 0xFF because they share the same address space with the Special Function Registers (SFRs).

The 8052 core also has the means to access individual bits of certain addresses in the General Purpose RAM and Special Function Memory spaces. The individual bits of General Purpose RAM addresses 0x20 through 0x2F can be accessed through their bit addresses 0x00 through 0x7F. The benefit of bit addressing is that the individual bits can be accessed quickly, without the need for bit masking, which takes more code memory and execution time. The bit addresses for General Purpose RAM addresses 0x20 through 0x2F can be seen in Figure 58.

Byte Address	Bit Addresses (hexa)							
0x2F	7F	7E	7D	7C	7B	7A	79	78
0x2E	77	76	75	74	73	72	71	70
0x2D	6F	6E	6D	6C	6B	6A	69	68
0x2C	67	66	65	64	63	62	61	60
0x2B	5F	5E	5D	5C	5B	5A	59	58
0x2A	57	56	55	54	53	52	51	50
0x29	4F	4E	4D	4C	4B	4A	49	48
0x28	47	46	45	44	43	42	41	40
0x27	3F	3E	3D	3C	3B	3A	39	38
0x26	37	36	35	34	33	32	31	30
0x25	2F	2E	2D	2C	2B	2A	29	28
0x24	27	26	25	24	23	22	21	20
0x23	1F	1E	1D	1C	1B	1A	19	18
0x22	17	16	15	14	13	12	11	10
0x21	0F	0E	0D	0C	0B	0A	09	08
0x20	07	06	05	04	03	02	01	00

Figure 58: Bit Addressable Area of General Purpose RAM

Bit addressing can be used for instructions that involve Boolean variable manipulation and program branching—see the Instruction set.

Special Function Registers: Special Function Registers are registers that affect the function of the 8051 core or its peripherals. These registers are located in RAM with addresses 0x80 through 0xFF. They are only accessible through direct addressing as shown in Figure 57 .

The individual bits of some of the SFRs can be accessed for use in Boolean and program branching instructions. These SFRs are labeled as bit-addressable and the bit addresses are given in the SFR Mapping.

Extended Internal RAM (XRAM): The ADE75XX/ADE71XX provides 256 bytes of extended on-chip RAM. No external RAM is supported. This RAM is located in addresses 0x0000 through 0x00FF in the Extended RAM space. To select the Extended RAM memory space, the extended indirect addressing modes are used. The internal XRAM is enabled in the Configuration SFR (CFG, 0xAF) by writing 01 to CFG[1:0].

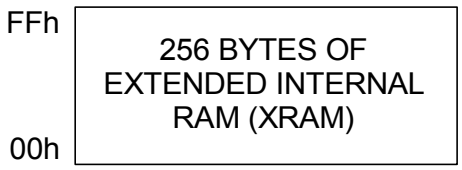


Figure 59: Extended Internal RAM (XRAM) Space

Code Memory: Code and data memory are stored in the 16kbyte Flash memory space. No external code memory is supported. To access Code memory, Code Indirect addressing is used.

ADDRESSING MODES

The 8052 core provides several addressing modes. The addressing mode determines how the core will interpret the memory location or data value specified in assembly language code. There are six addressing modes as shown in Table 60:

Table 60. 8052 Addressing Modes

Addressing Mode	Example	Bytes	Core Clock Cycles
Immediate	MOV A, #A8h	2	2
	MOV DPTR,#A8h	3	3
Direct	MOV A, A8h	2	2
	MOV A, IE	2	2
	MOV A, R0	1	1
Indirect	MOV A,@R0	1	2
Extended Direct	MOVX A, @DPTR	1	4
Extended Indirect	MOVX A, @R0	1	4
Code Indirect	MOVC A, @A+DPTR	1	4
	MOVC A, @A+PC	1	4
	JMP @A+DPTR	1	3

Immediate Addressing: In Immediate Addressing, the expression entered after the number sign (#) will be evaluated

by the assembler and stored in the memory address specified. This number is referred to as a literal because it refers only to a value and not to a memory location. Instructions using this addressing mode will be slower than those between two registers since the literal must be stored and fetched from memory. The expression can be entered as a symbolic variable or an arithmetic expression; the value will be computed by the assembler.

Direct Addressing: With Direct Addressing, the value at the source address is moved to the destination address. Direct Addressing provides the fastest execution time of all the addressing modes when an instruction is performed between registers using direct addressing. Note that indirect or direct addressing modes can be used to access general purpose RAM addresses 0x00 through 0x7F. An instruction with direct addressing that uses an address between 0x80 and 0xFF is referring to a special function memory location.

Indirect Addressing: With Indirect Addressing, the value pointed to by the register is moved to the destination address. For example, to move the contents of internal RAM address 82h to the accumulator:

```
MOV    R0,#82h
MOV    A,@R0
```

The two instructions above require a total of four clock cycles and three bytes of storage in the program memory.

Indirect addressing allows addresses to be computed, and is useful for indexing into data arrays stored in RAM.

Note that an instruction that refers to addresses 00 through 7Fh is referring to internal RAM and indirect or direct addressing modes can be used. An instruction with indirect addressing that uses an address between 80h and FFh is referring to internal RAM, not to a SFR.

Extended Direct Addressing: The DPTR register is used to access internal extended RAM in extended indirect addressing mode. The ADE75XX/ADE71XX provides 256 bytes of internal extended RAM (XRAM), accessed through MOVX instructions. External memory spaces are not supported on this device.

In extended direct addressing mode, the DPTR register points to the address of the byte of extended RAM. The following code will move the contents of extended RAM address 100h to the accumulator:

```
MOV    DPTR,#100h
MOVX   A,@DPTR
```

The two instructions above require a total of seven clock cycles and four bytes of storage in the program memory.

Extended Indirect Addressing: The internal extended RAM is accessed through a pointer to the address in indirect addressing mode. The ADE75XX/ADE71XX provides 256 bytes of internal extended RAM, accessed through MOVX instructions. External memory is not supported on this device.

In extended indirect addressing mode, a register holds the address of the byte of extended RAM. The following code will move the contents of extended RAM address 80h to the accumulator:

```
MOV    R0,#80h
MOVX   A,@R0
```

The two instructions above require six clock cycles and three bytes of storage.

Note that there are 256 bytes of extended RAM, so both extended direct and extended indirect addressing can cover the whole address range. There is a storage and speed advantage to using extended indirect addressing because the additional byte of addressing available through the DPTR register that is not needed is not stored.

From the three examples demonstrating the access of internal RAM from 80h through FFh and extended internal RAM from 00h through FFh, it can be seen that it is most efficient to use the entire internal RAM accessible through indirect access before moving to extended RAM.

Code Indirect Addressing: The internal code memory can be accessed indirectly. This can be useful for implementing lookup tables and other arrays of constants that are stored in Flash. For example, to move the data stored in Flash memory at address 8002h into the Accumulator:

```
MOV    DPTR,#8002h
CLR    A
MOVX   A,@A+DPTR
```

The Accumulator can be used as a variable index into the array of Flash memory located at DPTR.

INSTRUCTION SET

Table 61 documents the number of clock cycles required for eachinstruction. Most instructions are executed in one or two clock cycles,resulting in a 4 MIPS peak performance.

Table 61. Instruction Set

Mnemonic	Description	Bytes	Cycles
Arithmetic			
ADD A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2

Mnemonic	Description	Bytes	Cycles
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn 1 1	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carry	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @	Ri Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	9
DIV AB	Divide A by B	1	9
DA A A	Decimal adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3
XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,	dir Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Mnemonic	Description	Bytes	Cycles
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn,dir	Move register to direct byte	2	2
MOV dir,Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A 1	1	4
MOVX A,@Ri	Move external (A8) data to A	1	4
MOVX A,@DPTR	Move external (A16)data to A	1	4
MOVX @Ri,A	Move A to external data (A8)	1	4
MOVX @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit OR	direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			

Mnemonic	Description	Bytes	Cycles
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry equal to 1	2	3
JNC rel	Jump on carry equal to 0	2	3
JZ rel	Jump on accumulator =0	2	3
JNZ rel	Jump on accumulator not equal to 0	2	3
DJNZ Rn,rel	Decrement register,JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit =1	3	4
JNB bit,rel	Jump on direct bit =0	3	4
JBC bit,rel	Jump on direct bit =1 and clear	3	4
CJNE A,dir,rel	Compare A,direct JNE relative	3	4
CJNE A,#data,rel	Compare A,immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register,immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect,immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte,JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

READ-MODIFY-WRITE INSTRUCTIONS

Some 8051 instructions read the latch while others read the pin. The state of the pin is read for instructions that input a port bit. Instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and rewrite it to the latch. Since these instructions involve modifying the port, it is assumed that the pins being modified are outputs, so the output state of the pin is read from the latch. This prevents a possible misinterpretation of the voltage level of a pin. For example, if a port pin is used to drive the base of a transistor, a 1 is written to the bit, to turn the transistor on. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

The instructions that read the latch rather than the pins are called read-modify-write instructions, and are listed in Table 62. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 62. Read-Modify-Write Instructions

Instruction	Example	Description
ANL	ANL P0, A	Logical AND
ORL	ORL P1, A	Logical OR
XRL	XRL P2, A	Logical EX-OR
JBC	JBC P1.1, LABEL	Jump if Bit = 1 and clear bit
CPL	CPL P2.0	Complement bit
INC	INC P2	Increment
DEC	DEC P2	Decrement
DJNZ	DJNZ P0, LABEL	Decrement and jump if not zero
MOV PX.Y, C[1]	MOV P0.0,C	Move Carry to Bit Y of Port X
CLR PX.Y[1]	CLR P0.0	Clear Bit Y of Port X
SETB PX.Y[1]	SETB P0.0	Set Bit Y of Port X

[1] These instructions read the port byte (all 8 bits), modify the addressed bit, and write the new byte back to the latch.

INSTRUCTIONS THAT AFFECT FLAGS

Many instructions explicitly modify the Carry bit such as the MOV C, bit and CLR C instructions. Other instructions that affect status flags are listed in this section.

ADD A, source

Function: Adds the source to the Accumulator.

Status Flags Referenced by Instruction: None
Status Flags Affected:

Status Flag	Description
C	Set if there is a carry out of bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.
OV	Set if there is a carry out of bit 6 or a carry out of bit 7 but not if both are set. Used to indicate an overflow for signed addition. This flag will be set if two positive operands yield a negative result or two negative operands yield a positive result.
AC	Set if there is a carry out of bit 3. Cleared otherwise.

ADDC A, source

Function: Adds the source and the Carry bit to the Accumulator

Status Flags Referenced by Instruction: Carry
Status Flags Affected:

Status Flag	Description
C	Set if there is a carry out of bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.
OV	Set if there is a carry out of bit 6 or a carry out of bit 7 but not if both are set. Used to indicate an overflow for signed addition. This flag will be set if two positive operands yield a negative result or two negative operands yield a positive result.
AC	Set if there is a carry out of bit 3. Cleared otherwise.

SUBB A, source

Function: Subtract the source byte and the carry (borrow) flag from the Accumulator.

Status Flags Referenced by Instruction: Carry (Borrow)
Status Flags Affected:

Status Flag	Description
C	Set if there is a borrow needed for of bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.
OV	Set if there is a borrow is needed for bit 6 or bit 7 but not for both. Used to indicate an overflow for signed subtraction. This flag will be set if a negative number subtracted from a positive yields a negative result or it a positive number subtracted from a negative number yields a positive result.
AC	Set if a borrow is needed for bit 3. Cleared otherwise.

MUL AB

Function: Multiplies the Accumulator by the B register. This operation is unsigned. The lower byte of the 16-bit product is stored in the Accumulator and the higher byte is left in the B register.

Status Flags Referenced by Instruction: None
Status Flags Affected: None

Status Flag	Description
C	Cleared
OV	Set if the result is greater than 255. Cleared otherwise.

DIV AB

Function: Divides the Accumulator by the B register. This operation is unsigned. The integer part of the quotient is stored in the Accumulator and the remainder goes into the B register.

Status Flags Referenced by Instruction: None
Status Flags Affected:

Status Flag	Description
C	Cleared
OV	Cleared unless the B register was equal to 0, in which case the results of the division are undefined and the OV flag is set.

DA A

Function: Adjusts the Accumulator to hold two four bit digits after the addition of two binary coded decimals (BCDs) with the ADD or ADDC instructions. If the AC bit is set or if the value of bits 0-3 exceed 9, 0x06 is added to the accumulator to correct the lower four bits. If the carry bit was set when the instruction began, or if 0x06 was added to the accumulator in the first step, 0x60 is added to the accumulator to correct the higher four bits.

Status Flags Referenced by Instruction: Carry, AC
Status Flags Affected:

Status Flag	Description
C	Set if the result is greater than 99h. Cleared otherwise.

RRC A

Function: Rotates the accumulator to the right through the carry flag. The old LSB of the Accumulator becomes the new carry flag and the old carry flag is loaded into the new MSB of the Accumulator.

Status Flags Referenced by Instruction: Carry
Status Flags Affected:

Status Flag	Description
C	Equal to the state of ACC.0 before execution of the instruction

RLC A

Function: Rotates the accumulator to the left through the carry flag. The old MSB of the Accumulator becomes the new carry flag and the old carry flag is loaded into the new LSB of the Accumulator.

Status Flags Referenced by Instruction: Carry
Status Flags Affected:

Status Flag	Description
C	Equal to the state of ACC.7 before execution of the instruction

CJNE destination, source, relative jump

Function: Compares the value of the source to the value of the destination and branches to the location set by the relative jump if they are not equal. If the values are equal, program execution continues with the instruction after the CJNE instruction.

Status Flags Referenced by Instruction: None
Status Flags Affected:

Status Flag	Description
C	Set if the source value is greater than the destination value. Cleared otherwise.

INTERRUPT SYSTEM

The unique power management architecture of the ADE75XX/ADE71XX includes an operating mode where the 8052 MCU core is shut down, PSM2. There are events that can be configured to wake the 8052 MCU core from the PSM2 operating mode where the MCU core is shut down. A distinction is drawn here between events that can trigger the wakeup of the 8052 MCU core and events that can trigger an interrupt when the MCU core is active. Events that can wake the core are referred to as **wakeup events** while events that can interrupt the program flow when the MCU is active are called **interrupts**. See the 3.3V Peripherals and Wakeup Events section to learn more about events that can wake the 8052 core from PSM2.

The ADE75XX/ADE71XX provides 12 interrupt sources with three priority levels. The power management interrupt is alone at the highest priority level. The other two priority levels are configurable through the Interrupt priority SFR (IP, 0xB8) and Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9).

STANDARD 8051 INTERRUPT ARCHITECTURE

The 8051 standard interrupt architecture includes two tiers of interrupts, where some interrupts are assigned a high priority and others are assigned a low priority.

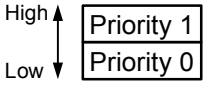


Figure 60: Standard 8051 Interrupt Priority Levels

A Priority 1 interrupt can interrupt the service routine of a Priority 0 interrupt, and if two interrupts of different priorities occur at the same time, the Priority 1 interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed. See the Interrupt Priority section.

ADE75XX/ADE71XX INTERRUPT ARCHITECTURE

The ADE75XX/ADE71XX provides advanced power supply monitoring features. To ensure a fast response to time critical power supply issues, such as a loss of line power, the power supply monitoring interrupt should be able to interrupt any interrupt service routine. In order to enable the user to make full use of the standard 8051 interrupt priority levels, an additional priority level was added for the power supply management, PSM, interrupt. The PSM interrupt is the only interrupt at this highest interrupt priority level.

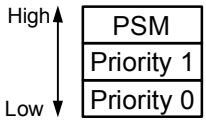


Figure 61: ADE75XX/ADE71XX Interrupt Architecture

See the Power Supply Monitor Interrupt (PSM) section for more information on the PSM interrupt.

INTERRUPT SFR REGISTER LIST

The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

SFR	Address	Default Value	Bit Addressable	Description
IE	0xA8	0x00	Yes	Interrupt Enable Register
IP	0xB8	0x00	Yes	Interrupt Priority Register
IEIP2	0xA9	0xA0	No	Secondary Interrupt Enable Register
INTPR	0xFF	0x00	No	Interrupt Pins Configuration SFR

Table 63. Interrupt Enable SFR (IE, 0xA8)

Bit Location	Bit Addr.	Bit Name	Description
7	0xAF	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	0xAE	ETEMP	Set by the user to enable the temperature ADC interrupt.
5	0xAD	ET2	Set by the user to enable the Timer 2 interrupt.
4	0xAC	ES	Set by the user to enable the UART serial port interrupt.
3	0xAB	ET1	Set by the user to enable the Timer 1 interrupt.
2	0xAA	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT1}$).
1	0xA9	ET0	Set by the user to enable the Timer 0 interrupt.

0	0xA8	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$).

Table 64. Interrupt priority SFR (IP, 0xB8)

Bit Location	Bit Addr.	Bit Name	Description
7	0xBF	PADE	ADE Energy Measurement Interrupt Priority (1 = High; 0 = Low).
6	0xBE	PTEMP	Temperature ADC Interrupt Priority (1 = High; 0 = Low).
5	0xBD	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	0xBC	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	0xBB	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	0xBA	PX1	$\overline{INT1}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	0xB9	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	0xB8	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

Table 65. Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9)

Bit Location	Bit Mnemonic	Description
7		
6	PTI	RTC Interrupt Priority (1 = High; 0 = Low).
5		
4	PSI	SPI/I2C Interrupt Priority (1 = High; 0 = Low).
3	EADE	Set by the user to enable the Energy Metering Interrupt (ADE)
2	ETI	Set by the user to enable the RTC interrupt.
1	EPSM	Set by the user to enable the PSM Power Supply Management interrupt.
0	ESI	Set by the user to enable the SPI/I2C interrupt.

Interrupt pins configuration SFR (INTPR, 0xFF)

Bit Location	Bit Mnemonic	Default Value	Description
7	RTCCAL	0	Control RTC calibration output When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.
6-5	FSEL[1:0]		Sets RTC calibration output frequency and calibration window

FSEL[1:0]		Calibration window, f_{RTCCAL} calibration frequency
0	0	30.5 seconds, 1Hz
0	1	30.5 seconds, 512 Hz
1	0	0.244 seconds, 500Hz
1	1	0.244 seconds, 16.384 kHz

4	Reserved			
3-1	INT1PRG[2:0]	000	Controls the function of $\overline{INT1}$	
			INT1PRG[2:0]	Function
			x 0 0	GPIO
			x 0 1	BCTRL
			0 1 x	$\overline{INT1}$ input disabled
			1 1 x	$\overline{INT1}$ input enabled
0	INT0PRG	0	Controls the function of $\overline{INT0}$	
			INT0PRG	Function
			0	$\overline{INT0}$ input disabled
			1	$\overline{INT0}$ input enabled

Table 66. WatchDog Timer SFR (WDCON, 0xC0)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7-4	0xC7 – 0xC4	PRE[3:0]	7	Watchdog pre-scaler. In normal mode, the 16-bit watchdog timer is clocked by the input clock (32.768kHz). The PRE bits set which of the upper bits of the counter are used as the watchdog output following: $t_{watchdog} = 2^{PRE} \times \frac{2^9}{CLKIN}$ [3:0] Watchdog Timeout 0000 15.6ms 0001 31.2ms 0010 62.5ms 0011 125ms 0100 250ms 0101 500ms 0110 1s 0111 2s 1000 0 Automatic Reset 1001 0 Serial download reset 1010 to 1111 Not a valid selection
3	0xC3	WDIR	0	Watchdog interrupt response bit. When clear, watchdog will generate a system reset when the watchdog time out period has expired When set, the watchdog will generate a interrupt when the watchdog time out period has expired.
2	0xC2	WDS	0	WDS Watchdog status bit. This bit is set to indicate that a watchdog timeout has occurred. WDS is cleared by writing a zero or by an external hardware reset. A watchdog reset will not clear WDS. The bit can therefore be used to distinguish between a watchdog reset and a hardware reset from the RESET pin.
1	0xC1	WDE	1	WDE Watchdog enable bit. When set, enables the watchdog and clears its counter (e.g. 2 above). The watchdog counter is subsequently cleared again whenever the WDE bit is set. If the watchdog is not cleared within its selected timeout period it will generate a system reset or watchdog interrupt, depending on the WDIR bit. The watchdog is disabled (and WDE cleared) by any of the following: Write zero to WDE Watchdog reset (WDIR = 0) Hardware reset PSM interrupt LOCK interrupt.
0	0xC0	WDWR	0	WDWR Watchdog write enable bit. To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the following instruction must be a write instruction to the WDCON SFR. This sequence is necessary so that the WDCON SFR is protected from code execution upsets that might unintentionally modify this SFR. Interrupts should be disabled during this operation due to the consecutive instruction cycles. e.g. Disable Watch dog 1 write to WDCON e.g. 2 Clear WDE bit CLR EA SETB WDWR CLR WDE SETB EA

INTERRUPT PRIORITY

If two interrupts of the same priority level occur simultaneously, the polling sequence, as shown in Table **67**, is observed.

Table 67. Priority within Interrupt Level

Source	Priority	Description
IPSM	0 (Highest)	Power Supply Monitor Interrupt
IRTC	1	RTC interrupt
IADE	2	ADE Energy measurement interrupt
WDT	3	Watchdog Timer Overflow Interrupt
ITEMP	4	Temperature ADC interrupt
IE0	5	External Interrupt 0
TF0	6	Timer/Counter 0 Interrupt
IE1	7	External Interrupt 1
TF1	8	Timer/Counter 1 Interrupt
ISPI/I2CI	9	SPI/I^2C Interrupt
RI/TI	10	UART Serial Port Interrupt
TF2/EXF2	11 (Lowest)	Timer/Counter 2 Interrupt

INTERRUPT FLAGS

The interrupt and status flags associated with the interrupt vectors are shown in Table 68 and Table 69. Most of the interrupts have flags associated with them.

Table 68. Interrupt Flags

Interrupt Source	Flags	Bit Address	Details
IE0	TCON.1	IE0	External Interrupt 0 **Note:** The INT0PRG bit must be set in the Interrupt pins configuration SFR (INTPR, 0xFF) to allow the INT0 signal into the chip
TF0	TCON.5	TF0	Timer 0
IE1	TCON.3	IE1	External Interrupt 1 **Note:** The INT1PRG[2] bit must be set in the Interrupt pins configuration SFR (INTPR, 0xFF) to allow the INT1 signal into the chip
TF1	TCON.7	TF1	Timer 1
RI + TI	SCON.1	TI	Transmit Interrupt
	SCON.0	RI	Receive Interrupt
TF2 + EXF2	T2CON.7	TF2	Timer 2 overflow flag
	T2CON.6	EXF2	Timer 2 external flag
ITEMP (Temperature ADC)	-		The Temperature ADC interrupt does not have an interrupt flag associated with it.
IPSM (Power Supply)	IPSMF.6	FPSM	PSM interrupt flag
IADE (Energy Measurement DSP)	MIRQSTL.7		Read MIRQSTH, MIRQSTM, MIRQSTL. Write a "0" to a bit to clear and acknowledge the event.

Table 69. Status Flags

Interrupt Source	Flags	Bit Address	Details
ITEMP (Temperature ADC)	-		The Temperature ADC interrupt does not have an status flag associated with it.
ISPI/I2CI	SPISTAT		SPI Interrupt Status register

	I2CSTAT		I²C Interrupt Status register
IRTC	TIMECON.7		RTC Midnight flag
	TIMECON.2		RTC Alarm flag
WDT (Watchdog Timer)	WDCON.2	WDS	Watchdog Timeout flag

A functional block diagram of the interrupt system is shown in Figure 62. Note that the PSM interrupt is the only interrupt in the highest priority level.

If an external **wakeup event** occurs to wake the ADE75XX/ADE71XX from PSM2, a pending external interrupt will be generated. When the EX0 or EX1 bits are set in the Interrupt Enable SFR (IE, 0xA8) to enable external interrupts, the program counter will be loaded with the IE0 or IE1 interrupt vector. The IE0 and IE1 interrupt flags in the TCON register will not be affected by events that occur when the 8052 MCU core is shut down during PSM2 — see the Power Supply Monitor Interrupt (PSM) section.

The RTC, temperature ADC and I2C/SPI interrupts are latched such that pending interrupts cannot be cleared without entering their respective interrupt service routines. Clearing the RTC Midnight and Alarm flags will not clear a pending RTC interrupt. Similarly, clearing the I2C/SPI status bits in the SPI Interrupt Status Register SFR (SPISTAT, 0xEA) will not cancel a pending I2C/SPI interrupt. These interrupts will remain pending until the RTC or I2C/SPI interrupt vectors are enabled. Their respective interrupt service routines will be entered shortly thereafter.

Figure 62 shows how the interrupts are cleared when the interrupt service routines are entered. Some interrupts with multiple interrupt sources are not automatically cleared, specifically the PSM, ADE, UART and Timer 2 interrupt vectors. Note that the INT0 and INT1 interrupts are only cleared if the external interrupt is configured to be triggered by a falling edge, by setting IT0 in the Timer/Counter 0 and 1 Control SFR (TCON, 0x88). If INT0 or INT1 is configured to interrupt on a low level, the interrupt service routine will be reentered until the respective pin goes high.

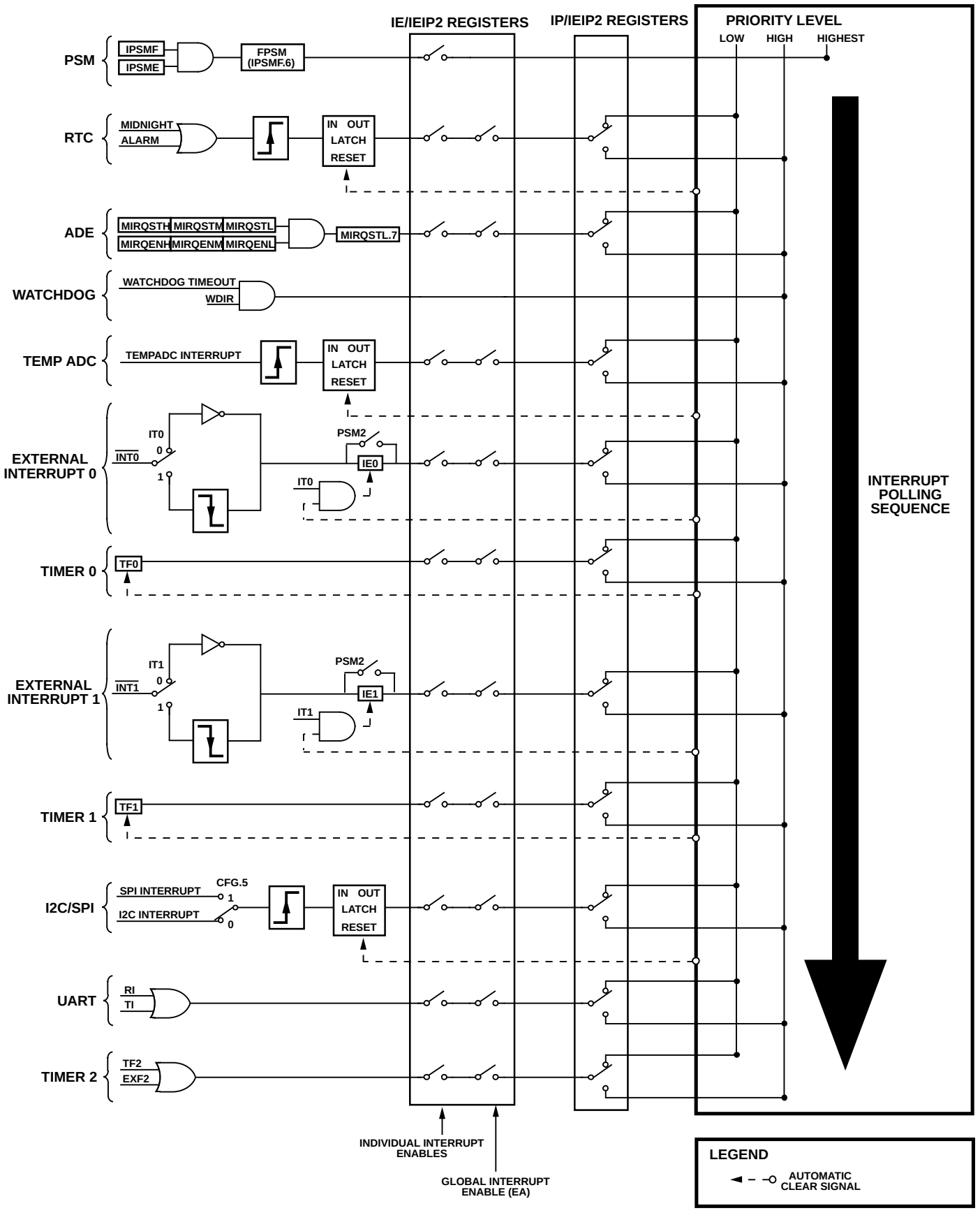

IE/IEIP2 REGISTERS
IP/IEIP2 REGISTERS
PRIORITY LEVEL
LOW
HIGH
HIGHEST
PSM
IPSMF
IPSME
FPSM (IPSMF.6)
RTC
MIDNIGHT
ALARM
IN OUT LATCH RESET
ADE
MIRQSTH MIRQSTM MIRQSTL
MIRQENH MIRQENM MIRQENL
MIRQSTL.7
WATCHDOG
WATCHDOG TIMEOUT
WDIR
TEMP ADC
TEMPADC INTERRUPT
IN OUT LATCH RESET
EXTERNAL INTERRUPT 0
IT0
INT0
0
1
PSM2
IE0
IT0
TIMER 0
TF0
EXTERNAL INTERRUPT 1
IT1
INT1
0
1
PSM2
IE1
IT1
TIMER 1
TF1
I2C/SPI
SPI INTERRUPT
I2C INTERRUPT
CFG.5
1
0
IN OUT LATCH RESET
UART
RI
TI
TIMER 2
TF2
EXF2
INTERRUPT POLLING SEQUENCE
INDIVIDUAL INTERRUPT ENABLES
GLOBAL INTERRUPT ENABLE (EA)
LEGEND
AUTOMATIC CLEAR SIGNAL

Figure 62: Interrupt System Functional Block Diagram

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. When the interrupt service routine has been completed, the program counter is popped off the stack by a RETI instruction. This allows program execution to resume from where it was interrupted. The interrupt vector addresses are shown in Table 70.

Table 70. Interrupt Vector Addresses

Source	Vector Address
IE0	0x0003
TF0	0x000B
IE1	0x0013
TF1	0x001B
RI + TI	0x0023
TF2 + EXF2	0x002B
ITEMP (Temperature ADC)	0x0033
ISPI/I2CI	0x003B
IPSM (Power Supply)	0x0043
IADE (Energy Measurement DSP)	0x004B
IRTC	0x0053
WDT (Watchdog Timer)	0x005B

INTERRUPT LATENCY

The 8051 architecture requires that at least one instruction executes between interrupts. To ensure this, the 8051 MCU core hardware prevents the program counter from jumping to an ISR immediately after completing a RETI instruction or an access of the IP and IE registers.

The shortest interrupt latency is 3.25 instruction cycles, 800ns with a clock of 4.096MHz. The longest interrupt latency for a high priority interrupt results when a pending interrupt is generated during a low priority interrupt RETI, followed by a multiply instruction. This results in a maximum interrupt latency of 16.25 instruction cycles, 4us with a clock of 4.096MHz.

CONTEXT SAVING

When the 8052 vectors to an interrupt, only the program counter is saved on the stack. Therefore the interrupt service routine must be written to ensure that registers that are used in the main program are restored to their pre-interrupt state. Common registers that may be modified in the ISR are the accumulator, and the PSW register. Any general purpose registers that are used as scratchpads in the ISR should also be restored before exiting the interrupt. The example 8051 code shown below shows how to restore some commonly used registers:

```
GeneralISR:
; save the current Accumulator value
        PUSH    ACC
; save the current status and register bank selection
        PUSH    PSW

; service interrupt
…

; restore the status and register bank selection
        POP     PSW
; restore the accumulator
        POP     ACC
        RETI
```

WATCHDOG TIMER

The watchdog timer generates a device reset or interrupt within a reasonable amount of time if the ADE75XX/ADE71XX enters an erroneous state, possibly due to a programming error or electrical noise. The watchdog is enabled by default with a time out of 2 seconds and will create a system reset if not cleared within 2 seconds. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WatchDog Timer SFR (WDCON, 0xC0).

The watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the WDE bit within a predetermined amount of time (see the PRE3…0 bits in WatchDog Timer SFR (WDCON, 0xC0)). The watchdog timer is clocked from the 32.768 kHz external crystal connected between the CLKIN and CLKOUT pins. The WDCON SFR can be written only by user software if the double write sequence described in Table 71 is initiated on every write access to the WDCON SFR.

In order to prevent any code from inadverdently disabling the watchdog, a watchdog protection can be activated. This watchdog protection locks in the watchdog enable and event settings so that they cannot be changed by user code. The protection is activated by clearing a watchdog protection bit in the Flash memory. The watchdog protection bit is the most significant bit at the address 0x3FFA of the Flash memory. When this bit is cleared, the WDIR bit is forced to 0 and the WDE bit is forced to 1. Note that the sequence for configuring the flash protection bits must be followed to modify the watchdog protection bit at 0x3FFA—see the Protecting the Flash section.

Table 71. WatchDog Timer SFR (WDCON, 0xC0)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7-4	0xC7 – 0xC4	PRE[3:0]	7	Watchdog pre-scaler. In normal mode, the 16-bit watchdog timer is clocked by the input clock (32.768kHz). The PRE bits set which of the upper bits of the counter are used as the watchdog output following: $t_{watchdog} = 2^{PRE} \times \frac{2^9}{CLKIN}$ [3:0] Watchdog Timeout 0000 15.6ms 0001 31.2ms 0010 62.5ms 0011 125ms 0100 250ms 0101 500ms 0110 1s 0111 2s 1000 0 Automatic Reset 1001 0 Serial download reset 1010 to 1111 Not a valid selection
3	0xC3	WDIR	0	Watchdog interrupt response bit. When clear, watchdog will generate a system reset when the watchdog time out period has expired When set, the watchdog will generate a interrupt when the watchdog time out period has expired.
2	0xC2	WDS	0	WDS Watchdog status bit. This bit is set to indicate that a watchdog timeout has occurred. WDS is cleared by writing a zero or by an external hardware reset. A watchdog reset will not clear WDS. The bit can therefore be used to distinguish between a watchdog reset and a hardware reset from the RESET pin.
1	0xC1	WDE	1	WDE Watchdog enable bit. When set, enables the watchdog and clears its counter (e.g. 2 above). The watchdog counter is subsequently cleared again whenever the WDE bit is set. If the watchdog is not cleared within its selected timeout period it will generate a system reset or watchdog interrupt, depending on the WDIR bit.
0	0xC0	WDWR	0	WDWR Watchdog write enable bit. To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the following instruction must be a write instruction to the WDCON SFR. This sequence is

				necessary so that the WDCON SFR is protected from code execution upsets that might unintentionally modify this SFR. Interrupts should be disabled during this operation due to the consecutive instruction cycles. e.g. Disable Watch dog CLR EA SETB WDWR CLR WDE SETB EA

Table 72. WatchDog and Flash protection byte in Flash (Flash Address = 0x3FFA)

Bit Location	Bit Name	Default Value	Description
7	WDPROT_PROTKY7	1	This bit holds the protection for the Watchdog timer and the 7th bit of the Flash protection key. When this bit is cleared, the watchdog enable and event, selected by WDE and WDIR cannot be changed by user code. The watchdog configuration is then fixed to WDIR=0 and WDE=1. The watchdog timeout in PRE[3:0] can still be modified by user code. The value of this bit is also used to set the Flash protection key. If this bit is cleared to protect the watchdog, then the default value for the Flash protection key is 0x7F instead of 0xFF—see the Protecting the Flash section for more information on how to clear this bit.
7-0	PROTKY[7:0]	0xFF	These bits hold the flash protection key. The content of this Flash address is compared to the Flash Protection Key SFR (PROTKY, 0xBB) when the protection is being set or changed. If the two values match, the new protection is written to the Flash addresses 0x3FFF to 0x3FFB. see the Protecting the Flash section for more information on how to configure these bits.

Watchdog Timer Interrupt

If the watchdog timer is not cleared within the watchdog timeout period, a system reset will occur unless the watchdog timer interrupt is enabled. The watchdog timer interrupt enable bit is located in the WatchDog Timer SFR (WDCON, 0xC0). Enabling the watchdog timer interrupt allows the program to examine the stack or other variables that could have led the program astray. The watchdog timer interrupt also allows the watchdog to be used as a long interval timer.

Note that the Watchdog Timer Interrupt is automatically configured as a high priority interrupt. This interrupt cannot be disabled by the EA bit in the IE register. Even if all of the other interrupts are disabled, the watchdog is kept active to watch over the program.

LCD DRIVER

The LCD module is capable of directly driving an LCD panel of 24 x 4 segments without compromising any ADE75XX/ADE71XX functionalities. Using shared pins, the driver can accommodate an LCD with up to 26 x 4 segments. It is capable of driving LCDs with 2x, 3x and 4x multiplexing. LCD waveform voltages generated through internal charge pump circuitry support up to 5V LCDs. An external resistor ladder for LCD waveform voltage generation is also supported.

The ADE75XX/ADE71XX has an embedded LCD control circuit, LCD driver and power supply circuit. The LCD module is functional in all Operating modes.

LCD SFR REGISTER LIST

There are six LCD control registers that configure the driver for the specific type of LCD in the end system and set up the user display preferences. The LCD Configuration SFR (LCDCON, 0x95), LCD Configuration X SFR (LCDCONX, 0x9C) and LCD Configuration Y SFR (LCDCONY, 0xB1) SFRs contains general LCD driver configuration information including the LCD enable and reset, as well as method of LCD voltage generation and the multiplex level. The LCD Clock SFR (LCDCLK, 0x96) configures timing settings for LCD frame rate and blink rate. LCD pins are configured for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).

Table 73. LCD Driver SFRs

SFR address (hex)	R/W	Name	Description
0x95	R/W	LCDCON	LCD Configuration SFR
0x96	R/W	LCDCLK	LCD Clock
0x97	R/W	LCDSEGE	LCD Segment Enable
0x9C	R/W	LCDCONX	LCD Configuration X
0xAC	R/W	LCDPTR	LCD Pointer
0xAE	R/W	LCDDAT	LCD Data
0xB1	R/W	LCDCONY	LCD Configuration Y
0xED	R/W	LCDSEGE2	LCD Segment Enable 2
0xF4	R/W	PERIPH	Peripheral Configuration

Table 74. LCD Configuration SFR (LCDCON, 0x95)

Bit Location	Bit Mnemonic	Default Value	Description
7	LCDEN	0	LCD enable. If this bit is set, the LCD driver is enabled.
6	LCDRST	0	LCD data registers are reset to zero. If this bit is set, the LCD data registers will be reset to zero.
5	BLINKEN	0	Blink Mode enable bit. If this bit is set, blink mode is enabled. The blink mode is configured by the BLKMOD[1:0] and BLKFREQ[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96)
4	LCDPSM2	0	Force LCD off when in PSM2 (Sleep mode). 0 The LCD is disabled or enabled in PSM2 by LCDEN bit. 1 The LCD is disabled in PSM2 regarless of LCDEN setting.
3	CLKSEL	0	LCD clock selection f_{LCDCLK} 0 2048Hz 1 128Hz
2	BIAS	0	Bias Mode 0 1/2

			1	1/3	
1-0	LMUX[1:0]	0	LCD Multiplex level		
			LMUX[1:0]		
			0	0	Reserved
			0	1	2x FP27/COM3 is used as FP27 FP28/COM2 is used as FP28
			1	0	3x FP27/COM3 is used as FP27 FP28/COM2 is used as COM2
			1	1	4x FP27/COM3 is used as COM3 FP28/COM2 is used as COM2

Table 75. LCD Configuration X SFR (LCDCONX, 0x9C)

Bit Location	Bit Mnemonic	Default Value	Description
7	Reserved	0	Reserved
6	EXTRES	0	External Resistor Ladder selection bit. 0 External resistor ladder is disabled. Charge pump is enabled. 1 External resistor ladder is enabled. Charge pump is disabled.
5-0	BIASLVL[5:0]	0	Bias Level Selection bits. See Table 76.

Table 76. LCD bias voltage when contrast control is enabled

BLVL[5]	V_A (V)	1/2 Bias		1/3 Bias	
		V_B	V_C	V_B	V_C
0	$V_{ref} \times \frac{BLVL[4:0]}{31}$	$V_B = V_A$	$V_C = 2 \times V_A$	$V_B = 2 \times V_A$	$V_C = 3 \times V_A$
1	$V_{ref} \times \left(1 + \frac{BLVL[4:0]}{31}\right)$				

Table 77. LCD Configuration Y SFR (LCDCONY, 0xB1)

Bit Location	Bit Mnemonic	Default Value	Description
7	Reserved	0	This bit should be kept cleared for proper operation
6	INV_LVL	0	Frame Inversion Mode Enable bit If this bit is set, frames are inverted every other frame If this bit is cleared, frames are not inverted
5-2	Reserved	0	These bits should be kept cleared for proper operation
1	UPDATEOVER	0	Update finished flag bit. This bit is updated by LCD driver. When set, indicates that the LCD memory has been updated and a new frame has begun.
0	REFRESH	0	Refresh LCD data memory bit, this bit should be set by user. When set, the LCD driver does not use the data in the LCD data registers to update display. The LCD data registers can be updated by the 8052. When clear, the LCD driver will use the data in the LCD data registers to update display at the next frame.

Table 78. LCD Clock SFR (LCDCLK, 0x96)

Bit Location	Bit Mnemonic	Default Value	Description
7-6	BLKMOD[1:0]	0	Blink Mode Clock Source Configuration bits BLKMOD[1:0] 0 0 The blink rate is controlled by software. The display is OFF. 0 1 The blink rate is controlled by software. The display is ON. 1 0 The blink rate is 2 Hz 1 1 The blink rate is set by BLKFREQ[1:0]
5-4	BLKFREQ[1:0]	0	Blink Rate Configuration bits These bits control LCD blink rate if BLKMOD[1:0]=11 BLKFREQ[1:0] Blink rate (Hz) 0 0 1 0 1 1/2 1 0 1/3 1 1 1/4
3-0	FD[3:0]	0	LCD Frame Rate Selection bits. See Table 79 and Table 80.

Table 79. LCD frame rate selection for f_{LCDCLK}=2048Hz (LCDCON[3]=0)

				2x multiplexing		3x multiplexing		4x multiplexing	
FD3	FD2	FD1	FD0	f_{LCD}(Hz)	Frame Rate (Hz)	f_{LCD}(Hz)	Frame Rate (Hz)	f_{LCD}(Hz)	Frame Rate (Hz)
0	0	0	1	256	128	512	170.7	512	128
0	0	1	0	170.7	85.3	341.3	113.8	341.3	85.3
0	0	1	1	128	64	256	85.3	256	64
0	1	0	0	102.4	51.2	204.8	68.3	204.8	51.2
0	1	0	1	85.3	42.7	170.7	56.9	170.7	42.7
0	1	1	0	73.1	36.6	146.3	48.8	146.3	36.6
0	1	1	1	64	32	128	42.7	128	32
1	0	0	0	56.9	28.5	113.8	37.9	113.8	28.5
1	0	0	1	51.2	25.6	102.4	34.1	102.4	25.6
1	0	1	0	46.5	23.25	93.1	31	93.1	23.25
1	0	1	1	42.7	21.35	85.3	28.4	85.3	21.35
1	1	0	0	39.4	19.7	78.8	26.3	78.8	19.7
1	1	0	1	36.6	18.3	73.1	24.4	73.1	18.3
1	1	1	0	34.1	17.05	68.3	22.8	68.3	17.05
1	1	1	1	32	16	64	21.3	64	16
0	0	0	0	16	8	32	10.7	32	8

Table 80. LCD frame rate selection for f_{LCDCLK}=128Hz (LCDCON[3]=1)

					2x multiplexing	3x multiplexing	4x multiplexing
FD3	FD2	FD1	FD0	f_{LCD}(Hz)	Frame Rate (Hz)	Frame Rate (Hz)	Frame Rate (Hz)
1	1	1	1	128	64	42.7	32
0	0	0	0	64	32	21.3	16
0	0	0	1	32	16	10.7	8
0	0	1	0	21.3	10.6	10.7	8
0	0	1	1	16	8	10.7	8

: Boxes shaded in grey are not within the range of typical LCD frame rates

Table 81. LCD Segment Enable SFR (LCDSEGE, 0x97)

Bit Location	Bit Mnemonic	Default Value	Description
7	FP25EN	0	FP25 Function Select bit 0 General Purpose I/O 1 LCD Function
6	FP24EN	0	FP24 Function Select bit 0 General Purpose I/O 1 LCD Function
5	FP23EN	0	FP23 Function Select bit 0 General Purpose I/O 1 LCD Function
4	FP22EN	0	FP22 Function Select bit 0 General Purpose I/O 1 LCD Function
3	FP21EN	0	FP21 Function Select bit 0 General Purpose I/O 1 LCD Function
2	FP20EN	0	FP20 Function Select bit 0 General Purpose I/O 1 LCD Function
1-0	FDELAY	0	Delay before powerdown? FDELAY[1:0] 0 0 No timeout 0 1 2 cycles 1 0 4 cycles 1 1 8 cycles

Table 82. LCD Pointer SFR (LCDPTR, 0xAC)

Bit Location	Bit Mnemonic	Default Value	Description

7	W/R	0	Read or Write LCD bit If this bit is set, the data in LCDDAT will be written to the address indicated by the bits LCDPTR[5 :0]
6	RESERVED	0	Reserved
5-0	ADDRESS	0	LCD Memory Address - See Table 85.

Table 83. LCD Data SFR (LCDDAT, 0xAE)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	LCDDATA	0	Data to be written into or read out of the LCD Memory SFRs.

Table 84. LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)

Bit Location	Bit Mnemonic	Default Value	Description
7-4	RESERVED	0	Reserved
3	FP19EN	0	FP19 Function Select bit 0 General Purpose I/O 1 LCD Function
2	FP18EN	0	FP18 Function Select bit 0 General Purpose I/O 1 LCD Function
1	FP17EN	0	FP17 Function Select bit 0 General Purpose I/O 1 LCD Function
0	FP16EN	0	FP16 Function Select bit 0 General Purpose I/O 1 LCD Function

Peripheral Configuration SFR (PERIPH, 0xF4)

Bit Location	Bit Mnemonic	Default Value	Description		
7	RXFLAG	0	If set, indicates that a RX Edge event triggered wakeup from PSM2		
6	VSWSOURCE	1	Indicates the power supply that is connected internally to V_{SW}. 0 $V_{SW}=V_{BAT}$ 1 $V_{SW}=V_{DD}$		
5	VDD_OK	1	If set, indicates that VDD power supply is ok for operation		
4	PLL_FLT	0	If set, indicates that PLL is not locked		
3	REF_BAT_EN	0	If set, Internal voltage reference enabled in PSM2 mode. This bit should be set if LCD On in PSM2 mode.		
2	Reserved	0			
1-0	RXPROG[1:0]	00	Controls the function of the P1.0/RX pin.		
			RXPROG [1:0]		Function
			0	0	GPIO
			0	1	RX with wakeup disabled
			1	1	RX with wakeup enabled

LCD SETUP

The LCD Configuration SFR (LCDCON, 0x95) configures the LCD module to drive the type of LCD in the user end system. The BIAS and LMUX[1:0] bits in this SFR should be set according to the LCD specifications.

The COM2/FP28 and COM3/FP27 pins default to LCD segment lines. Selecting the 3x multiplex level in the LCD Configuration SFR (LCDCON, 0x95) by setting LMUX[1:0] to 2d, changes the FP28 pin functionality to COM2. The 4x multiplex level selection, LMUX[1:0]=3d, changes the FP28 pin to COM2 and the FP27 pin to COM3.

LCD segments FP0-FP15 are enabled by default. Additional pins are selected for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and LCD Segment Enable 2 SFR (LCDSEGE2, 0xED) where there are individual enable bits for segment pins FP16-25. The LCD pins do not have to be enabled sequentially. For example, if the alternate function of FP23, the timer 2 input, is required, then any of the other shared pins, FP16-25, could be enabled instead.

The Display Element Control section contains details about setting up the LCD data memory to turn individual LCD segments ON and OFF. Setting the LCDRST bit in the LCD Configuration SFR (LCDCON, 0x95) will reset the LCD data memory to its default, zero. A power on reset also clears the LCD data memory.

LCD TIMING AND WAVEFORMS

An LCD segment acts like a capacitor that is charged and discharged at a certain rate. The rate at which these capacitors are charged and discharged, the refresh rate, determines the visual characteristics of the LCD. A slow refresh rate will result in the user being able to see the LCD blink on and off in between refreshes. A fast refresh rate will present a screen that appears to be lit up continuously. However, a faster refresh rate consumes more power.

The frame rate, or refresh rate, for the LCD module is derived from the LCD clock, f_{LCDCLK}. The LCD clock is selected as 2048Hz or 128Hz by the CLKSEL bit in the LCD Configuration X SFR (LCDCONX, 0x9C). The minimum refresh rate that is needed for the LCD to appear solid, without blinking, is independent of the multiplex level.

The LCD waveform frequency, f_{LCD}, is the frequency at which the LCD switches which common line is active. Thus the LCD waveform frequency depends heavily on the multiplex level. The frame rate and LCD waveform frequency are set by f_{LCDCLK}, the multiplex level and the FD[3:0] frame rate selection bits in the LCD Clock SFR (LCDCLK, 0x96).

The LCD module provides 16 different frame rates for f_{LCDCLK}=2048Hz, ranging from 8 to 128Hz for an LCD with 4x multiplexing. There are fewer options available with f_{LCDCLK}=128Hz, ranging from 8 to 32Hz for a 4x multiplexed LCD. The 128Hz clock is beneficial for battery operation because it consumes less power than the 2048Hz clock. The frame rate is set by the FD[3:0] bits in the LCD Clock SFR (LCDCLK, 0x96)—see Table 79 and Table 80.

The LCD waveform is inverted at twice the LCD waveform frequency, f_{LCD}. This way each frame has an average DC offset of zero. ADC offset would degrade the lifetime and performance of the LCD.

BLINK MODE

Blink mode is enabled by setting the BLINKEN bit in the LCD Configuration SFR (LCDCON, 0x95). This mode is used to alternate between LCD on and off states so that the LCD screen appears to blink. There are two blinking modes: a software controlled blink mode and an automatic blink mode.

Software Controlled Blink Mode

The LCD blink rate can be controlled by user code with the BLKMOD[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96) by toggling the bits to turn the display on and off at a rate determined by the MCU code.

Automatic Blink Mode

There are five blink rates available if the RTC peripheral is enabled (enable the RTC by…xxx). These blink rates are selected by the BLKMOD[1:0] and BLKFREQ[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96) – see Table 78.

DISPLAY ELEMENT CONTROL

A bank of 15 bytes of data memory located in the LCD module controls the on or off state of each segment of the LCD. The LCD data memory is stored in addresses 0 through 14 in the LCD module. Each byte configures the on and off states of two segment lines. The LSBs store the state of the even numbered segment lines and the MSBs store the state of the odd numbered segment lines. For example, LCD data address zero refers to segment lines one and zero—see Table 85. Note that the LCD data memory is maintained in the PSM2 operating mode.

Table 85. LCD Data Memory accessed indirectly through LCD Pointer SFR (LCDPTR, 0xAC) and LCD Data SFR (LCDDAT, 0xAE)

LCD Memory Address	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
0Eh					FP28	FP28	FP28	FP28
0Dh	FP27	FP27	FP27	FP27	FP26	FP26	FP26	FP26
0Ch	FP25	FP25	FP25	FP25	FP24	FP24	FP24	FP24
0Bh	FP23	FP23	FP23	FP23	FP22	FP22	FP22	FP22
0Ah	FP21	FP21	FP21	FP21	FP20	FP20	FP20	FP20

09h	FP19	FP19	FP19	FP19	FP18	FP18	FP18	FP18
08h	FP17	FP17	FP17	FP17	FP16	FP16	FP16	FP16
07h	FP15	FP15	FP15	FP15	FP14	FP14	FP14	FP14
06h	FP13	FP13	FP13	FP13	FP12	FP12	FP12	FP12
05h	FP11	FP11	FP11	FP11	FP10	FP10	FP10	FP10
04h	FP9	FP9	FP9	FP9	FP8	FP8	FP8	FP8
03h	FP7	FP7	FP7	FP7	FP6	FP6	FP6	FP6
02h	FP5	FP5	FP5	FP5	FP4	FP4	FP4	FP4
01h	FP3	FP3	FP3	FP3	FP2	FP2	FP2	FP2
00h	FP1	FP1	FP1	FP1	FP0	FP0	FP0	FP0

COM# designates the common lines
FP# designates the segment lines

The LCD data memory is accessed indirectly through the LCD Pointer SFR (LCDPTR, 0xAC)and Table 83. LCD Data SFR (LCDDAT, 0xAE). Moving a value to the LCD Pointer SFR (LCDPTR, 0xAC) selects the LCD data byte to be accessed and initiates a read or write operation—see Table 82.

Writing to LCD Data registers

To update the LCD data memory, first set the LSB of the LCD Configuration Y SFR (LCDCONY, 0xB1) to freeze the data being displayed on the LCD while updating it. Then, move the data to the LCD Data SFR (LCDDAT, 0xAE) prior to accessing the LCD Pointer SFR (LCDPTR, 0xAC). When the MSB of the LCD Pointer SFR (LCDPTR, 0xAC) is set, the content of the LCD Data SFR (LCDDAT, 0xAE) is transferred to the internal LCD data memory designated by the address in the LCD Pointer SFR (LCDPTR, 0xAC). Clear the LSB of the LCD Configuration Y SFR (LCDCONY, 0xB1) when all of the data memory has been updated to allow to use the new LCD set up for display.

Sample 8052 code to update the segments attached to pins FP10 and FP11 on is shown below:

```
ORL     LCDCONY,#01h     ; start updating the data
MOV     LCDDATA,#FFh
MOV     LCDPTR,#80h OR 05h
ANL     LCDCONY,#0FEh   ; update finished
```

Reading LCD Data registers

When the MSB of the LCD Pointer SFR (LCDPTR, 0xAC) is cleared, the content of the LCD Data memory address designated by LCDPTR are transferred to the LCD Data SFR (LCDDAT, 0xAE).

Sample 8052 code to read the contents of LCD data memory address 07h, which holds the on and off state of the segments attached to FP14 and FP15, is shown below:

```
MOV     LCDPTR,#NOT 80h AND 07h
MOV     R1, LCDDATA
```

VOLTAGE GENERATION

The ADE75XX/ADE71XX provides two ways to generate the LCD waveform voltage levels. The on-chip charge pump option can generate 5V. This makes it possible to use 5V LCDs with the 3.3V ADE75XX/ADE71XX. There is also an option to use an external resistor ladder with a 3.3V LCD. The EXTRES bit in the LCD Configuration X SFR (LCDCONX, 0x9C) selects the resistor ladder or charge pump option.

When selecting how to generate the LCD waveform voltages, the following should be considered:

- Power Consumption
- Contrast Control
- Lifetime Performance

Power Consumption

In most LCDs, a high amount of current is required when the LCD waveforms change state. The external resistor ladder option draws a constant amount of current whereas the charge pump circuitry allows dynamic current consumption. If the LCD module is used with the internal charge pump option, when the display is disabled, the voltage generation is disabled, so that no power is consumed by the LCD function. This feature will result in significant power savings if the display is turned off in battery operation.

Contrast control

The electrical characteristics of the liquid in the LCD change over temperature, requiring adjustments in the LCD waveform voltages to ensure a readable display. An added benefit of the internal charge pump voltage generation is a configurable bias voltage that can be compensated over temperature to maintain contrast on the LCD. These compensations can be performed based on the ADE75XX/ADE71XX temperature measurements—see the Temperature, Battery and External Voltage Measurements section. This dynamic contrast control is not easily implemented with external resistor ladder voltage generation.

The LCD bias voltage sets the contrast of the display when the charge-pump provides the LCD waveform voltages. The ADE75XX/ADE71XX provides 64 bias levels selectable using the BLVL bits in the LCD Configuration X SFR (LCDCONX, 0x9C). The voltage level on LCDVA, LCDVB and LCDVC depend on the the Interntal voltage reference value (Vref), BLVL[5:0] selection and the biasing selected as described in Table 76.

Lifetime Performance

DC offset on a segment will degrade its performance over time. The voltages generated through the internal charge pump

switch faster than those generated by the external resistor ladder, reducing the likelihood of a DC voltage being applied to a segment and increasing the lifetime of the LCD.

LCD EXTERNAL CIRCUITRY

The voltage generation selection is made by bit EXTRES in the LCD Configuration X SFR (LCDCONX, 0x9C). This bit is clear by default for charge pump voltage generation but can be set to enable an external resistor ladder.

Charge Pump:

Voltage generation through the charge pump requires external capacitors to store charge. The external connections to VA, VB, and VC as well as VP1 and VP2 are shown in LCD Configuration X SFR (LCDCONX, 0x9C).

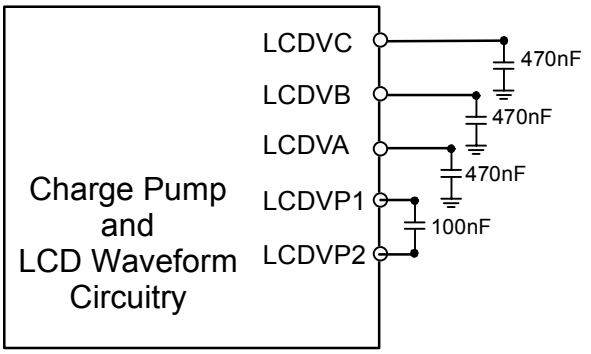


Figure 63: External circuitry for Charge Pump option

External Resistor Ladder:

To enable the external resistor ladder option, set the EXTRES bit in the LCD Configuration X SFR (LCDCONX, 0x9C). When EXTRES=1, the LCD waveform voltages are supplied by the external resistor ladder. Since the LCD voltages are not being generated on-chip, the LCD bias compensation implemented to maintain contrast over temperature and supply is not possible.

The external circuitry needed for the resistor ladder option is shown in Figure 64. The resistors required should be in the range of 10k to 100k and based on the current required by the LCD being used.

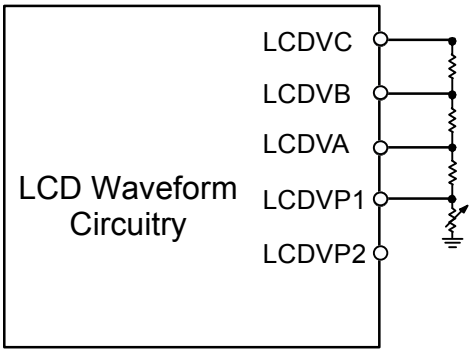


Figure 64: External circuitry for External Resistor Ladder option

LCD FUNCTION IN PSM2

The LCDPSM2 bit in the LCD Configuration SFR (LCDCON, 0x95) and the LCDEN bit in the LCD Configuration SFR (LCDCON, 0x95) control LCD functionality in the PSM2 operating mode. The voltage reference must be enabled during battery mode for the charge pump voltage generation to work. Ensure this by setting REF_BAT_EN in the Peripheral Configuration SFR (PERIPH, 0xF4).

LCDPSM2	LCDEN	Comments
0	0	The display is OFF in PSM2.
0	1	The display is ON in PSM2.
1	X	The display is OFF in PSM2.

Note that the LCD configuration and data memory is retained when the display is turned off.

EXAMPLE LCD SETUP

An example to set up the LCD peripheral for a specific LCD is described below.

Type of LCD: 5V, 4x multiplexed with 1/3 bias, 96 segments
Voltage Generation: Internal Charge Pump
Refresh Rate: 64Hz

A 96 segment LCD with 4x multiplexing requires 96/4=24 segment lines. There are 16 pins that automatically dedicated for use as LCD segments, FP0 to FP15. Eight more pins must be chosen for the LCD function. Since the LCD has 4x multiplexing, all four common lines are used so COM2/FP28 and COM3/FP27 cannot be utilized as segment lines. Based on the alternate functions of the pins used for FP16 through FP25, FP16-23 are chosen for the seven remaining segment lines. These pins will be enabled for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).

To determine contrast setting for this 5V LCD, look in Table 76 to find the BIASLVL[5:0] setting that corresponds to a VC of 5V in 1/3 Bias Mode. The nominal bias level setting for this LCD is BIASLVL[5:0]=[111111].

The LCD is setup with the following 8052 code:

```
; setup LCD pins to have LCD functionality
MOV     LCDSEGE, # 00111100b
MOV     LCDSEGE2, #00001111b

; setup LCDCON for fLCDCLK=2048Hz, 1/3 bias and 4x multiplexing
MOV     LCDCON, #00000111b
; setup LCDCONX for charge pump and BIASLVL[110111]
MOV     LCDCONX, #00110111b
; set up refresh rate for 64Hz with fLCDCLK=2048Hz, from Table 79
MOV     LCDCLK, #00000011b
; set up LCD data registers with data to be displayed using
; LCDPTR and LCDDATA registers
```

```
; turn all segments on FP25 ON and FP26 OFF
ORL     LCDCONY,#01h      ; start data memory refresh
MOV     LCDDAT, #F0H
MOV     LCDPTR, #80h OR 0DH
ANL     LCDCONY,#0FEh     ; end of data memory refresh
ORL     LCDCON,#080h ; enable LCD
```

To setup the same 3.3V LCD for use with an external resistor ladder:

```
; setup LCD pins to have LCD functionality
MOV     LCDSEGE, # 00111100b
MOV     LCDSEGE2, #00001111b

; setup LCDCON for fLCDCLK=2048Hz, 1/3 bias and 4x multiplexing
MOV     LCDCON, #00000111b
; setup LCDCONX for external resistor ladder
MOV     LCDCONX, #01000000b
; set up refresh rate for 64Hz with fLCDCLK=2048Hz, from Table 79
MOV     LCDCLK, #00000011b
; set up LCD data registers with data to be displayed using
; LCDPTR and LCDDATA registers
; turn all segments on FP25 ON and FP26 OFF
ORL     LCDCONY,#01h      ; start data memory refresh
MOV     LCDDAT, #F0H
MOV     LCDPTR, #80h OR 0DH
ANL     LCDCONY,#0FEh     ; end of data memory refresh
ORL     LCDCON,#080h ; enable LCD
```

FLASH MEMORY

FLASH MEMORY OVERVIEW

Flash memory is a type of non-volatile memory that is in-circuit programmable. The default, erased, state of a byte of flash memory is 0xFF. When a byte of flash memory is programmed, the required bits change from one to zero. The flash memory must be erased to turn the zeros back to ones. However, a byte of flash memory cannot be erased individually. The entire segment, or page, of flash memory that contains the byte must be erased.

The ADE75XX/ADE71XX provides 8 or 16kbytes of flash program/information memory. This memory is segmented into 32 pages of 512 bytes each. So, to reprogram one byte of flash memory, the 511 bytes in that page must be erased. The flash memory can be erased by page or all at once in a mass erase. There is a command to verify that a flash write operation has completed successfully. The ADE75XX/ADE71XX flash memory controller also offers configurable flash memory protection.

The 8 or 16 kbytes of flash memory are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download mode provided or using conventional third party memory programmers.

Flash/EE Memory Reliability

The Flash memory arrays on the ADE75XX/ADE71XX are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the specification table, the ADE75XX/ADE71XX flash memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C, +25°C and +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with a minimum endurance figure of 20,000 cycles of operation at 25°C.

Retention is the ability of the Flash memory to retain its programmed data over time. Again, the parts have been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash memory is cycled to its specified endurance limit described previously, before data retention is characterized. This means that the Flash memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 65.

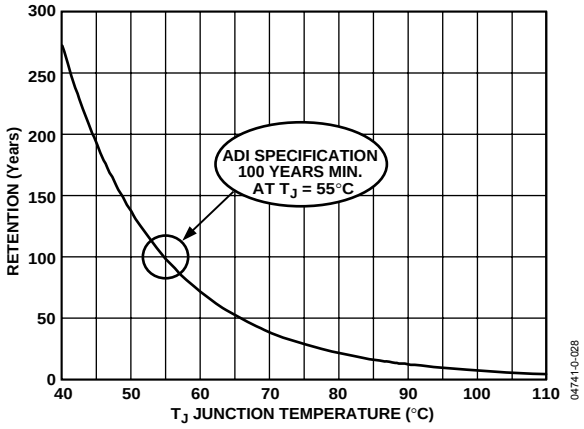


Figure 65. Flash/EE Memory Data Retention

FLASH MEMORY ORGANIZATION

The 8 or 16kbytes of flash memory provided by the ADE75XX/ADE71XX are segmented into 32 pages of 512 bytes each. It is up to the user to decide which Flash memory he would like to allocate for data memory. It is recommended that each page be dedicated solely to program or data memory so that an instance does not arise where the program counter is loaded with data memory instead of an opcode from the program memory or where program memory is erased to update a byte of data memory.

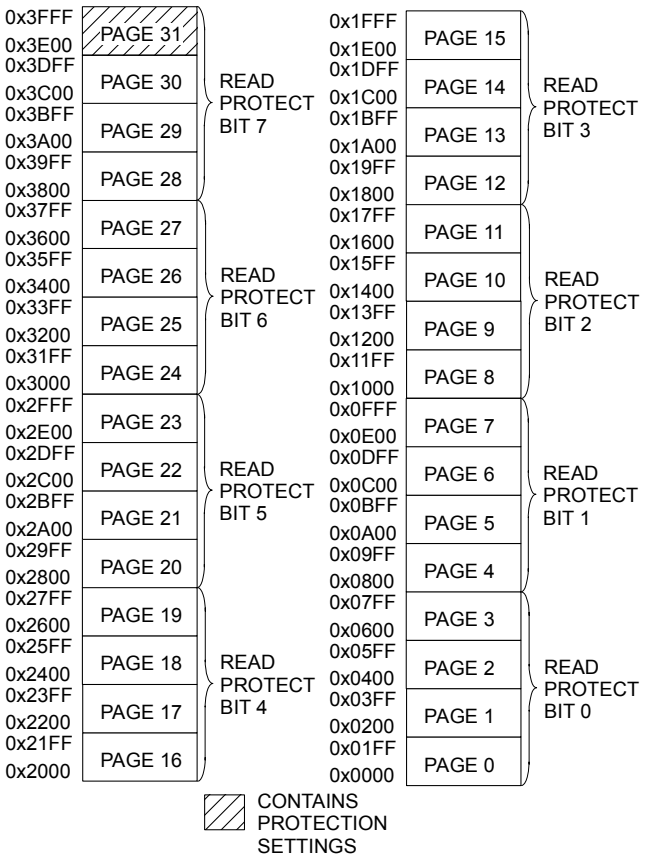


Figure 66: Flash Memory Organization

The flash memory can be protected from read or write/erase access. The protection is implemented in part of the last page of the flash memory, Page 31. Four of the bytes from this page are used to set up write/erase protection for each of the pages. Another byte is used for configuring read protection of the flash memory. The read protection is selected for groups of four pages. Finally, there is a byte used to store the key required for modifying the protection scheme. If any code protection is required, the last page of flash memory must be write/erase protected at a minimum. The implication of write/erase protecting the last page is that the content of the 506 bytes in this page that are available to the user must not change.

Thus it is recommended that if code protection is enabled, this last page should be used for program memory only if the firmware does not need to be updated in the field. If the firmware must be protected and can be updated at a future date, the last page should be used only for constants used by the program code that will not need to be read during emulation or debug.

Therefore, Pages 0 through 30 are for general program and data memory use. It is recommended that Page 31 is used for constants or code that will not need to be updated. Note that the last 6 bytes of Page 31 are reserved for protecting the flash memory.

USING THE FLASH MEMORY

The 8k or 16 kbytes of Flash memory are configured as 16 or 32 pages, each of 512 bytes. As with the other ADE75XX/ADE71XX peripherals, the interface to this memory space is via a group of registers mapped in the SFR space – see . A data register, EDATA, holds the byte of data to be accessed. The byte of flash memory is addressed via the EADRH and EADRL registers. The Flash SFRs

Table 86. Flash SFRs

SFR	Address	Default Value	Bit Addressable	Description
ECON	0xB9	0x00	No	Flash Control
FLSHKY	0xBA	0xFF	No	Flash Key
PROTKY	0xBB	0xFF	No	Flash Protection Key
EDATA	0xBC	0x00	No	Flash Data
PROTB0	0xBD	0xFF	No	Flash W/E Protection 0
PROTB1	0xBE	0xFF	No	Flash W/E Protection 1
PROTR	0xBF	0xFF	No	Flash Read protection
EADRL	0xC6	0x00	No	Flash Low address
EADRH	0xC7	0x00	No	Flash High address

Finally, ECON is an 8-bit control register that can be written to with one of seven Flash memory access commands to trigger various read, write, erase, and verify functions. Figure 67 demonstrates the steps required for access to the flash memory.

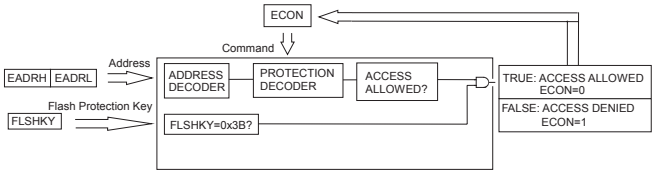


Figure 67: Flash Memory Read/Write/Erase Protection Block Diagram

ECON—Flash/EE Memory Control SFR

Programming Flash memory is done through the Flash memory control Flash Control SFR (ECON, 0xB9). This SFR allows the user to read, write, erase, or verify the 16 or 32 kbytes of Flash memory. As a method of security, a key must be written to the FLSHKY register to initiate any user access to the

flash memory. Upon completion of the flash memory operation, the FLSHKY register is reset such that it must be written prior to another flash memory operation. Requiring the key to be set before an access to the flash memory decreases the likelihood of user code or data being overwritten by a program that has run amuck.

The program counter, PC, is held on the instruction where the ECON register is written to until the flash memory controller is done performing the requested operation. Then the PC increments to continue with the next instruction. Any interrupts requests that occur while the flash controller is performing an operation are not handled until the flash operation is complete. All peripherals, such as timers and counters, will continue to operate as configured throughout the flash memory access.

Table 87. Flash Control SFR (ECON, 0xB9)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	ECON	0	1 Write byte: The value in EDATA is written to the Flash memory, at the page address given by EADRH and EARDL. Note that the byte being addressed must be pre-erased 2 Erase page: A 512-byte page of Flash memory address is erased. The page is selected by the address in EADRH/L. Any address in the page can be written to EADRH/L to select it for erasure. 3 Erase all: All 16 or 32kbytes of the Flash memory are erased. Note: This command is used during serial and parallel download modes but should not be executed by user code. 4 Read byte: The byte in the Flash memory, addressed by EADRH/L, is read into EDATA. 5 Erase page and write byte: The page that holds the byte addressed by EADRH/L is erased. Then, data in EDATA is written to the byte of flash memory addressed by EADRH/L. 8 Protect code: See Protecting the Flash.

Table 88. Flash Key SFR (FLSHKY, 0xBA)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	FLSHKY	0xFF	The content of this SFR is compared to the Flash key – 0x3B. If the two values match the next ECON operation is allowed - see Protecting the Flash.

Table 89. Flash Protection Key SFR (PROTKY, 0xBB)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	PROTKY	0xFF	The content of this SFR is compared to the Flash memory location at address 0x3FFA. If the two values match, the update of the Write/Erase and Read protection set up is allowed - see Protecting the Flash. If the protection Key in the flash is 0xFF, PROTKY SFR value is not used for comparison. The PROTKY SFR is also used to write the protection key in the flash. This is done by writing the desired value in PROTKY and write 0x08 in the ECON SFR. This operation can only be done once.

Table 90. Flash Data SFR (EDATA, 0xBC)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	EDATA	0	Flash pointer data

Table 91. Flash Write/Erase Protection 0 SFR (PROTB0, 0xBD)

Bit	Bit	Default	Description

Location	Mnemonic	Value	
7-0	PROTB0	0xFF	This SFR is used to write the write/erase protection bits for pages 0 to 7 of the Flash memory – see Protecting the Flash. Clearing the bit enables the protection. PROTB0.7: Page 7 PROTB0.6: Page 6 PROTB0.5: Page 5 PROTB0.4: Page 4 PROTB0.3: Page 3 PROTB0.2: Page 2 PROTB0.1: Page 1 PROTB0.0: Page 0

Table 92. Flash Write/Erase Protection 1 SFR (PROTB1, 0xBE)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	PROTB1	0xFF	This SFR is used to write the write/erase protection bits for pages 8 to 15 of the Flash memory – see Protecting the Flash. Clearing the bit enables the protection. PROTB1.7: Page 15 PROTB1.6: Page 14 PROTB1.5: Page 13 PROTB1.4: Page 12 PROTB1.3: Page 11 PROTB1.2: Page 10 PROTB1.1: Page 9 PROTB1.0: Page 8

Table 93. Flash Read Protection SFR (PROTR, 0xBF)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	PROTR	0xFF	This SFR is used to write the read protection bits for pages 0 to 31 of the Flash memory – see Protecting the Flash. Clearing the bit enables the protection. PROTR.7: Page 28 to 31 PROTR.6: Page 24 to 27 PROTR.5: Page 20 to 23 PROTR.4: Page 16 to 19 PROTR.3: Page 12 to 15 PROTR.2: Page 8 to 11 PROTR.1: Page 4 to 7 PROTR.0: Page 0 to 3

Table 94. Flash Low Byte Address SFR (EADRL, 0xC6)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	EADRL	0	Flash pointer low byte address This SFR is also used to write the write/erase protection bits for pages 16 to 23 of the Flash memory – see Protecting the Flash. Clearing the bit enables the protection. EADRL.7: Page 23 EADRL.6: Page 22 EADRL.5: Page 21

			EADRL.4: Page 20 EADRL.3: Page 19 EADRL.2: Page 18 EADRL.1: Page 17 EADRL.0: Page 16

Table 95. Flash High Byte Address SFR (EADRH, 0xC7)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	EADRH	0	Flash pointer high byte address This SFR is also used to write the write/erase protection bits for pages 24 to 31 of the Flash memory – see Protecting the Flash. Clearing the bit enables the protection. EADRH.7: Page 31 EADRH.6: Page 30 EADRH.5: Page 29 EADRH.4: Page 28 EADRH.3: Page 27 EADRH.2: Page 26 EADRH.1: Page 25 EADRH.0: Page 24

Flash functions

Sample 8051 code is provided below to demonstrate how to use the Flash functions. For these examples, the byte of flash memory, 0x3C00 is accessed.

Write Byte: Write F3H into flash memory byte 0x3C00.

```
MOV EDATA, #F3h      ; Data to be written
MOV EADRH, #3Ch      ; Setup byte address
MOV EADRL, #00h
MOV FLSHKY, #3Bh     ; Write Flash security key.
MOV ECON, #01H       ; Write Byte
```

Erase Page: Erase the page containing flash memory byte 0x3C00.

```
MOV EADRH, #3Ch      ; Select page through byte address
MOV EADRL, #00h
MOV FLSHKY, #3Bh     ; Write Flash security key.
MOV ECON, #02H       ; Erase Page
```

Erase All: Erase all of the 16 or 32kbyte flash memory

```
MOV FLSHKY, #3Bh     ; Write Flash security key.
MOV ECON, #03H       ; Erase All
```

Read Byte: Read flash memory byte 0x3C00.

```
MOV EADRH, #3Ch      ; Setup byte address
MOV EADRL, #00h
MOV FLSHKY, #3Bh     ; Write Flash security key.
MOV ECON, #04H       ; Read Byte
; Data is ready in EDATA register
```

Erase Page and Write Byte: Erase the page containing flash memory byte 0x3C00 and then write F3H to that address. Note that the other 511 bytes in this page will be erased.

```
MOV EDATA, #F3h      ; Data to be written
MOV EADRH, #3Ch      ; Setup byte address
MOV EADRL, #00h
MOV FLSHKY, #3Bh     ; Write Flash security key.
MOV ECON, #05H       ; Erase page and then write byte
```

PROTECTING THE FLASH

Two forms of protection are offered for this flash memory: read protection and write/erase protection. The read protection ensures that any pages that are read protected will not be able to be read by the end user. The write protection ensures that the flash memory cannot be erased or written over. This protects the end system from tampering and can prevent the code from being overwritten in the event of a runaway program.

Write/erase protection is individually selectable for all of the 16 or 32 pages. Read protection is selected in groups of 4 pages. See Figure 66 for the groupings. The protection bits are stored in the last flash memory locations, addresses 0x3FFA through 0x3FFF– see Figure 68. 4 bytes are reserved for write/erase protection, 1 byte for read protection and another byte to set the protection security key. The user must enable write/erase protection for the last page at a minimum for the entire protection scheme to work.

Remark: The read protection does not prevent MOVC commands from being executed within the code.

There is an additional layer of protection offered by a protection security key. The user can setup a protection security key so that the protection scheme cannot be changed without this key. Once the protection key has been configured, it may not be modified.

Enabling Flash Protection by Code

The protection byts in the Flash can be programmed using Flash controller command and programming ECON to 0x08. The EADRH, EADRL, PROTB1 and PROTB0 bytes are used in this case to store the data to be written to the 32 bits of write protection. Note that the EADRH and EADRL registers are not used as data pointers here, but to store write protection data.

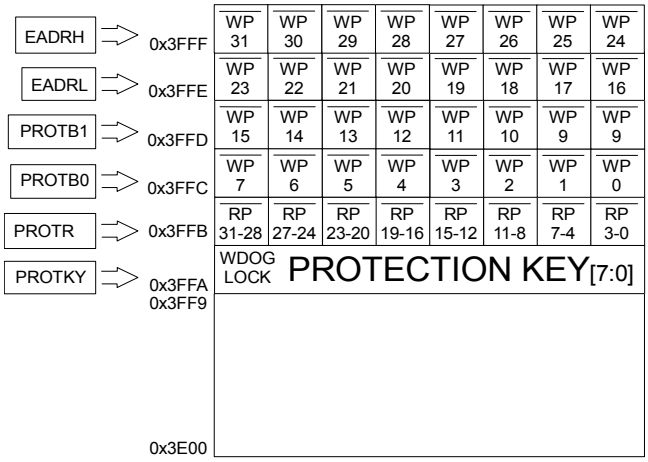


Figure 68: Flash Protection in Page 31

The sequence for writing the protection bits is:

1. Set up the EADRH, EADRL, PROTB1 and PROTB0 registers with the write/erase protection bits. When erased, the protection bits default to 1, like any other bit of Flash memory. The default protection setting is for no protection. To enable protection, write a 0 to the bits corresponding to the pages that should be protected.
2. Set up the PROTR register with the read protection bits. Note that every read protection bit protects four pages. To enable the read protection bit, write a 0 to the bits that should be read protected.
3. To enable the protection key, write to the PROTKY register. If enabled, the protection key will be required to modify the protection scheme. The protection key, flash memory address 0x3FFA defaults to FFH so if the PROTKY register is not written to, it will remain 0xFFH. If the protection key is written to, the PROTKY register must be written with this value every time the protection functionality is accessed. Note that once the protection key is configured, it cannot be modified. Also note that the most significant bit of 0x3FFA is used to enable a lock mechanism for the watchdog settings—see the Watchdog Timer section for more information.
4. Run the protection command by writing 08H to the ECON register.
5. Reset the chip to activate the new protection.

To enable read and write/erase protection for the last page only, use the following 8051 code. Writing the flash protection command to the ECON register initiates programming the protection bits in the flash.

```
; enable write/erase protection on the last page only
MOV EADRH, #07FH
MOV EADRL, #0FFH
MOV PROTB1, #FFH
MOV PROTB0, #FFH

; enable read protection on the last four pages only
MOV PROTR, #07FH

; set up a protection key of 0A3H. This command can be
; omitted to use the default protection key of 0xFF
MOV PROTKY, #0A3H

; write the flash key to the FLSHKY register to enable flash
; access. The flash access key is not configurable.
MOV FLSHKY, #3BH

; write flash protection command to the ECON register
MOV ECON, #08H
```

Enabling Flash Protection by emulator commands

Another way to set the Flash protection bytes is to use some reserved emulator commands available only in download mode. These commands write directly to the SFRs and can be used to duplicate the operation mentioned in the Enabling Flash Protection by Code paragraph. Once these Flash bytes are written, the part can exit emulation mode by reset and the protections will be effective. This method can be used in production and implemented after downloading the program. The commands used for this operation are an extension of the commands listed in the application note uC004 – Understanding the Serial Download Protocol:

- Command with ASCII code 'I' or 0x49 write the data into R0

- Command with ASCII code 'F' or 0x46 write R0 into the SFR address defined in the data of this command

Omitting the protocol defined in uC004, the sequence to load

protections are similar to the sequence presented mentioned in the Enabling Flash Protection by Code paragraph.except that two emulator commands are necessary to replace one assembly command. For example to write the protection value in EADRH the two following commands need to be executed:

- Command 'I ' with Data = Value of protection byte 0x3FFF
- Command 'F' with Data = 0xC7

Following this protocol, the protection can be written to the Flash using the same sequence as mentioned in the Enabling Flash Protection by Code paragraph. When the part is reset the protection will be effective.

Notes on Flash Protection

The flash protection scheme is disabled by default so that none of the pages of the flash are protected from reading or writing/erasing.

The last page must be write/erase protected for the protection scheme to work.

To activate the protection settings, the ADE75XX/ADE71XX must be reset after configuring the protection.

After configuring protection on the last page and resetting the part, protections that have been enabled can only be removed by mass erasing the flash memory. The protection bits are read and erase protected by enabling read and write/erase protection the last page, but the protection bits are never truly write protected. Protection bits can be programmed modified from a 1 to a 0, even after the last page has been protected. In this way, more protection can be added but none can be removed.

The protection scheme is intended to protect the end system. Protection should be disabled while developing and emulating code.

Flash memory timing

Typical program and erase times for the flash memory are as follows:

Command	Bytes Affected	Flash Memory Timing
WRITE BYTE	1 byte	30us
ERASE PAGE	512 bytes	20ms
ERASEALL	16 or 32kbytes	200ms
READ BYTE	1 bytes	100ns
ERASEPAGE and WRITE BYTE	512 bytes	21ms
VERIFY BYTE	1 byte	100ns

Note that the core microcontroller operation is idled until the requested flash memory operation is complete. In practice, this means that even though the Flash operation is typically initiated with a two-machine-cycle MOV instruction (to write to the Flash Control SFR (ECON, 0xB9)), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions such as counter/ timers continue to count as configured throughout this period.

IN CIRCUIT PROGRAMMING

Serial Downloading

The ADE75XX/ADE71XX facilitates code download via the standard UART serial port. The parts enter serial download mode after a reset or a power cycle if the $\overline{\text{SDEN}}$ pin is pulled low through an external 1 kΩ resistor. Once in serial download mode, the hidden embedded download kernel executes. This allows the user to download code to the full 16 or 32 kbytes of Flash memory while the device is in circuit in its target application hardware.

Protection configured in the last page of the ADE75xx/ADE71xx affects whether flash memory can be accessed in serial download mode. Read protected pages cannot be read. Write/erase protected pages cannot be written or erased. The configuration bits cannot be programmed in serial download mode.

TIMERS

The ADE75XX/ADE71XX has three 16-bit timer/ counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware is included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2). All three can be configured to operate either as timers or as event counters.

When functioning as a timer, the TLx register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Because a machine cycle on a single-cycle core consists of one core clock period, the maximum count rate is the core clock frequency.

When functioning as a counter, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin: T0, T1, or T2. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. Because it takes two machine cycles (two core clock periods) to recognize a 1-to-0 transition, the maximum count rate is half the core clock frequency.

There are no restrictions on the duty cycle of the external input signal, but, to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. User configuration and control of all timer operating modes is achieved via the SFRs in Table 96.

Table 96. Timer SFRs

SFR	Address	Bit Addressable	Description
TCON	0x88	Yes	Timer0 and Timer1 Control Register – see Table 98
TMOD	0x89	No	Timer Mode register– see Table 97
TL0	0x8A	No	Timer0 LSB– see Table 101
TL1	0x8B	No	Timer1 LSB– see Table 103
TH0	0x8C	No	Timer0 MSB– see Table 100
TH1	0x8D	No	Timer1 MSB– see Table 102
T2CON	0xC8	Yes	Timer2 Control Register – see Table 99
RCAP2L	0xCA	No	Timer2 Reload/Capture LSB – see Table 107
RCAP2H	0xCB	No	Timer2 Reload/Capture MSB – see Table 106
TL2	0xCC	No	Timer2 LSB – see Table 105
TH2	0xCD	No	Timer2 MSB – see Table 104

TIMER SFR REGISTER LIST

Table 97. Timer/Counter 0 and 1 Mode SFR (TMOD, 0x89)

Bit Location	Bit Mnemonic	Default Value	Description		
7	Gate1	0	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while the $\overline{INT1}$ pin is high and the TR1 control is set. Cleared by software to enable Timer 1 whenever the TR1control bit is set.		
6	C_T1	0	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select the timer operation (input from internal system clock).		
5-4	T1_M1, T1_M0	00	Timer 1 Mode Select bits		
			M1	M0	Description
			0	0	TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler.
			0	1	16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler.

			1	0	8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows.
			1	1	Timer/Counter 1 Stopped.
3	Gate0	0	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.		
2	C_T0	0	Timer 0 Timer or Counter Select Bit. Set by software to the select counter operation (input from T0 pin). Cleared by software to the select timer operation (input from internal system clock).		
1-0	T0_M1, T0_M0	00	Timer 0 Mode Select Bits		
			M1	M0	Description
			0	0	TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler.
			0	1	16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler.
			1	0	8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows.
			1	1	TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

Table 98. Timer/Counter 0 and 1 Control SFR (TCON, 0x88)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0x8F	TF1	0	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	0x8E	TR1	0	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	0x8D	TF0	0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	0x8C	TR0	0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	0x8B	IE1[1]	0	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or by a zero level applied to the external interrupt pin, $\overline{INT1}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
2	0x8A	IT1[1]	0	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.
1	0x89	IE0[1]	0	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{INT0}$, depending on the statue of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
0	0x88	IT0[1]	0	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.

2 These bits are not used to control Timer/Counters 0 and 1, but are used instead to control and monitor the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Table 99. Timer/Counter 2 Control SFR (T2CON, 0xC8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0xCF	TF2	0	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	0xCE	EXF2	0	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	0xCD	RCLK	0	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	0xCC	TCLK	0	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	0xCB	EXEN2	0	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	0xCA	TR2	0	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	0xC9	CNT2	0	Timer 2 Timer or Counter Function Select Bit. Set by the user to select the counter function (input from external T2 pin). Cleared by the user to select the timer function (input from on-chip core clock).
0	0xC8	CAP2	0	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Table 100. Timer 0 High byte SFR (TH0, 0x8C)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TH0	0	Timer 0 Data high byte

Table 101. Timer 0 Low byte SFR (TL0, 0x8A)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TL0	0	Timer 0 Data high byte

Table 102. Timer 1 High byte SFR (TH1, 0x8D)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TH1	0	Timer 1 Data high byte

Table 103. Timer 1 Low byte SFR (TL1, 0x8B)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TL1	0	Timer 1 Data high byte

Table 104. Timer 2 High byte SFR (TH2, 0xCD)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TH2	0	Timer 2 Data high byte

Table 105. Timer 2 Low byte SFR (TL2, 0xCC)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TL2	0	Timer 2 Data high byte

Table 106. Timer 2 Reload/capture High byte SFR (RACP2H, 0xCB)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TH2	0	Timer 2 Reload/capture high byte

Table 107. Timer 2 Reload/capture Low byte SFR (RACP2L, 0xCA)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TL2	0	Timer 2 Reload/capture low byte

TIMER 0 AND TIMER 1

Timer/Counter 0 and 1 Data Registers

Each timer consists of two 8-bit registers: Timer 0 High byte SFR (TH0, 0x8C), Timer 0 Low byte SFR (TL0, 0x8A), Timer 1 High byte SFR (TH1, 0x8D) and Timer 1 Low byte SFR (TL1, 0x8B) These can be used as independent registers or combined into a single 16-bit register, depending on the timers' mode configuration – see Table 100 to Table 103.

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 69 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

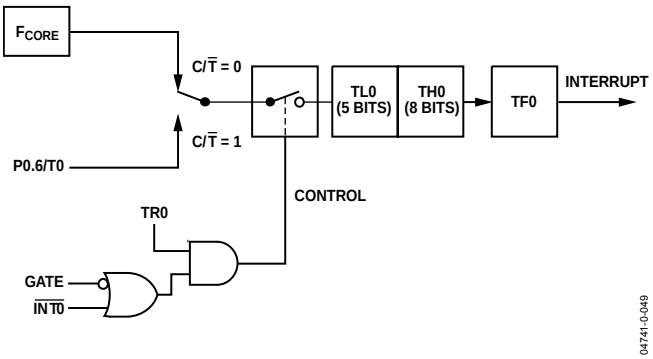


Figure 69. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register.

As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the Timer/Counter 0 and 1 Control SFR (TCON, 0x88); the Gate bit is in Timer/Counter 0 and 1 Mode SFR (TMOD, 0x89). The 13-bit register consists of all 8 bits of Timer 0 High byte SFR (TH0, 0x8C) and the lower 5 bits of Timer 0 Low byte SFR (TL0, 0x8A). The upper 3 bits of Timer 0 Low byte SFR (TL0, 0x8A) are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 70.

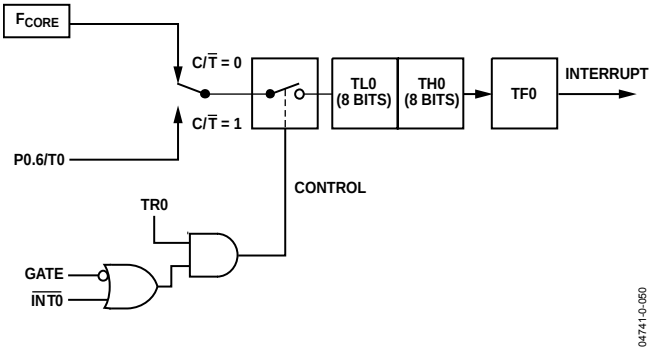


Figure 70. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 71. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

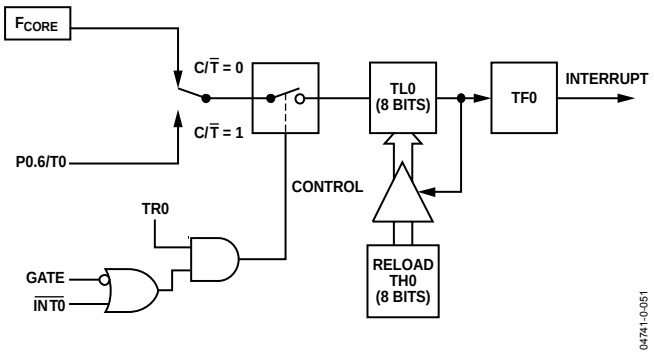


Figure 71. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 72. TL0 uses the Timer 0 control bits C/T, Gate, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

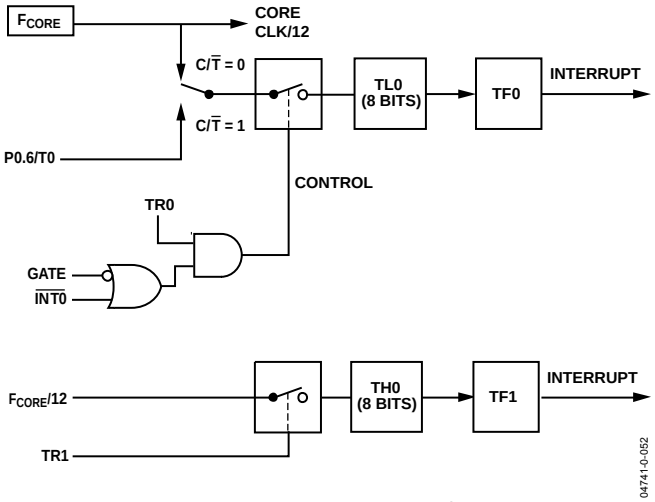


Figure 72. Timer/Counter 0, Mode 3

TIMER 2

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it: Timer 2 High byte SFR (TH2, 0xCD), Timer 2 Low byte SFR (TL2, 0xCC), Timer 2 Reload/capture High byte SFR (RACP2H, 0xCB) and Timer 2 Reload/capture Low byte SFR (RACP2L, 0xCA). These are used as both timer data registers and as timer capture/reload registers – see Table 104 to Table 107.

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the Timer/Counter 2 Control SFR (T2CON, 0xC8) as shown in Table 99 and Table 108.

Table 108. T2CON Operating Modes

RCLK (or) TCLK	CAP2	TR2	Mode
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by bit EXEN2 in Timer/Counter 2 Control SFR (T2CON, 0xC8). If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers Timer 2 Reload/capture High byte SFR (RACP2H, 0xCB) and Timer 2 Reload/capture Low byte SFR (RACP2L, 0xCA), which are preset by software. If EXEN2 = 1, Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 73.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 74. The

baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur, so they do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts, which can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in UART serial interface section.

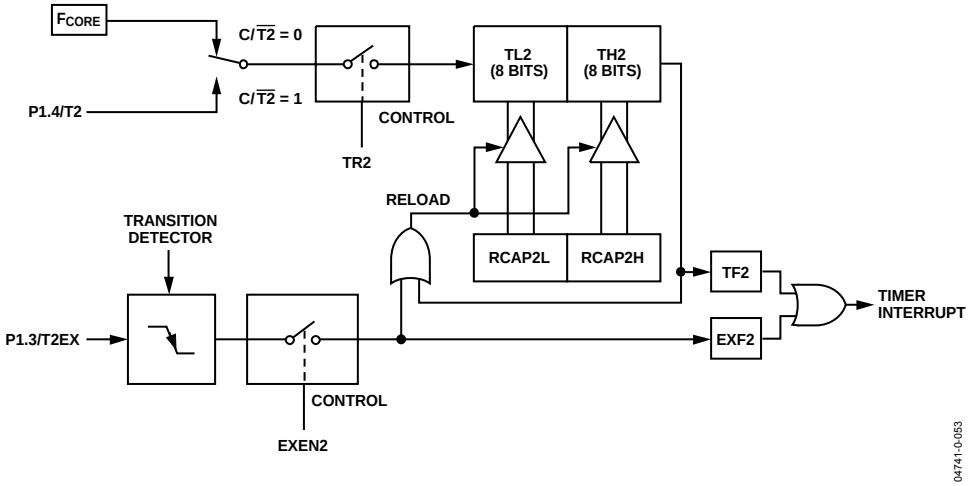


Figure 73. Timer/Counter 2, 16-Bit Autoreload Mode

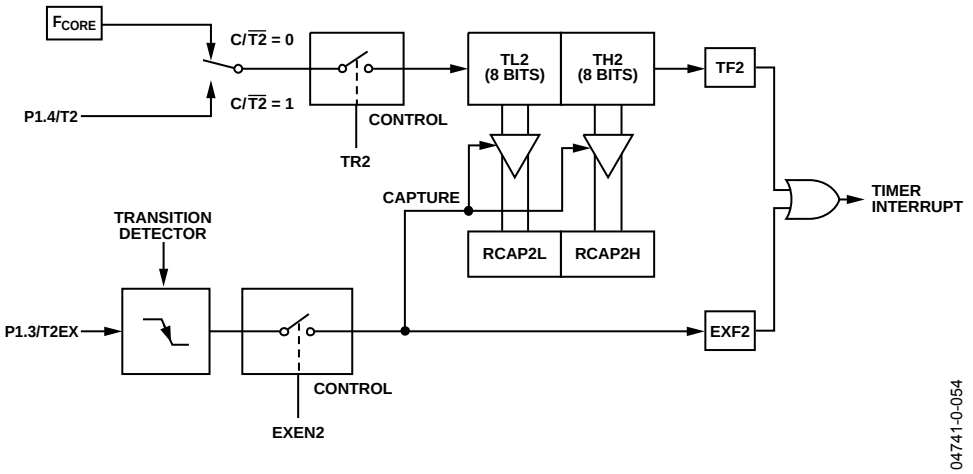


Figure 74. Timer/Counter 2, 16-Bit Capture Mode

PLL

The ADE75xx/ADE71xx is intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple of this frequency to provide a stable 4.096 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 4 or 1.024 MHz. The ADE energy measurement clock is derived from the PLL clock and is maintained at 4.096/5 MHz, 819.2 kHz across all CD settings. The PLL is controlled by the CD[2:0] bits in the Power Control SFR (POWCON, 0xC5). To protect erroneous changes to the Power Control SFR (POWCON, 0xC5), a key is required to modify the register. First the Key SFR (KYREG, 0xC1) is written with the key, 0xA7, and then a new value is written to the Power Control SFR (POWCON, 0xC5).

If the PLL loses lock, the MCU is reset and the PLLFAULT bit is set in the Peripheral Configuration SFR (PERIPH, 0xF4). Set the PLLACK bit in the Start ADC Measurement SFR (ADCGO, 0xD8) to acknowledge the PLL fault, clearing the PLL_FLT flag.

PLL SFR REGISTER LIST

Power Control SFR (POWCON, 0xC5)

Bit Location	Bit Mnemonic	Default Value	Description			
7	RESERVED	X	Reserved			
6	METER_OFF	0	Set this bit to turn off the modulators and energy metering DSP circuitry to reduce power if metering functions are not needed in PSM0			
5	RESERVED	0	Reserved			
4	COREOFF	0	Set this bit to shut down the core if in the PSM1 operating mode.			
3	RESERVED		Reserved			
2-0	CD[2:0]	010	Controls the core clock frequency, F_{core}. F_{core}=4.096MHz/2^{CD}			
			CD[2:0]			F_{core} (MHz)
			0	0	0	4.096
			0	0	1	2.048
			0	1	0	1.024
			0	1	1	0.512
			1	0	0	0.256
			1	0	1	0.128
			1	1	0	0.064
			1	1	1	0.032

Table 109.Key SFR (KYREG, 0xC1)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	KYREG	0	Write 0xA7 to the KYREG SFR before writing the POWCON SFR, to unlock it Write 0xEA to the KYREG SFR before writing to the HTHSEC, SEC, MIN, or HOUR timekeeping register to unlock it.

Peripheral Configuration SFR (PERIPH, 0xF4)

Bit Location	Bit Mnemonic	Default Value	Description
7	RXFLAG	0	If set, indicates that a RX Edge event triggered wakeup from PSM2
6	VSWSOURCE	1	Indicates the power supply that is connected internally to V_{SW}. 0 V_{SW}=V_{BAT} 1 V_{SW}=V_{DD}
5	VDD_OK	0	If set, indicates that VDD power supply is ok for operation

4	PLL_FLT	0	If set, indicates that PLL is not locked	
3	RESERVED			
2	EXTREFEN	0	Set this bit if an external reference is connected to the REFIN pin.	
1-0	RXPROG[1:0]	00	Controls the function of the P1.0/RX pin.	
			RXPROG [1:0]	Function
			0 0	GPIO
			0 1	RX with wakeup disabled
			1 1	RX with wakeup enabled

Start ADC Measurement SFR (ADCGO, 0xD8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0xDF	PLL_FTL_ACK	0	Set this bit to clear the PLL fault bit, PLL_FLT in the PERIPH register. A PLL fault is generated if a reset was caused because the PLL lost lock.
6-3	0xDE – 0xDB	Reserved	0	Reserved
2	0xDA	VDCIN_ADC_GO	0	Set this bit to initiate an external voltage measurement. This bit will be cleared when the measurement request is received by the ADC.
1	0xD9	TEMP_ADC_GO	0	Set this bit to initiate a temperature measurement. This bit will be cleared when the measurement request is received by the ADC.
0	0xD8	BATT_ADC_GO	0	Set this bit to initiate a battery measurement. This bit will be cleared when the measurement request is received by the ADC.

RTC - REAL TIME CLOCK

The ADE75XX/ADE71XX has an embedded Real Time Clock (RTC) – see Figure 75. The external 32.768 kHz crystal is used as the clock source for the RTC. Calibration is provided to compensate the nominal crystal frequency and for variations in the external crystal frequency over temperature. By default, the RTC is maintained active in all the Power Saving Modes. The RTC counters retain their values through watchdog resets and external resets and are only reset during a power on reset.

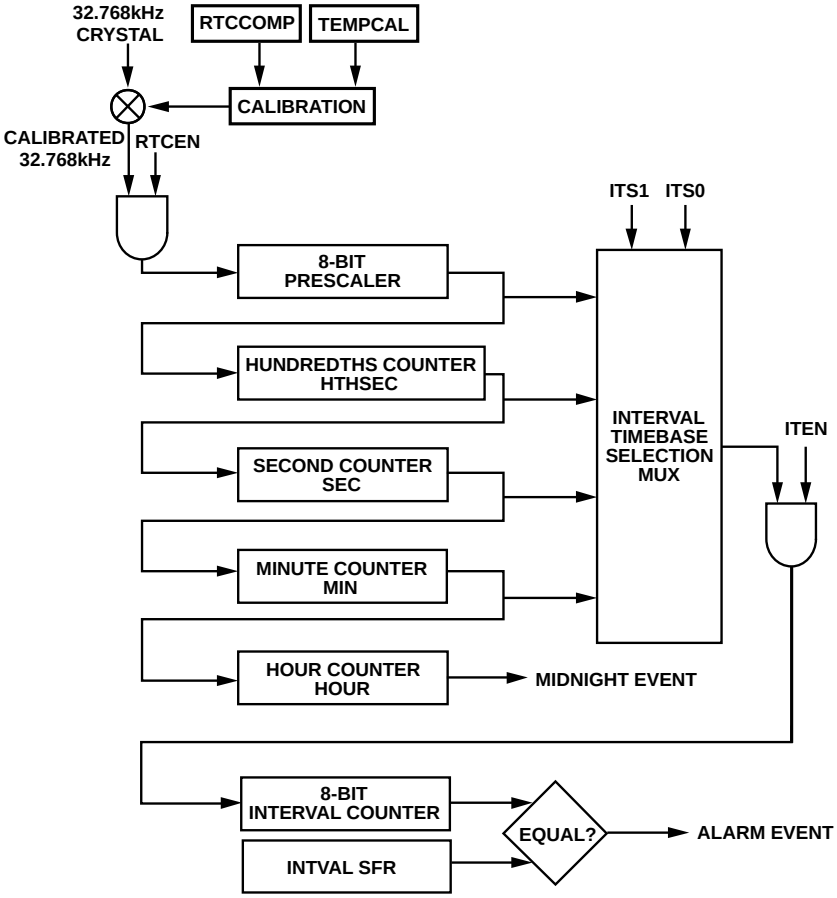


Figure 75: RTC implementation

RTC SFR REGISTER LIST

SFR	Address	Bit Addressable	Description
TIMECON	0xA1	No	RTC configuration
HTHSEC	0xA2	No	Hundredth of a second counter
SEC	0xA3	No	Seconds counter
MIN	0xA4	No	Minutes counter
HOUR	0xA5	No	Hours counter
INTVAL	0xA6	No	Alarm interval
RTCCOMP	0xF6	No	RTC nominal compensation

TEMPCAL	0xF7	No	RTC temperature compensation
INTPR	0xFF	No	RTC Calibration output options
KYREG	0xC1	No	Key Register

Table 110. RTC Configuration SFR (TIMECON, 0xA1)

Bit Location	Bit Mnemonic	Default Value	Description
7	MIDNIGHT	0	Midnight Flag This bit is set when the RTC rolls over to 00:00:00:00. It can be cleared by the user to indicate that the midnight event has been serviced. In twenty-four hour mode, the midnight flag is raised once a day at midnight.
6	TFH	0	Twenty-four hour mode 0 256 Hour mode. The HOUR register will roll over from 255 to 0. 1 24 Hour mode. The HOUR register will roll over from 23 to 0. Note: This bit is retained during a watchdog reset or an external reset. It is reset after a power on reset (POR).
5-4	ITS[1:0]	0	Interval Timer Timebase Selection ITS[1:0] Timebase 0 0 1/128 second 0 1 Second 1 0 Minute 1 1 Hour
3	SIT	0	Interval Timer One-Time Alarm 0 The ALARM flag will be set after INTVAL counts and then another interval count will start. 1 The ALARM flag will be set after one time interval.
2	ALARM	0	Interval Timer Alarm Flag This bit is set when the configured time interval has elapsed. It can be cleared by the user to indicate that the alarm event has been serviced.
1	ITEN	0	Interval Timer Enable 0 The interval timer is disabled. The 8-bit interval timer counter is reset. 1 Set this bit to enable the interval timer. The RTCEN bit must also be set to enable the interval timer.
0	RTCEN	1	RTC Enable. Also Temperature, Battery and Supply ADC Background Strobe Enable Note: The RTC is always enabled.

Table 111. Hundredths of a Second Counter SFR (HTHSEC, 0xA2)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	HTHSEC	0	This counter updates every 1/128 second, referenced from the calibrated 32kHz clock. It overflows from 127 to 00, incrementing the seconds counter, SEC. Note: This register is retained during a watchdog reset or an external reset. It is reset after a power on reset (POR).

Table 112. Seconds Counter SFR (SEC, 0xA3)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SEC	0	This counter updates every second, referenced from the calibrated 32kHz clock. It overflows from 59 to 00, incrementing the minutes counter, MIN.
			Note: This register is retained during a watchdog reset or an external reset. It is reset after a power on reset (POR).

Table 113. Minutes Counter SFR (MIN, 0xA4)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	MIN	0	This counter updates every minute, referenced from the calibrated 32kHz clock. It overflows from 59 to 00, incrementing the hours counter, HOUR.
			Note: This register is retained during a watchdog reset or an external reset. It is reset after a power on reset (POR).

Table 114. Hours Counter SFR (HOUR, 0xA5)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	HOUR	0	This counter updates every hour, referenced from the calibrated 32kHz clock. If the TFH bit in the RTC Configuration SFR (TIMECON, 0xA1) is set, the HOUR SFR overflows from 23 to 00, setting the MIDNIGHT bit and creating a pending RTC interrupt. If the TFH bit in the RTC Configuration SFR (TIMECON, 0xA1) is clear, the HOUR SFR overflows from 255 to 00, setting the MIDNIGHT bit and creating a pending RTC interrupt.
			Note: This register is retained during a watchdog reset or an external reset. It is reset after a power on reset (POR).

Table 115. Alarm Interval SFR (INTVAL, 0xA6)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	INTVAL	0	The interval timer counts according to the timebase established in the ITS[1:0] bits of the RTC Configuration SFR (TIMECON, 0xA1). Once the number of counts is equal to INTVAL, the ALARM flag is set and a pending RTC interrupt is created. Note that the interval counter is 8-bits so it could count up to 255 seconds, for example.

Table 116. RTC Nominal Compensation SFR (RTCCOMP, 0xF6)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	RTCCOMP	0	The RTCCOMP SFR holds the nominal RTC compensation value at 25°C.
			Note: This register is reset after a watchdog reset, an external reset or a power on reset (POR).

Table 117. RTC Temperature Compensation SFR (TEMPCAL, 0xF7)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	TEMPCAL	0	The TEMPCAL SFR is adjusted based on the temerature read in the TEMPADC to calibrate the RTC over temperature. This allows the external crystal shift to be compensated over temperature.

			Note: This register is reset after a watchdog reset, an external reset or a power on reset (POR).

Table 118. Interrupt pins configuration SFR (INTPR, 0xFF)

Bit Location	Bit Mnemonic	Default Value	Description
7	RTCCAL	0	Control RTC calibration output When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.
6-5	FSEL[1:0]		Sets RTC calibration output frequency and calibration window

FSEL[1:0]		Calibration window, frequency
0	0	30.5 seconds, 1Hz
0	1	30.5 seconds, 512 Hz
1	0	0.244 seconds, 500Hz
1	1	0.244 seconds, 16.384 kHz

4	Reserved			
3-1	INT1PRG[2:0]	000	Controls the function of $\overline{INT1}$T	

INT1PRG[2:0]			Function
x	0	0	GPIO
x	0	1	BCTRL
0	1	x	$\overline{INT1}$ input disabled
1	1	x	$\overline{INT1}$ input enabled

0	INT0PRG	0	Controls the function of $\overline{INT0}$

INT0PRG	Function
0	$\overline{INT0}$ input disabled
1	$\overline{INT0}$ input enabled

Table 119. Key SFR (KYREG, 0xC1)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	KYREG	0	Write 0xA7 to the KYREG SFR before writing the POWCON SFR, to unlock it Write 0xEA to the KYREG SFR before writing to the HTHSEC, SEC, MIN, or HOUR timekeeping register to unlock it..

READ AND WRITE OPERATIONS

Writing the RTC Registers

The RTC circuitry runs off a 32.768kHz clock. The timekeeping registers, HTHSEC, SEC, MIN, HOUR are updated with a 32.768 kHz clock. However, the TIMECON and INTVAL SFRs are updated with a 128Hz clock. It takes up to two 128Hz clock cycles from when the MCU writes the TIMECON or INTVAL register until it is successfully updated in the RTC.

To protect the RTC timekeeping registers from runaway code, a key must be written to the KYREG register to obtain write access to the HTHSEC, SEC, MIN and HOUR registers. The KYREG should be set to 0xEA to unlock the timekeeping registers and is reset to zero after a timekeeping register is written to. The RTC registers can be written using the following 8052 assembly code:

```
        MOV     RTCKey, #0EAh
        CALL    UpdateRTC
        …
UpdateRTC:
        MOV     KYREG, RTCKey
        MOV     SEC, #30
        MOV     KYREG, RTCKey
        MOV     MIN, #05
        MOV     KYREG, RTCKey
        MOV     HOUR, #04
        RET
```

Reading the RTC Counter SFRs

The RTC cannot be stopped to read the current time because stopping the RTC would introduce an error in its timekeeping. So the RTC is read on the fly. Therefore the counter registers

must be checked for overflow. This can be accomplished through the following 8052 assembly code:

```
ReadAgain:
        MOV     R0, HTHSEC          ; using Bank 0
        MOV     R1, SEC
        MOV     R2, MIN
        MOV     R3, HOUR
        MOV     A, HTHSEC
        CJNE    A, 00h, ReadAgain   ; 00h is R0 in Bank 0
```

RTC MODES

The RTC can be configured in a 24 hour mode or a 256 hour mode. A midnight event is generated when the RTC hour counter rolls over from 23 to 0 or 255 to 0, depending on whether the TFH bit is set in the RTC Configuration SFR (TIMECON, 0xA1). The midnight event sets the MIDNIGHT flag in the RTC Configuration SFR (TIMECON, 0xA1) and a pending RTC interrupt is created. The RTC midnight event will wake the 8052 MCU core if the MCU is asleep in PSM2 when the midnight event occurs. To acknowledge the midnight event, service the RTC interrupt.

In the 24 hour mode, the midnight event is generated once a day, at midnight. The 24 hour mode is useful for updating a software calendar to keep track of the current day. The 256 hour mode will result in power savings during extended operation in PSM2 because the MCU core will be awoken less frequently.

RTC INTERRUPTS

The RTC Midnight and Alarm Interrupts are enabled by setting the ETI bit in the Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9). When a midnight or alarm event occurs, a pending RTC interrupt is generated. If the RTC interrupt is enabled, the program will vector to the RTC interrupt address and the pending interrupt will be cleared. If the RTC interrupt is disabled, then the RTC interrupt will remain pending until the RTC interrupt is enabled. Then the program will vector to the RTC interrupt address.

The MIDNIGHT and ALARM flags are set when the midnight and alarm events occur, respectively. The user should manage these flags to keep track of which event caused an RTC interrupt by servicing the event and clearing the appropriate flag in the RTC ISR.

Note that if the ADE7100/7500 is awakened by an RTC event, either the MIDNIGHT or ALARM, then the pending RTC interrupt must be serviced before the ADE7100/7500 can go back to sleep again. The ADE7100/7500 will keep waking up until this interrupt has been serviced.

Interval Timer Alarm

The RTC can be used as an interval timer. When the interval timer is enabled by setting the ITEN bit in the RTC Configuration SFR (TIMECON, 0xA1), the interval timer clock source selected by the ITS1 and ITS0 bits is passed through to an 8-bit counter. This counter increments on every interval timer clock pulse until the 8-bit counter is equal to the value in the Alarm Interval SFR (INTVAL, 0xA6). Then an alarm event is generated, setting the ALARM flag and creating a pending RTC interrupt. If the SIT bit in the RTC Configuration SFR (TIMECON, 0xA1) is clear then the 8-bit counter is cleared and starts counting again. If the SIT bit is set then the 8-bit counter is held in reset after the alarm occurs.

Take care when changing the interval timer timebase. The recommended prodedure is as follows:

1. If the INTVAL SFR is going to be modified, write this register first. Then wait for one 128Hz clock cycle, to synchronize with the RTC, 64000 cycles at a 4.096MHz instruction cycle clock.
2. Disable the interval timer by clearing the ITEN bit in the TIMECON SFR. Then wait for one 128Hz clock cycle, to synchronize with the RTC, 64000 cycles at a 4.096MHz instruction cycle clock.
3. Read the TIMECON SFR to ensure that the ITEN bit is clear. If it is not, wait for another 128Hz clock cycle.
4. Set the timebase bits, ITS[1:0] in the TIMECON SFR to configure the interval. Wait for a 128Hz clock cycle for this change to take effect.

The RTC alarm event will wake the 8052 MCU core if the MCU is in PSM2 when the alarm event occurs.

RTC CALIBRATION

The RTC provides registers to calibrate the nominal external crystal frequency and its variation over temperature. Up to ±248ppm frequency error can be calibrated out by the RTC circuitry, which adds or subtracts pulses from the external crystal signal.

The nominal crystal frequency should be calibrated with the RTCCOMP register so that the clock going into the RTC is precisely 32.768 kHz at 25°C. The RTC Temperature Compensation SFR (TEMPCAL, 0xF7) is used to compensate for the external crystal drift over temperature by adding or subtracting additional pulses based on temperature.

The LSB of each RTC compensation register represents a ±2ppm, or 0.17s/day, frequency error. The RTC compensation circuitry adds the RTC Temperature Compensation SFR (TEMPCAL, 0xF7) and the RTC Nominal Compensation SFR (RTCCOMP, 0xF6) to determine how much compensation is required and the sum of these two registers is limited to ±248ppm, or 42.85s/day.

Calibration Flow:

A RTC calibration pulse output is provided on the P0.2/CF1/RTCCAL pin. Enable the RTC output by setting the RTCCAL bit in the INTPR SFR.

The RTC calibration is accurate to within ±2ppm over a 30.5 second window in all operational modes: PSM0, PSM1 and PSM2. Two output frequencies are offered for the normal RTC mode: 1Hz with FSEL[1:0]=00 and 512Hz with FSEL[1:0]=01 in the INTPR register.

A shorter window of 0.244 seconds is offered for fast calibration during PSM0 or PSM1. Two output frequencies are offered for this RTC calibration output mode: 500Hz with FSEL[1:0]=01 and 16.384kHz with FSEL[1:0]=11 in the INTPR register. Note that for the 0.244s calibration window, the RTC is clocked 125 times faster than in the normal mode, resulting in timekeeping registers that represent seconds/125, minutes/125 and hours/125 instead of seconds, minutes and hours. Therefore this mode should be used for calibration only.

Option	FSEL[1:0]	Calibration Window (s)	F_{RTCCAL} (Hz)
Normal Mode 0	00	30.5	1
Normal Mode 1	01	30.5	512
Calibration Mode 0	10	0.244	500
Calibration Mode 1	11	0.244	16384

Table 120: RTC calibration options

When no RTC compensation is applied, when RTCCOMP and TEMPCAL equal to zero, the nominal compensation required to account for the error in the external crystal can be determined. In this case, it is not necessary to wait for an entire calibration window to determine the error in the pulse output. Calculating at the error in frequency between two consecutive pulses on the P0.2/CF1/RTCCAL pin is enough.

The value to write to the RTCCOMP register is calculated from the % error or seconds per day error on the frequency output. Each LSB of the RTCCOMP SFR represents 2ppm of correction where1s/day error is equal to 11.57ppm.

$$RTCCOMP = 5000 \times (\%\ Error)$$

$$RTCCOMP = \frac{1}{2 \times 11.57} \times (s / day\ Error)$$

to determine how much compensation is required and the sum of these two registers is limited to ±248ppm.

During calibration, user software writes the RTC with the current time. Refer to the RTC Read and Write operations section for more information on how to read and write the RTC timekeeping registers.

UART SERIAL INTERFACE

The ADE75XX/ADE71XX UART can be configured in one of four modes:

- Shift register with baud rate fixed at $F_{core}/12$

- 8-bit UART with variable baud rate

- 9- bit UART with baud rate fixed at $F_{core}/64$ or $F_{core}/32$

- 9 bit UART with variable baud rate

Variable baud rates are defined by using an internal timer to generate any rate between 300 and 115200 bauds/s.

The UART serial interface provided in the ADE75XX/ADE71XX is a full-duplex serial interface. It is also receive buffered, by storing the first received byte in a receive buffer until the reception of the second byte is complete. The physical interface to the UART is provided via the RxD (P1.0) and TxD (P1.1) pins, while the firmware interface is through the SFRs presented in Table 121.

Both the serial port receive and transmit registers are accessed through the SBUF SFR (SFR address = 0x99). Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

An enhanced UART mode is offered by using UART Timer and providing enhanced frame error, break error and overwrite error detection. This mode is enabled by setting the EXTEN bit in the CFG SFR—see the UART additional features section. The SBAUDT and SBAUDF SFR are used to configure UART Timer and to indicate the enhanced UART errors.

UART SFR REGISTER LIST

Table 121. Serial port SFRs

SFR	Address	Bit Addressable	Description
SCON	0x98	Yes	Serial Communications Control register – see Table 122
SBUF	0x99	No	Serial Port Buffer – see Table 123
SBAUDT	0x9E	No	**Enhanced error checking** – see Table 124
SBAUDF	0x9D	No	**Enhanced Fractional Divider** – see Table 125

Table 122. SCON SFR Bit Description SFR (SCON, 0x98)

Bit Location	Bit Addr.	Bit Name	Default Value	Description		
7-6	0x9F, 0x9E	SM0, SM1	00	UART Serial Mode Select Bits. These bits select the serial port operating mode as follows:		
				SM0	SM1	Selected Operating Mode.
				0	0	Mode 0: Shift register, fixed baud rate ($F_{core}/12$).
				0	1	Mode 1: 8-bit UART, variable baud rate.
				1	0	Mode 2: 9-bit UART, fixed baud rate ($F_{core}/32$) or ($F_{core}/16$).
				1	1	Mode 3: 9-bit UART, variable baud rate.
5	0x9D	SM2	0	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Modes 2 and 3 and framing error detection in Mode 1. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit was not received. If SM2 is		

				cleared, RI is set as soon as the byte of data is received. In Modes 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.
4	0x9C	REN	0	Serial Port Receive Enable Bit. Set by user software to enable serial port reception. Cleared by user software to disable serial port reception.
3	0x9B	TB8	0	Serial Port Transmit (Bit 9). The data loaded into TB8 is the ninth data bit transmitted in Modes 2 and 3.
2	0x9A	RB8	0	Serial Port Receiver Bit 9. The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	0x99	TI	0	Serial Port Transmit Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	0x98	RI	0	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by user software.

Table 123. Serial port Buffer SFR (SBUF, 0x99)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SBUF	0	Serial port data buffer

Table 124. Enhanced Serial baud rate control SFR (SBAUDT, 0x9E)

Bit Location	Bit Mnemonic	Default Value	Description			
7	OWE	0	Overwrite Error. This bit is set when new data is received and RI=1. It indicates that SBUF was not read before the next character was transferred in, causing the prior SBUF data to be lost. Write a zero to this bit to clear it..			
6	FE	0	Frame Error. This bit is set when the received frame did not have a valid stop bit. This bit is read only and updated every time a frame is received.			
5	BE	0	Break Error. This bit is set whenever the receive data line (Rx) is low for longer than a full transmission frame, the time required for a start bit, 8 data bits, a parity bit and half a stop bit. This bit is updated every time a frame is received.			
4-3	SBTH1, SBTH0	0	Extended divider ratio for baud rate setting as shown in Table 126			
2, 1, 0	DIV2, DIV1, DIV0	0	Binary Divider			
			DIV2	DIV1	DIV0	
			0	0	0	Divide by 1. See Table 126.
			0	0	1	Divide by 2. See Table 126.
			0	1	0	Divide by 4. See Table 126.
			0	1	1	Divide by 8. See Table 126.
			1	0	0	Divide by 16. See Table 126.
			1	0	1	Divide by 32. See Table 126.
			1	1	0	Divide by 64. See Table 126.

			1	1	1	Divide by 128. See Table 126.

Table 125. UART Timer Fractional Divider SFR (SBAUDF, 0x9D)

Bit Location	Bit Mnemonic	Default value	Description
7	UARTBAUDEN	0	UART Baud Rate Enable Set to enable UART Timer to generate the baud rate. When set, PCON.7, T2CON.4, and T2CON.5 are ignored. Cleared to let the baud rate be generated as per a standard 8052.
6	----		Not Implemented. Write Don't Care.
5	SBAUDF.5	0	UART Timer Fractional Divider Bit 5.
4	SBAUDF.4	0	UART Timer Fractional Divider Bit 4.
3	SBAUDF.3	0	UART Timer Fractional Divider Bit 3.
2	SBAUDF.2	0	UART Timer Fractional Divider Bit 2.
1	SBAUDF.1	0	UART Timer Fractional Divider Bit 1.
0	SBAUDF.0	0	UART Timer Fractional Divider Bit 0.

Table 126. Common Baud Rates Using UART Timer with a 4.096 MHz FLL Clock

Ideal Baud	CD	SBTH	DIV	SBAUDT	SBAUDF	% Error
115200	0	0	1	01H	87H	+ 0.16
115200	1	0	0	00H	87H	+ 0.16
57600	0	0	2	02H	87H	+ 0.16
57600	1	0	1	01H	87H	+ 0.16
38400	0	0	2	02H	ABH	- 0.31
38400	1	0	1	01H	ABH	- 0.31
38400	2	0	0	00H	ABH	- 0.31
19200	0	0	3	03H	ABH	- 0.31
19200	1	0	2	02H	ABH	- 0.31
19200	2	0	1	01H	ABH	- 0.31
19200	3	0	0	00H	ABH	- 0.31
9600	0	0	4	04H	ABH	- 0.31
9600	1	0	3	03H	ABH	- 0.31
9600	2	0	2	02H	ABH	- 0.31
9600	3	0	1	01H	ABH	- 0.31
9600	4	0	0	00H	ABH	- 0.31
4800	0	0	5	05H	ABH	- 0.31
4800	1	0	4	04H	ABH	- 0.31
4800	2	0	3	03H	ABH	- 0.31
4800	3	0	2	02H	ABH	- 0.31
4800	4	0	1	01H	ABH	- 0.31
4800	5	0	0	00H	ABH	- 0.31
2400	0	0	6	06H	ABH	- 0.31
2400	1	0	5	05H	ABH	- 0.31
2400	2	0	4	04H	ABH	- 0.31
2400	3	0	3	03H	ABH	- 0.31
2400	4	0	2	02H	ABH	- 0.31
2400	5	0	1	01H	ABH	- 0.31

2400	6	0	0	00H	ABH	- 0.31
300	0	2	7	17H	ABH	- 0.31
300	1	1	7	0FH	ABH	- 0.31
300	2	0	7	07H	ABH	- 0.31
300	3	0	6	06H	ABH	- 0.31
300	4	0	5	05H	ABH	- 0.31
300	5	0	4	04H	ABH	- 0.31
300	6	0	3	03H	ABH	- 0.31
300	7	0	2	02H	ABH	- 0.31

UART OPERATION MODES

Mode 0 (Shift Register with baud rate fixed at Fcore /12)

Mode 0 is selected when the SM0 and SM1 bits in the SCON SFR are clear. In this shift register mode, serial data enters and exits through RxD. TxD outputs the shift clock. The baud rate is fixed at $F_{core}/12$. Eight data bits are transmitted or received.

Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line as shown in Figure 76.

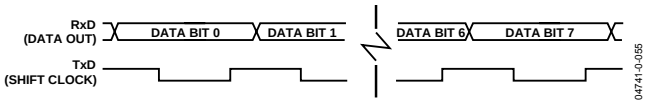


Figure 76. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, each frame consists of 10 bits transmitted on TxD or received on RxD.

The baud rate is set by a timer overflow rate. Timer 1 or Timer 2 can be used to generate baud rates or both timers can be used simultaneously where one generates the transmit rate and the other generates the receive rate. There is also a dedicated timer for baud rate generation, UART Timer, which has a fractional divisor to precisely generate any baud rate—see the UART Timer Generated Baud Rates section.

Transmission is initiated by a write to SBUF. Next a stop bit (a 1) is loaded into the 9th bit position of the transmit shift register. The data is output bit-by-bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 77.

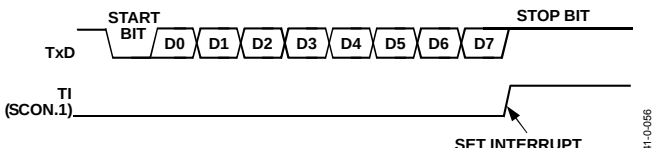


Figure 77. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The 8 data bits are clocked into the serial port shift register.

All of the following conditions must be met at the time the final shift pulse is generated to receive a character:

- If the extended UART is disabled (EXTEN=0 in the CFG SFR), RI must be zero to receive a character. This ensures that the data in SBUF will not be overwritten if the last received character has not been read.
- If frame error checking is enabled by setting SM2, the received stop bit must be set to receive a character. This ensures that every character received comes from a valid frame, with both a start and a stop bit)

If any of these conditions are *not* met, the received frame is irretrievably lost, and the receive interrupt flag, RI, is not set.

If the received frame has met the above criteria, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th bit (stop bit) is clocked into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

Mode 2 (9- bit UART with baud fixed at $F_{core}/64$ or $F_{core}/32$)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at $F_{core}/64$ by default, although by setting the SMOD bit in PCON, the frequency can be doubled to $F_{core}/32$. Eleven bits are transmitted or received: a start bit (0), 8 data bits, a programmable 9th bit, and a stop bit (1). The 9th bit is most often used as a parity bit or as part of a multiprocessor communication protocol, although it can be used for anything, including a ninth data bit if required.

To use the 9th data bit as part of a communication protocol for a multiprocessor network such as RS-485, the 9th bit is set to indicate that the frame contains the address of the device that the master would like to communicate with. The devices on the network are always listening for a packet with the 9th bit set and are configured such that if the 9th bit is clear, the frame will not be valid and a receive interrupt will not be generated. If the 9th bit is set, all of the devices on the network will receive the address and get a receive character interrupt. The devices will examine the address and if it matches a device's preprogrammed address, the device will configure itself to listen to all incoming frames, even those with the 9th bit clear. Since the master has initiated communication with that device, all the following packets with the 9th bit clear are intended specifically for the addressed device until another packet with the 9th bit set is received. If the address does not match, the device will continue listening for address packets.

To transmit, the 8 data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the 8 data bits from SBUF are loaded into the transmit shift register (LSB first). The 9th data bit, held in TB8, is loaded into the 9th bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The transmit interrupt flag, TI, is set as soon as the transmission has completed, when the stop bit appears on TxD.

All of the following conditions must be met at the time the final shift pulse is generated to receive a character:

- If the extended UART is disabled (EXTEN=0 in the CFG SFR), RI must be zero to receive a character. This ensures that the data in SBUF will not be overwritten if the last received character has not been read.
- If multiprocessor communication is enabled by setting SM2, the received 9th bit must be set to receive a character. This ensures that only frames with the 9th bit set, frames that contain addresses, generate a receive interrupt.

If any of these conditions are *not* met, the received frame is irretrievably lost, and the receive interrupt flag, RI, is not set.

Reception for Mode 2 is similar to that of Mode 1. The 8 data bytes are input at RxD (LSB first) and loaded onto the receive shift register. If the received frame has met the above criteria, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th data bit is latched into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate. The baud rate is set by a timer overflow rate. Timer 1 or Timer 2 can be used to generate baud rates or both timers can be used simultaneously where one generates the transmit rate and the other generates the receive rate. There is also a dedicated timer for baud rate generation, UART Timer, which has a fractional divisor to precisely generate any baud rate—see the UART Timer Generated Baud Rates section. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART BAUD RATE GENERATION

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{F_{core}}{12} \right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times F_{core}$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate of the timer generating the baud rate: either Timer 1 or Timer 2 or the dedicated baud rate generator, UART Timer, which has an integer and fractional divisor.

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{F_{core}}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2

has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$\textit{Modes 1 and 3 Baud Rate} = \frac{1}{16} \times \textit{Timer 2 Overflow Rate}$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 78.

In this case, the baud rate is given by the formula

$$\textit{Modes 1 and 3 Baud Rate} = \frac{F_{core}}{(16 \times [65536 - (RCAP2H : RCAP2L)])}$$

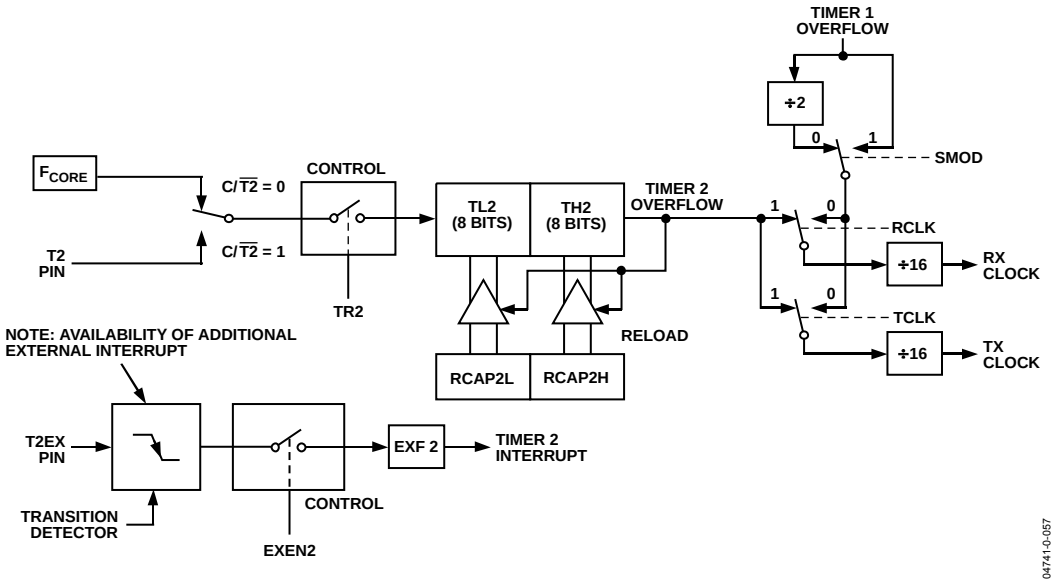


Figure 78. Timer 2, UART Baud Rates

UART Timer Generated Baud Rates

The high integer dividers in a UART block mean that high speed baud rates are not always possible. Also, generating baud rates requires the exclusive use of a timer, rendering it unusable for other applications when the UART is required. To address this problem, the ADE75XX/ADE71XX has a dedicated baud rate timer (UART Timer) specifically for generating highly accurate baud rates. UART Timer can be used instead of Timer 1 or Timer 2 for generating very accurate high speed UART baud rates including 115200. UART Timer also allows a much wider range of baud rates to be obtained. In fact, every desired bit rate from 12 bps to 393216 bps can be generated to within an error of ±0.8%. UART Timer also frees up the other three timers, allowing them to be used for different applications. A block diagram of UART Timer is shown in Figure 79.

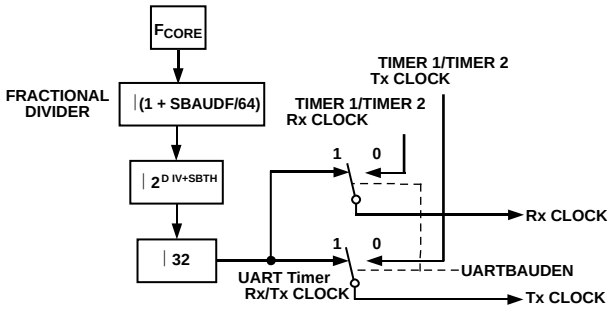


Figure 79. UART Timer, UART Baud Rate

Two SFRs Enhanced Serial baud rate control SFR (SBAUDT, 0x9E) and UART Timer Fractional Divider SFR (SBAUDF, 0x9D) are used to control UART Timer. SBAUDT is the baud rate control SFR; it sets up the integer divider (DIV) and the extended divider (SBTH) for UART Timer.

The appropriate value to write to the DIV[2:0] and SBTH[1:0] bits can be calculated using the following formula where F_{core} is defined in POWCON SFR. Note that the DIV value must be rounded down to the nearest integer.

$$DIV + SBTH = \frac{\log\left(\frac{F_{core}}{16 \times Baud\ Rate}\right)}{\log(2)}$$

SBAUDF is the fractional divider ratio required to achieve the required baud rate. The appropriate value for SBAUDF can be calculated with the following formula:

$$SBAUDF = 64 * \left(\frac{F_{core}}{16 \cdot 2^{DIV+SBTH} \times Baud\ Rate} - 1\right)$$

Note that SBAUDF should be rounded to the nearest integer. Once the values for DIV and SBAUDF are calculated, the actual baud rate can be calculated with the following formula:

$$Actual\ Baud\ Rate = \frac{F_{core}}{16 \cdot 2^{DIV+SBTH} \cdot \left(1 + \frac{SBAUDF}{64}\right)}$$

For example, to get a baud rate of 9600 while operating at a core clock frequency of 4.096 MHz, with the PLL CD bits equal to zero,

$DIV + SBTH = \log(4096000/(16 \times 9600))/\log 2 = 4.74 = 4$

Note that the DIV result is rounded down.

$SBAUDF = 64*(4096000/(16*2^3*9600)-1) = 42.67 = 2BH$

Therefore, the actual baud rate is 9570 bps, which gives an error of 0.31%.

UART ADDITIONAL FEATURES

Enhanced Error Checking

The extended UART provides frame error, break error and overwrite error detection. Framing errors occur when a stop bit is not present at the end of the frame. A missing stop bit implies that the data in the frame may not have been received properly. Break error detection indicates if the Rx line has been low for longer than a 9-bit frame. It indicates that the data just received, a zero, or NUL character, is not valid because the master has disconnected. Overwrite error detection indicates if the received data isn't read fast enough and as result, a byte of data has been lost.

The 8052 standard UART offers frame error checking for an 8-bit UART through the SM2 and RB8 bits. Setting the SM2 bit prevent frames without a stop bit from being received. The stop bit is latched into the RB8 bit in the SCON register. This bit can be examined to determine if a valid frame was received. The 8052 does not however, provide frame error checking for a 9-bit UART. This enhanced error checking functionality is available through the frame error bit, FE in the SBAUDT SFR. The FE bit will be set on framing errors for both 8-bit and 9-bit UARTs.

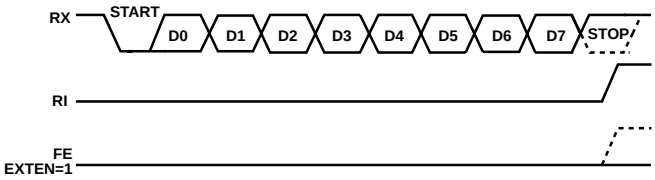


Figure 80: UART Timing in Mode 1

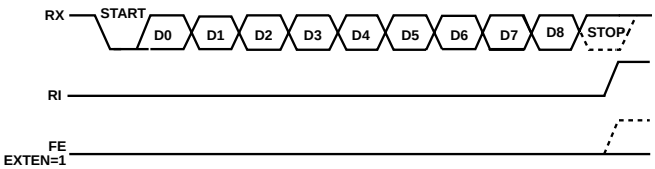


Figure 81: UART Timing in Modes 2 and 3

The 8052 standard UART does not provide break error detection. However for an 8-bit UART, it can be determined that a break error occurred if the received character is zero, a NUL character, and there was no stop bit because the RB8 bit is low. Break error detection is not possible for a 9-bit 8052 UART because the stop bit is not recorded. The ADE75XX/ADE71XX enhanced break error detection is available through the BE bit in the SBAUDT SFR.

The 8052 standard UART prevents overwrite errors by not allowing a character to be received if the RI, receive interrupt flag, is set. However, it does not indicate if a character has been lost because the RI bit was set when the frame was received. The enhanced UART overwrite error detection provides this information. When the enhanced 8052 UART is enabled, a frame will be received regardless of the state of the RI flag. If RI=1 when a new byte is received, the byte in SCON is overwritten, and the overwrite error flag will be set. The overwrite error flag will be cleared when SBUF is read.

The extended UART is enabled by setting the EXTEN bit in the CFG SFR.

UART TxD signal modulation

There is an internal 38 kHz signal which can be ORed with the UART transmit signal for use in remote control applications—see the 38 kHz Modulation section.

One of the events that can wake the MCU from sleep mode is activity on the UART RX pin—see the 3.3V Peripherals and Wakeup Events section.

SERIAL PERIPHERAL INTERFACE INTERFACE (SPI)

The ADE75XX/ADE71XX integrates a complete hardware serial peripheral interface on-chip. The SPI interface is full duplex so that eight bits of data are synchronously transmitted and received simultaneously. This SPI implementation is double buffered. This allows the user to read the last byte of received data while a new byte is shifted in. The next byte to be transmitted can be loaded while the current byte is shifted out.

The SPI port can be configured for Master or Slave operation. The physical interface to the SPI is done via MISO (P0.3), MOSI (P0.2), SCLK (P0.4) and $\overline{SS}$ (P0.5) pins, while the firmware interface is done via the SPI Configuration Register SFR (SPIMOD1, 0xE8), SPI Configuration Register SFR (SPIMOD2, 0xE9), SPI Interrupt Status Register SFR (SPISTAT, 0xEA), SPI/I2C Transmit Buffer SFR (SPI2CTx, 0x9A) and SPI Receive Buffer SFR (SPI2CRx, 0x9B).

Note that the SPI pins are shared with the I^2C pins. Therefore, the user can enable only one interface at a time. The SCPS bit in the CFG SFR selects which peripheral is active.

SPI SFR REGISTER LIST

SFR Address	Name	R/W	Length	Default Value	Description
0x9A	SPI2CTx	W	8		SPI Data out register
0x9B	SPI2CRx	R	8	0	SPI Data in register
0xE8	SPIMOD1	R/W	8	0x10	SPI configuration register
0xE9	SPIMOD2	R/W	8	0	SPI configuration register
0xEA	SPISTAT	R/W	8	0	SPI Interrupt Status register

Table 127: SPI SFR register list

Table 128. SPI/I2C Transmit Buffer SFR (SPI2CTx, 0x9A)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SPI2CTx	0	SPI or I2C transmit buffer When SPI2CTx SFR is written, its content is transfered to the transmit FIFO input. When a write is requested, the FIFO output is sent on the SPI or I2C bus.

Table 129. SPI Receive Buffer SFR (SPI2CRx, 0x9B)

Bit Location	Bit Mnemonic	Default Value	Description
7-0	SPI2CRx	0	SPI or I2C receive buffer When SPI2CRx SFR is read, one byte from the Receive FIFO output is transfered to SPI2CRx SFR. A new data from the SPI or I2C bus is written to the FIFO input.

Table 130. SPI Configuration Register SFR (SPIMOD1, 0xE8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description	
7-5	0xEF – 0xEE	Reserved	0	Reserved	
5	0xED	INTMOD	0	SPI Interrupt mode 0: SPI Interrupt set when SPI Rx buffer full 1: SPI interrupt set when SPI Tx buffer empty	
4	0xEC	AUTO_SS	1	Master Mode: $\overline{SS}$ output control. See Figure 82.	
				0	The $\overline{SS}$ is held low while this bit is clear. This allows manual chip select control using the $\overline{SS}$ pin.
				1	Single Byte Read or Write: The $\overline{SS}$ will go low during a single byte transmission and then return high.
					Continuous Transfer: The $\overline{SS}$ will go low during the duration of the multi-byte continuous transfer and then return high.
3	0xEB	SSE	0	Slave Mode: $\overline{SS}$ input enable	

				When this bit is set to logic one, the $\overline{SS}$ pin is defined as the Slave Select input pin for the SPI slave interface	
2	0xEA	RxOFW	0	Receive buffer overflow write enable	
				0	If the SPI2CRX SFR has not been read when a new data byte is received, the new byte will be discarded.
				1	If the SPI2CRX SFR has not been read when a new data byte is received, the new byte will overwrite the old data.
1-0	0xE9 – 0xE8	SPIR[1:0]	0	Master Mode: SPI SCLK frequency [1:0] 00 F_{core} / 8 = 512kHz if F_{core} = 4.096MHz 01 F_{core} / 16 = 256kHz if F_{core} = 4.096MHz 10 F_{core} / 32 = 128kHz if F_{core} = 4.096MHz 11 F_{core} / 64 = 64kHz if F_{core} = 4.096MHz	

Table 131. SPI Configuration Register SFR (SPIMOD2, 0xE9)

Bit Location	Bit Mnemonic	Default Value	Description	
7	SPICONT	0	SPI continuous transfer mode enable bit	
			0	The SPI interface will stop after one byte is transferred and $\overline{SS}$ will be deasserted. A new data transfer can be intiated after a stalled period.
			1	The SPI interface will continue transferring data until no valid data is availbale in the SPI2CTx SFR. $\overline{SS}$ will remain asserted until SPI2CTx SFR and the transmit shift register is empty.
6	SPIEN	0	SPI interface enable bit	
			0	The SPI interface is disabled.
			1	The SPI interface is enabled
5	SPIODO	0	SPI Open Drain Outputs configuration bit	
			0	Internal pull-up resistors are connected to the SPI outputs
			1	The SPI outputs are open-drain and need external pull-up resistors
4	SPIMS_b	0	SPI Master Mode enable bit	
			0	The SPI interface is defined as a Slave
			1	The SPI interface is defined as a Master
3	SPICPOL	0	SPI clock polarity configuration bit – see Figure 84.	
			0	The default state of SCLK is low and the first SCLK edge is rising. Depending on SPICPHA bit, the SPI data output changes state on the falling or rising edge of SCLK while the SPI data input is sampled on the rising or falling edge of SCLK.
			1	The default state of SCLK is high and the first SCLK edge is falling. Depending on SPICPHA bit, the SPI data output changes state on the rising or falling edge of SCLK while the SPI data input is sampled on the falling or rising edge of SCLK.
2	SPICPHA	0	SPI clock phase configuration bit – see Figure 84.	
			0	The SPI data output changes state when $\overline{SS}$ goes low, at the second edge of SCLK and then every two subsequent edges while the SPI data input is sampled at the first SCLK edge and then every two subsequent edges.
			1	The SPI data output changes state at the first edge of SCLK and then every two subsequent edges while the SPI data input is sampled at the second SCLK edge and then every two subsequent edges.
1	SPILSBF	0	Master Mode: LSB first configuration bit	

			0	The MSB of the SPI outputs is transmitted first
			1	The LSB of the SPI outputs is transmitted first
0	Reserved	1	This bit must be kept as 1.	

Table 132. SPI Interrupt Status Register SFR (SPISTAT, 0xEA)

Bit Location	Interrupt Flag	Default Value	Description	
7	BUSY	0	SPI Peripheral Busy Flag	
			0	The SPI peripheral is idle
			1	The SPI peripheral is busy transferring data in slave or master mode.
6	MMERR	0	SPI Multi-Master Error Flag	
			0	A multiple master error has not occurred.
			1	If the SS_EN bit is set, enabling the Slave Select input and the $\overline{SS}$ is asserted while the SPI peripheral is transferring data as a master, then this flag is raised to indicate the error. Write a zero to this bit to clear it..
5	SPIRxOF	0	SPI Receive Overflow Error Flag. Reading the SPI2CRx SFR will clear this bit.	
			SPIRxOF	
			0	The SPI2CRX register contains valid data
			1	This bit is set if the SPI2CRX register is not read before the end of the next byte transfer. If the RxOF_EN bit is set and this condition occurs, SPI2CRX will be overwritten.
4	Reserved		Reserved	
3	SPIRxBF	0	Status bit for SPI Rx buffer. When set the Rx FIFO is full. Reading the SPI2CRx SFR will clear this bit.	
2	SPITxUF	0	Status bit for SPI Tx buffer. When set the Tx FIFO is underflowing and data can be write into SPI2CTx. Write a zero to this bit to clear it.	
1	SPITxIRQ	0	SPI Transmit Interrupt Flag.	
			SPITxIRQ	
			0	The SPI2CTX register is full.
			1	This bit is set when the SPI2CTX register is empty. If the SPI/I2C interrupt is enabled, an interrupt will be generated when this bit is set. If new data isn't written into the SPI2CTX SFR before the end of the current byte transfer, the transfer will stop and the $\overline{SS}$ will be deasserted. Write a zero to this bit to clear it..
0	SPITxBF	0	Status bit for SPI Tx buffer. When set, the SPI Tx buffer is full. Write a zero to this bit to clear it..	

SPI PINS

MISO (Master In, Slave Out Data I/O Pin)

The MISO pin is configured as an input line in master mode and as an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out).The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI pin is configured as an output line in master mode and as an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in).The data is transferred as byte-wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O Pin)

The master serial clock (SCLK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the bit rate, polarity, and phase of the clock are controlled by the SPI Configuration Register SFR (SPIMOD1, 0xE8) and SPI Configuration Register SFR (SPIMOD2, 0xE9).

In slave mode, the SPI Configuration Register SFR (SPIMOD2, 0xE9) must be configured with the phase and polarity of the expected input clock.

In both master and slave modes, the data is transmitted on one edge of the SCLK signal and sampled on the other. It is

important, therefore, that CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Pin)

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$ low. The SPI port will then transmit and receive 8-bit data until the data is concluded by deassertion of $\overline{SS}$. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, the $\overline{SS}$ can be used to control data transfer to a slave device. In the automatic slave select control mode, the $\overline{SS}$ is asserted low to select the slave device and then raised to deselect the slave device after the transfer is complete. Automatic slave select control is enabled by setting the AUTO_SS bit in the SPI Configuration Register SFR (SPIMOD1, 0xE8).

In a multi-master system, the $\overline{SS}$ can be configured as an input so that the SPI peripheral can operate as a slave in some situations and as a master in other situations. In this case, the slave selects for the slaves controlled by this SPI peripheral should be generated with general I/O pins.

SPI MASTER OPERATING MODES

The double buffered receive and transmit registers can be used to maximize the throughput of the SPI peripheral by continuously streaming out data in master mode. The continuous transmit mode is designed to use the full capacity of the SPI. In this mode, the master will transmit and receive data until the SPI/I2C Transmit Buffer SFR (SPI2CTx, 0x9A) register is empty at the start of a byte transfer. Continuous mode is enabled by setting the SPICONT bit in the SPI Configuration Register SFR (SPIMOD2, 0xE9).The SPI peripheral also offers a single byte read and a single byte write function.

In master mode, the type of transfer is handled automatically depending on the configuration of bits 0 and 7 of the SPI Configuration Register SFR (SPIMOD2, 0xE9). Table 133 shows the sequence of events that should be performed for each master operating mode. Based on the $\overline{SS}$ configuration, some of these events will take place automatically.

Table 133. Procedures for using SPI as a Master

Mode	SPIMOD[7] = SPICONT bit	Description of operation
Single Byte Write	0	Step 1: Write to SPI2CTx SFR
		Step 2: $\overline{SS}$ is asserted low and write routine is initiated
		Step 3: SPITxIRQ Interrupt Flag is set when SPI2CTx register is empty
		Step 4: $\overline{SS}$ is deasserted high
		Step 5: Write to SPI2CTx SFR to clear SPI2CTxIRQ Interrupt flag
Continuous	1	Step 1: Write to SPI2CTx SFR
		Step 2: $\overline{SS}$ is asserted low and write routine is initiated
		Step 3: Wait for SPI2CTxIRQ Interrupt flag to write to SPI2CTx SFR. Transfer will continue until the SPI2CTX register and transmit shift registers are empty.
		Step 4: SPITxIRQ Interrupt Flag is set when SPI2CTx register is empty
		Step 5: $\overline{SS}$ is deasserted high
		Step 6: Write to SPI2CTx SFR to clear SPITxIRQ Interrupt flag

Figure 82 shows the SPI output for certain automatic chip select and continuous mode selections. Note that if the continuous mode is not used, a short delay is inserted between transfers.

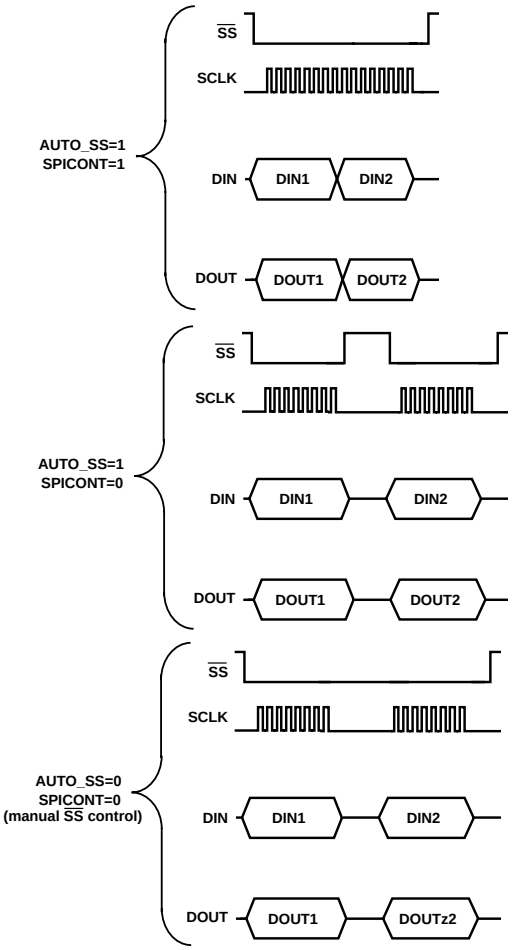


Figure 82: Automatic Chip Select and Continuous Mode Output

SPI INTERRUPT AND STATUS FLAGS

The SPI interface has several status flags that indicate the status of the double buffered receive and transmit registers. Figure 83 shows when the status and interrupt flags are raised. The transmit interrupt occurs when the transmit shift register is loaded with the data in the SPI/I2C Transmit Buffer SFR (SPI2CTx, 0x9A) register. If the SPI/I2C Transmit Buffer SFR (SPI2CTx, 0x9A) register has not been written with new data by the beginning of the next byte transfer, the transmit operation stops.

When a new byte of data is received in the SPI Receive Buffer SFR (SPI2CRx, 0x9B) register, the SPI receive interrupt flag is raised. If the data in the SPI Receive Buffer SFR (SPI2CRx, 0x9B) register is not read before new data is ready to be loaded into the SPI Receive Buffer SFR (SPI2CRx, 0x9B), an overflow condition has occurred. This overflow condition, indicated by the SPIRxOF flag, will force the new data to be discarded or overwritten if the RxOF_EN bit is set.

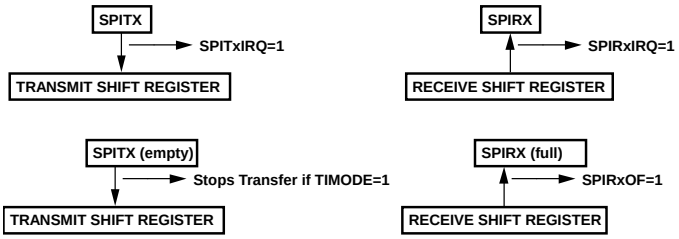


Figure 83: SPI Receive and Transmit Interrupt and Status Flags

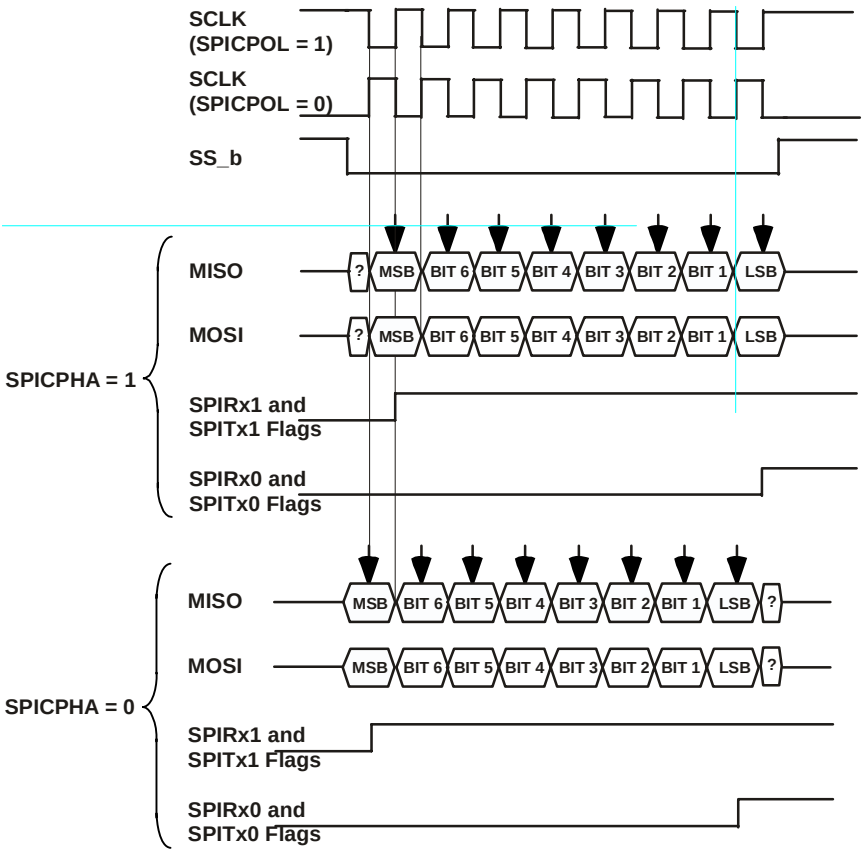


Figure 84. SPI timing configurations

I²C COMPATIBLE INTERFACE

The ADE75XX/ADE71XX supports a fully licensed* I²C interface. The I²C interface is implemented as a full hardware master.

SDATA is the data I/O pin, and SCLK is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. Therefore, the user can enable only one interface or the other on these pins at any given time. The SCPS bit in the CFG SFR selects which peripheral is active.

The two pins used for data transfer, SDA and SCL are configured in a Wired-AND format that allows arbitration in a multi-master system.

The transfer sequence of a I2C system consists of a master device initiating a transfer by generating a START condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges then the data transfer is initiated. This continues until the master issues a STOP condition and the bus becomes idle.

SERIAL CLOCK GENERATION

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in Fast mode (256 kHz) or Standard mode (32 kHz).

The bit-rate is defined in the I2CMODE SFR as follow:

$$f_{SCL} = \frac{f_{core}}{16 \times 2^{SCLDIV[1:0]}}$$

SLAVE ADDRESSES

The I2CADR SFR contains the slave device ID. The LSB of this register contains a read/write request. A write to this SFR will start the I²C communication.

I2C SFR REGISTER LIST

The I²C peripheral interface consists of five SFRs:

- I2CMOD
- I2CSTAT
- I2CADR
- SPI2CTx
- SPI2CRx.

As the SPI and I2C serial interfaces share the same pins, I2CMOD, I2CADR, I2CSTAT, SPI2CTx and SPI2CRx SFRs are also shared with SPIMOD1, SPIMOD2, SPISTAT, SPI2CTx and SPI2CRx SFRs respectively.

SFR Address	Name	R/W	Length	Default Value	Description
0x9A	SPI2CTx	W	8		SPI Data out register
0x9B	SPI2CRx	R	8	0	SPI Data in register
0xE8	I2CMOD	R/W	8	0	SPI configuration register
0xE9	I2CADR	R/W	8	0	SPI configuration register
0xEA	I2CSTAT	R/W	8	0	SPI/I2C Interrupt Status register

Table 134: SPI SFR register list

Table 135. I2C Mode Register SFR (I2CMOD, 0xE8)

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0xEF	I2CEN	0	I2C enable bit When this bit is set to logic one, the I2C interface is enabled. A write to the I2CADR SFR will start a communication
6-5	0xEE – 0xED	I2CR[1:0]	0	I2C SCLK frequency [1:0]

				00	F_{core} / 16 = 256kHz if F_{core} = 4.096MHz
				01	F_{core} / 32 = 128kHz if F_{core} = 4.096MHz
				10	F_{core} / 64 = 64Hz if F_{core} = 4.096MHz
				11	F_{core} / 128= 32kHz if F_{core} = 4.096MHz
4-0	0xEC – oxE8	I2CRCT[4:0]	0	Configures the length of the I2C received FIFO buffer. The I2C peripheral will stop when I2CRCT[4:0] + 1 bytes have been read or if an error has occured	

Table 136. I2C Slave Address SFR (I2CADR, 0xE9)

Bit Location	Bit Mnemonic	Default Value	Description
7-1	I2CSLVADR	0	Address of the I2C slave being adressed Writing to this register start the I2C transmission (Read or write)
0	I2CR_W	0	Command bit for Read or Write When this bit is set to logic one, a read command will be transmitted on the I2C bus. Data from slave in SPI2CRx SFR is expected after command byte When this bit is set to logic zero, a write command will be transmitted on the I2C bus. Data to slave is expected in SPI2CTx SFR

Table 137. I2C Interrupt Status Register SFR (I2CSTAT, 0xEA)

Bit Location	Bit Mnemonic	Default Value	Description
7	I2CBUSY	0	This bit is set to logic one when the I2C interface is used. When this bit is set by user code, the Tx FIFO is emptied
6	I2CNOACK	0	I2C no acknlowledgement transmit interrupt This bit is set to logic one when the slave device did not send an acknlowledgement. The I2C communication is stopped after this event. Write a zero to this bit to clear it.
5	I2CRxIRQ	0	I2C receive interrupt This bit is set to logic one when the receive FIFO is not empty Write a zero to this bit to clear it.
4	I2CTxIRQ	0	I2C transmit interrupt This bit is set to logic one when the transmit FIFO is empty Write a zero to this bit to clear it.
3-2	I2CFIFOSTAT[1:0]	0	Status bit for 3 or 4 bytes deep I2C FIFO. The FIFO monitored in these 2 bits is the one currently used in I2C communication (Receive or Transmit) as only one of them is active at a time [1:0] 00 FIFO empty 01 Reserved 10 FIFO Half full 11 FIFO Full
1	I2CACC_ERR	0	Set when trying to write and read at the same time. Write a zero to this bit to clear it.
0	I2CTxWR_ERR	0	Set when write was attempted when I2C transmit FIFO was full. Write a zero to this bit to clear it.

An I2C interrupt occurs

* Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use the ADE7XXX in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

READ AND WRITE OPERATIONS

Figure 85 and Figure 86 depict I2C read and write operations, respectively. Note that the LSB of the I2CADR register is used to select whether a read or write operation is performed on the slave device. During the read operation, the master acknowledges are generated automatically by the I2C peripheral. The master generated NACK before the end of a read operation is also generated automatically after I2CRCT[4:0] bytes have been read from the slave. If the I2CADR register is updated during a transmission, instead of generating a STOP at the end of the read or write operation, the master will generate a START condition and continue with the next communication.

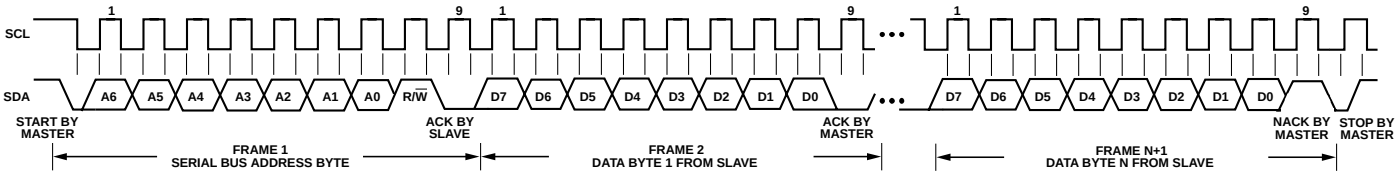


Figure 85: I2C Read operation

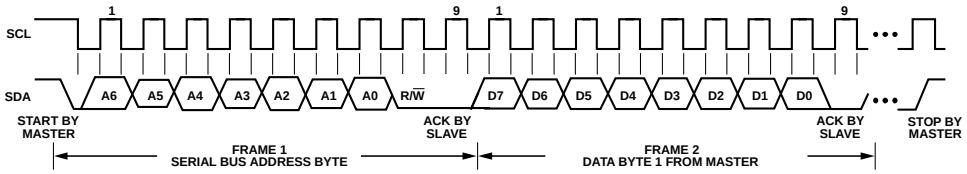


Figure 86: I2C Write operation

I2C RECEIVE AND TRANSMIT FIFOS

The I2C peripheral has a four byte receive FIFO and a four byte transmit FIFO. The buffers reduce the overhead associated with using the I2C peripheral. Figure 87 shows the operation of the I2C receive and transmit FIFOs.

The TX FIFO can be loaded with four bytes to be transmitted to the slave at the beginning of a write operation. When the transmit FIFO is empty, the I2C transmit interrupt flag will be set and the PC will vector to the I2C interrupt vector if this interrupt is enabled. If a new byte is not loaded into the TX FIFO before it is needed in the transmit shift register, the communication will stop. An error such as not receiving an acknowledge will also cause the communication to terminate. In case of an error during a write operation, the TX FIFO will be flushed.

The RX FIFO allows four bytes to be read in from the slave before the MCU has to read the data. A receive interrupt can be generated after each byte is received or when the RX FIFO is full. If the peripheral is reading from a slave address, the communication will stop once the number of received bytes equals the number set in the I2CRCT[4:0] bits. An error such as not receiving an acknowledge will also cause the communication to terminate.

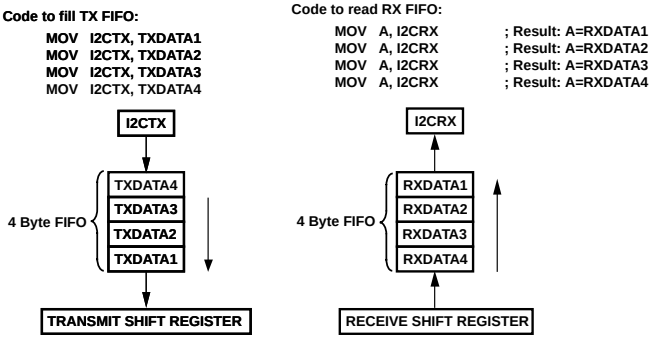


Figure 87: I2C FIFO operation

DUAL DATA POINTERS

The ADE75XX/ADE71XX incorporates two data pointers. The second data pointer is a shadow data pointer and is selected via the data pointer control SFR (DPCON). DPCON features automatic hardware post-increment and post-decrement as well as an automatic data pointer toggle.

Table 138. Data Pointer Control SFR SFR (DPCON, 0xA7)

Bit Location	Bit Mnemonic	Default Value	Description		
7	----	0	Not Implemented. Write Don't Care.		
6	DPT	0	Data Pointer Automatic Toggle Enable. Cleared by the user to disable auto swapping of the DPTR. Set in user software to enable automatic toggling of the DPTR after each MOVX or MOVC instruction.		
5, 4	DP1m1, DP1m0	0	Shadow Data Pointer Mode. These bits enable extra modes of the shadow data pointer operation, allowing more compact and more efficient code size and execution.		
			DP1m1	DP1m0	Behavior of the Shadow Data Pointer
			0	0	8052 behavior.
			0	1	DPTR is post-incremented after a MOVX or a MOVC instruction.
			1	0	DPTR is post-decremented after a MOVX or MOVC instruction.
			1	1	DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.)
3, 2	DP0m1, DP0m0	0	Main Data Pointer Mode. These bits enable extra modes of the main data pointer operation, allowing more compact and more efficient code size and execution.		
			DP0m1	DP0m0	Behavior of the Main Data Pointer
			0	0	8052 behavior.
			0	1	DPTR is post-incremented after a MOVX or a MOVC instruction.
			1	0	DPTR is post-decremented after a MOVX or MOVC instruction.
			1	1	DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction is useful for moving 8-bit blocks to/from 16-bit devices.)
1	----	0	Not Implemented. Write Don't Care.		
0	DPSEL	0	Data Pointer Select. Cleared by the user to select the main data pointer. This means that the contents of this 16-bit register are placed into the DPL, and DPH SFRs. Set by the user to select the shadow data pointer. This means that the contents of a separate 16-bit register appear in the DPL, and DPH SFRs.		

Note the following:

- The Dual Data Pointer section is the only place in which main and shadow data pointers are distinguished.

Whenever the DPTR is mentioned elsewhere in this data sheet, active DPTR is implied.

- Only the MOVC/MOVX @DPTR instructions automatically post-increment and post-decrement the DPTR. Other MOVC/MOVX instructions, such as MOVC PC or MOVC @Ri, do not cause the DPTR to automatically post-increment and post-decrement.

To illustrate the operation of DPCON, the following code copies 256 bytes of code memory at Address D000H into XRAM, starting from Address 0000H.

```
          MOV DPTR,#0       ;Main DPTR = 0
          MOV DPCON,#55H    ;Select shadow DPTR
                            ;DPTR1 increment mode
                            ;DPTR0 increment mode
                            ;DPTR auto toggling ON
          MOV DPTR,#0D000H ;DPTR = D000H
MOVELOOP: CLR A
          MOVC A,@A+DPTR    ;Get data
                            ;Post Inc DPTR
                            ;Swap to Main DPTR(Data)
              MOVX @DPTR,A     ;Put ACC in XRAM
                            ;Increment main DPTR
                            ;Swap Shadow DPTR(Code)
           MOV A, DPL
           JNZ MOVELOOP
```

I/O PORTS

PARALLEL I/O

The ADE75XX/ADE71XX uses three input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some are capable of driving an LCD or performing other alternate functions for the peripheral functions available on-chip. In general, when a peripheral is enabled, the pins associated with it cannot be used as a general-purpose I/O. The I/O port can be configured through the SFRs in Table 139.

Table 139. I/O port SFRs

SFR	Address	Bit Addressable	Description
P0	0x80	Yes	Port 0 register
P1	0x90	Yes	Port 1 register
P2	0xA0	Yes	Port 2 register
EPCFG	0x9F	No	Extended Port Configuration
PINMAP0	0xB2	No	Port 0 weak pull-up enable
PINMAP1	0xB3	No	Port 1 weak pull-up enable
PINMAP2	0xB4	No	Port 2 weak pull-up enable
INTPR	0xFF	No	Interrupt pin configuration

The three bidirectional I/O ports have internal pull-ups that can be enabled or disabled individually for each pin. The internal pull-ups are enabled by default. Disabling an internal pull-up causes a pin to become open-drain. Weak internal pull-ups are configured through PINMAPx SFRs.

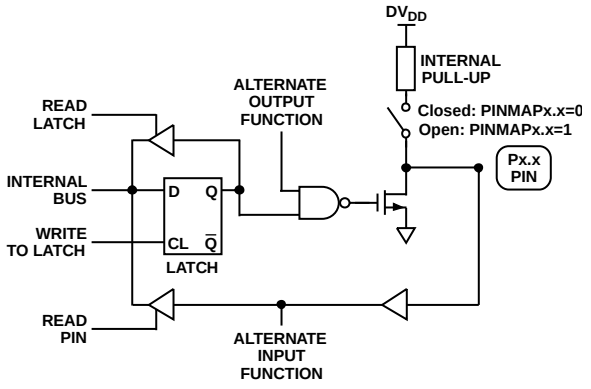


Figure 88. Port 0 Bit Latch and I/O Buffer

Figure 88 shows a typical bit latch and I/O buffer for an I/O pin. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a write to latch signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a read latch signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a read pin signal from the CPU. Some instructions that read a port activate the read latch signal, and others activate the read pin signal. See the Read-Modify-Write Instructions section for details.

Weak Internal Pullups Enabled

A pin with the weak internal pull-up enabled is used as an input by writing a 1 is written to the pin. The pin will be pulled high by the internal pull-ups and the pin will be read using the circuitry shown in Figure 88. If the pin is driven low externally, it will source current because of the internal pull-ups.

If used as an output, a pin with an internal pull-up enabled, will be written with a 1 or a 0 to control the level of the output. If a 0 is written to the pin, it will drive a logic low output voltage (V_{OL}) and is capable of sinking TBD mA.

Open Drain (Weak Internal Pull-ups Disabled)

When the weak internal pull-up on a pin is disabled, the pin becomes open drain. To use this open-drain pin as a high impedance input, a 1 is written to the pin. The pin will be read using the circuitry shown in Figure 88. The open drain option is preferable for inputs because it draws less current than the internal pull-ups were enabled.

To use an open-drain pin as a general purpose output, an external pull-up resistor is required. Open drain outputs are convenient for changing the voltage to a logic high. The ADE75XX/ADE71XX is a 3.3V device so an external resistor pulled up to 5V may ease interfacing to a 5V IC although most 5V ICs are tolerant of 3.3V inputs. Pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

38 kHz Modulation

The ADE75XX/ADE71XX provides a 38 kHz modulation signal. The 38 kHz modulation is accomplished by internally ORing the level written to the MOD38 pin with a 38 kHz square wave. Then when a zero is written to the MOD38 pin, it is modulated as shown in Figure 89.

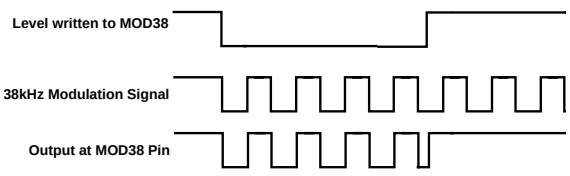


Figure 89: 38 kHz Modulation

Uses for this 38 kHz modulation include IR modulation of a

UART transmit signal or a low power signal to drive a LED. The modulation can be enabled or disabled with the MOD38EN bit in the CFG SFR. The 38 kHz modulation is available on eight pins, selected by the MOD38[7:0] bits in the Extended Port Configuration SFR (EPCFG, 0x9F).

I/O SFR REGISTER LIST

Table 140. Extended Port Configuration SFR (EPCFG, 0x9F)

Bit Location	Bit Mnemonic	Default Value	Description
7	MOD38_FP21	0	Enable 38kHz modulation on P1.6/FP21 pin
6	MOD38_FP22	0	Enable 38kHz modulation on P1.5/FP22 pin
5	MOD38_FP23	0	Enable 38kHz modulation on P1.4/FP23/T2 pin
4	MOD38_TxD	0	Enable 38kHz modulation on P1.1/Tx pin
3	MOD38_CF1	0	Enable 38kHz modulation on P0.2/CF1/RTCCAL pin
2	MOD38_SSb	0	Enable 38kHz modulation on P0.7/$\overline{SS}$/T1pin
1	MOD38_MISO	0	Enable 38kHz modulation on P0.5/MISO pin
0	MOD38_CF2	0	Enable 38kHz modulation on P0.3/CF2 pin

Table 141. Port 0 Weak pull-up enable SFR (PINMAP0, 0xB2)

Bit Location	Bit Mnemonic	Default Value	Description
7	PINMAP0.7	0	The weak pull-up on P0.7 is disabled when this bit is set
6	PINMAP0.6	0	The weak pull-up on P0.6 is disabled when this bit is set
5	PINMAP0.5	0	The weak pull-up on P0.5 is disabled when this bit is set
4	PINMAP0.4	0	The weak pull-up on P0.4 is disabled when this bit is set
3	PINMAP0.3	0	The weak pull-up on P0.3 is disabled when this bit is set
2	PINMAP0.2	0	The weak pull-up on P0.2 is disabled when this bit is set
1	PINMAP0.1	0	The weak pull-up on P0.1 is disabled when this bit is set
0	PINMAP0.0	0	The weak pull-up on P0.0 is disabled when this bit is set

Table 142. Port 1 Weak pull-up enable SFR (PINMAP1, 0xB3)

Bit Location	Bit Mnemonic	Default Value	Description
7	PINMAP1.7	0	The weak pull-up on P1.7 is disabled when this bit is set
6	PINMAP1.6	0	The weak pull-up on P1.6 is disabled when this bit is set
5	PINMAP1.5	0	The weak pull-up on P1.5 is disabled when this bit is set
4	PINMAP1.4	0	The weak pull-up on P1.4 is disabled when this bit is set
3	PINMAP1.3	0	The weak pull-up on P1.3 is disabled when this bit is set
2	PINMAP1.2	0	The weak pull-up on P1.2 is disabled when this bit is set
1	PINMAP1.1	0	The weak pull-up on P1.1 is disabled when this bit is set
0	PINMAP1.0	0	The weak pull-up on P1.0 is disabled when this bit is set

Table 143. Port 2 Weak pull-up enable SFR (PINMAP2, 0xB4)

Bit Location	Bit Mnemonic	Default Value	Description
7 - 6	Reserved	0	Reserved. Should be left cleared
5	PINMAP2.5	0	The weak pull-up on Reset is disabled when this bit is set
4	Reserved	0	The weak pull-up on EA is disabled when this bit is set
3	PINMAP2.3	0	Reserved. Should be left cleared
2	PINMAP2.2	0	The weak pull-up on P2.2 is disabled when this bit is set
1	PINMAP2.1	0	The weak pull-up on P2.1 is disabled when this bit is set
0	PINMAP2.0	0	The weak pull-up on P2.0 is disabled when this bit is set

Table 144. Port 0 SFR (P0, 0x80)

Note: When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7	0x87	T1	1	This bit reflects the state of P0.7/$\overline{SS}$/T1 pin. It can be written or read.
6	0x86	T0	1	This bit reflects the state of P0.6/SCLK/T0 pin. It can be written or read.
5	0x85		1	This bit reflects the state of P0.5/MISO pin. It can be written or read.
4	0x84		1	This bit reflects the state of P0.4/MOSI/SDATA pin. It can be written or read.
3	0x83	CF2	1	This bit reflects the state of P0.3/CF2 pin. It can be written or read.
2	0x82	CF1	1	This bit reflects the state of P0.2/CF1/RTCCAL pin. It can be written or read.
1	0x81		1	This bit reflects the state of P0.1 pin. It can be written or read.
0	0x80	$\overline{INT1}$	1	This bit reflects the state of P0.0/$\overline{INT1}$/BCTRL pin. It can be written or read.

Table 145. Port 1 SFR (P1, 0x90)

Note: When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set

Bit Location	Bit Addr.	Bit Name	Default value	Description
7	0x97		1	This bit reflects the state of P1.7 pin. It can be written or read.
6	0x96		1	This bit reflects the state of P1.6 pin. It can be written or read.
5	0x95		1	This bit reflects the state of P1.5 pin. It can be written or read.
4	0x94	T2	1	This bit reflects the state of P1.4/T2 pin. It can be written or read.
3	0x93	T2EX	1	This bit reflects the state of P1.3/T2EX pin. It can be written or read.
2	0x92		1	This bit reflects the state of P1.2 pin. It can be written or read.
1	0x91	TxD	1	This bit reflects the state of P1.1/TxD pin. It can be written or read.
0	0x90	RxD	1	This bit reflects the state of P1.0/RxD pin. It can be written or read.

Table 146. Port 2 SFR (P2, 0xA0)

Note: When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set

Bit Location	Bit Addr.	Bit Name	Default Value	Description
7 - 2	0x97 – 0x92		0x3F	These bits are unused and should be left set
1	0x91	P2.1	1	This bit reflects the state of P2.1 pin. It can be written or read.
0	0x90	P2.0	1	This bit reflects the state of P2.0 pin. It can be written or read.

Interrupt pins configuration SFR (INTPR, 0xFF)

Bit Location	Bit Mnemonic	Default Value	Description		
7	RTCCAL	0	Control RTC calibration output When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.		
6-5	FSEL[1:0]		Sets RTC calibration output frequency and calibration window		
			FSEL[1:0]		Calibration window, frequency
			0	0	30.5 seconds, 1Hz
			0	1	30.5 seconds, 512 Hz
			1	0	0.244 seconds, 500Hz
			1	1	0.244 seconds, 16.384 kHz
4	Reserved				
3-1	INT1PRG[2:0]	000	Controls the function of $\overline{INT1T}$		
			INT1PRG[2:0]		Function

			x	0	0	GPIO
			x	0	1	BCTRL
			0	1	x	$\overline{\text{INT1}}$ input disabled
			1	1	x	$\overline{\text{INT1}}$ input enabled
0	INT0PRG	0	Controls the function of $\overline{\text{INT0}}$			
			INT0PRG			Function
			0			$\overline{\text{INT0}}$ input disabled
			1			$\overline{\text{INT0}}$ input enabled

Table 147.Table 148. Port 0 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P0.0	BCTRL external battery control input	Set INT1PROG[2:0]=X01 in the Interrupt pins configuration SFR (INTPR, 0xFF)
	$\overline{\text{INT1}}$ external interrupt	Set EX1 in the Interrupt Enable SFR (IE, 0xA8).
	$\overline{\text{INT1}}$ wakeup from PSM2 operating mode	Set INT1PROG[2:0]=11X in the Interrupt pins configuration SFR (INTPR, 0xFF)
P0.1	FP19 LCD Segment Pin	Set FP19EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)
P0.2	CF1 ADE Calibration Frequency output	Clear the DISCF1 bit in the ADE energy measurement internal MODE1 register (0x0B)
	RTC Calibration output	Select the calibration window and frequency options and then set the RTCCAL bit in the Interrupt pins configuration SFR (INTPR, 0xFF)
	Note: The RTC Calibration output has priority over the CF1 output, so if the DISCF1 in the MODE1 register (0x0B) is clear and RTCCAL bit in the Interrupt pins configuration SFR (INTPR, 0xFF) is set, the P0.2/CF1/RTCCAL pin will follow the RTC Calibration output.	
P0.2	CF1 ADE Calibration Frequency output	Clear the DISCF1 bit in the ADE energy measurement internal MODE1 register (0x0B)
P0.3	CF2 ADE Calibration Frequency output	Clear the DISCF2 bit in the ADE energy measurement internal MODE1 register (0x0B)
P0.4	MOSI SPI Data line	Set the SCPS bit in the CFG SFR and set the SPIEN bit in the SPI Configuration Register SFR (SPIMOD1, 0xE8).
	SDATA I^2C Data line	Clear the SCPS bit in the Configuration SFR (CFG, 0xAF) and set the I2CEN bit in the I2C Mode Register SFR (I2CMOD, 0xE8).
P0.5	MISO SPI Data line	Set the SCPS bit in the Configuration SFR (CFG, 0xAF) and set the SPIEN bit in the SPI Configuration Register SFR (SPIMOD2, 0xE9)
P0.6	SCLK serial clock for I^2C or SPI	Set the I2CEN bit in the I2CMOD SFR or the SPIEN bit in the SPI Configuration Register SFR (SPIMOD2, 0xE9) to enable the I^2C or SPI interface
	T0 Timer0 input	Set the CNT0 bit in the Timer/Counter 0 and 1 Mode SFR (TMOD, 0x89) to enable T0 as an external event counter
P0.7	$\overline{\text{SS}}$ SPI slave select input for SPI in slave mode	Set the SS_EN bit in the SPI Configuration Register SFR (SPIMOD1, 0xE8)
	$\overline{\text{SS}}$ SPI slave select output for SPI in master mode	Set the SPIMS_b bit in the SPI Configuration Register SFR (SPIMOD2, 0xE9)
	T1 Timer 1 input	Set the CNT1 bit in the Timer/Counter 0 and 1 Mode SFR (TMOD, 0x89) to enable T1 as an external event counter

Table 149. Port 1 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P1.0	RxD Receiver Data Input for UART	Set the REN bit in the SCON SFR Bit Description SFR (SCON, 0x98).
	RX Edge wakeup from PSM2 operating mode	Set RXPROG[1:0]=11 in the Peripheral Configuration SFR (PERIPH, 0xF4)
P1.1	TxD Transmitter Data Output for UART	
P1.2	FP25 LCD Segment Pin	Set FP25EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)
P1.3	FP24 LCD Segment Pin	Set FP24EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)
	T2EX Timer 2 control input	Set EXEN2 in the Timer/Counter 2 Control SFR (T2CON, 0xC8)
P1.4	FP23 LCD Segment Pin	Set FP23EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)
	T2 Timer 2 input	Set the CNT2 bit in the Timer/Counter 2 Control SFR (T2CON, 0xC8) to enable T2 as an external event counter
P1.5	FP22 LCD Segment Pin	Set FP22EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)
P1.6	FP21 LCD Segment Pin	Set FP21EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)
P1.7	FP20 LCD Segment Pin	Set FP20EN in the LCD Segment Enable SFR (LCDSEGE, 0x97)

Table 150. Port 2 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P2.0	FP18 LCD Segment Pin	Set FP18EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)
P2.1	FP17 LCD Segment Pin	Set FP17EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)
P2.2	FP16 LCD Segment Pin	Set FP16EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)
P2.3	$\overline{\text{SDEN}}$ Serial Download pin sampled on reset. P2.3 is an output only.	Enabled by default.

PORT 0

Port 0 is controlled directly through the bit-addressable Port 0 SFR (80H). The weak internal pull-ups for Port 0 are configured through the Port 0 Weak pull-up enable SFR (PINMAP0, 0xB2); they are enabled by default. Disable the weak internal pull-up by writing a one to P0CFG..x.

Port 0 pins also have various secondary functions as described in **Interrupt pins configuration SFR (INTPR, 0xFF)**

Bit Location	Bit Mnemonic	Default Value	Description			
7	RTCCAL	0	Control RTC calibration output When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.			
6-5	FSEL[1:0]		Sets RTC calibration output frequency and calibration window			
			FSEL[1:0]		Calibration window, frequency	
			0	0	30.5 seconds, 1Hz	
			0	1	30.5 seconds, 512 Hz	
			1	0	0.244 seconds, 500Hz	
			1	1	0.244 seconds, 16.384 kHz	
4	Reserved					
3-1	INT1PRG[2:0]	000	Controls the function of T			
			INT1PRG[2:0]			Function
			x	0	0	GPIO

			x	0	1	BCTRL
			0	1	x	input disabled
			1	1	x	input enabled
0	INT0PRG	0	Controls the function of			
			INT0PRG			Function
			0			input disabled
			1			input enabled

Table 147.Table 148. The alternate functions of Port 0 pins can be activated only if the corresponding bit latch in the P0 SFR contains a 1. Otherwise, the port pin remains at 0.

PORT 1

Port 1 is an 8-bit bidirectional port controlled directly through the bit-addressable Port 1 SFR (90H). The weak internal pull-ups for Port 1 are configured through the Port 1 Weak pull-up enable SFR (PINMAP1, 0xB3); they are enabled by default. Disable the weak internal pull-up by writing a one to P1CFG..x.

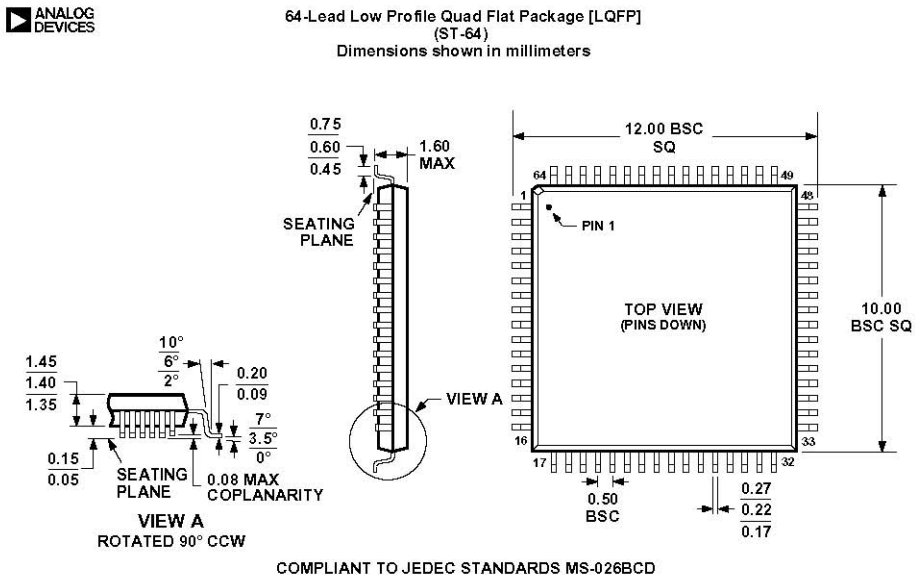
Port 1 pins also have various secondary functions as described in Table 149. The alternate functions of Port 1 pins can be activated only if the corresponding bit latch in the P1 SFR contains a 1. Otherwise, the port pin remains at 0.

PORT 2

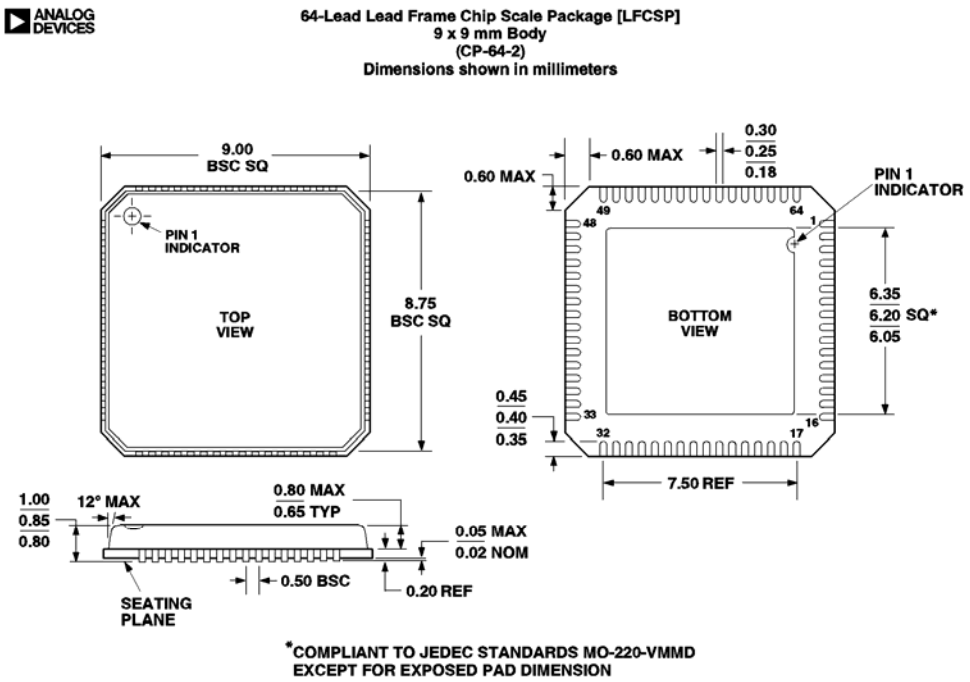
Port 2 is a 4-bit bidirectional port controlled directly through the bit-addressable Port 2 SFR (A0H). Note that P2.3 can be used as an output only. The weak internal pull-ups for Port 2 are configured through the Port 2 Weak pull-up enable SFR (PINMAP2, 0xB4); they are enabled by default. Disable the weak internal pull-up by writing a one to P2CFG..x.

Port 2 pins also have various secondary functions as described in Table 150. The alternate functions of Port 2 pins can be activated only if the corresponding bit latch in the P2 SFR contains a 1. Otherwise, the port pin remains at 0.

OUTLINE DIMENSIONS



LQFP package



LFCSP package[17]

Dimensions shown in millimeters

[17] Please contact your Analog Devices representative to check availability of this package

SELECTION GUIDE

Table 151. Selection Guide

Part Number	Antitamper	W + VA + rms	VAR	5V LCD	RTC	Flash (kB)	Package
ADE7166	Yes	Yes	No	Yes	Yes	8/16	64-LQFP or LFCSP
ADE7169	Yes	Yes	Yes	Yes	Yes	16	64-LQFP or LFCSP
ADE7566	No	Yes	No	Yes	Yes	8/16	64-LQFP or LFCSP
ADE7569	No	Yes	Yes	Yes	Yes	16	64-LQFP or LFCSP

ORDERING GUIDE

Table 152. Ordering Guide

Model	Package Description	Package Option*	Temperature Range
ADE7169ASTZF16	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7169ASTZF16-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7169ACPZF16[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7169ACPZF16-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
ADE7166ASTZF16	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7166ASTZF16-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7166ACPZF16[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7166ACPZF16-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
ADE7166ASTZF8	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7166ASTZF8-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7166ACPZF8[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7166ACPZF8-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
ADE7569ASTZF16	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7569ASTZF16-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7569ACPZF16[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7569ACPZF16-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
ADE7566ASTZF16	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7566ASTZF16-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7566ACPZF16[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7566ACPZF16-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
ADE7566ASTZF8	64-Lead Lead Free LQFP	LQFP-64	−40°C to +85°C
ADE7566ASTZF8-RL	64-Lead Lead Free LQFP in Reel	LQFP-64	−40°C to +85°C
ADE7566ACPZF8[1]	64-Lead Lead Free CSP	LFCSP-64[1]	−40°C to +85°C
ADE7566ACPZF8-RL[1]	64-Lead Lead Free CSP in Reel	LFCSP-64[1]	−40°C to +85°C
EVAL-ADE7169F16EB	ADE7169 Evaluation Board		−40°C to +85°C

[1] Please contact your Analog Devices representative to check availability of this package

PR06717-0-1/07(PrE)