M6759(1)

8-bit MTP Micro-controller

Version 1.01

M6759 : 8-bit MTP Micro-controller

Section 1 : Features

- **8051 instruction set compatible 8-bit micro-controller**
- **8051/8052 compatible pinout**
- **Complete static design, wide range of operation frequency from 1 ~ 40 MHz**
- **Large on-chip memory**
  - 64K bytes built-in Multiple Times Programmable ROM (MTP-ROM) program memory
  - 512 bytes on-chip SRAM, expandable external 64K bytes address space
- **Dual Data Pointer**
- **Four 8-bit bi-directional I/O ports**
- **6 interrupts including 2 external sources**
- **One full-duplex serial UART ports compatible with standard 8052**
- **Three 16 bit timer/counters**
- **On chip oscillator for crystal**
- **Software Power-Down mode, supports Idle mode and Power Down mode for less power consumption**
- **ROM Code Protection**
- **4.5V~5.5V operation voltage, 12V programming voltage**
- **44-pin PLCC or QFP package**

1.1 General Description

The M6759 is an 8032/8052 instruction compatible 8-bit microcontroller with MTP Flash ROM for firmware updating. By combining a versatile 8-bit CPU with MTP-Flash, this device provides whole microcontroller system on one chip and still remains the feasibility for general control systems in a variety of applications. Furthermore, user-defined security registers can protect the firmware after the code is ready.

The M6759 contains the following: a) a non-volatile 64K bytes Multiple Times Programmable ROM program memory. b) a volatile 512 bytes read/write data memory c) four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51). d) a 16-bit timer (identical to the Timer 2 of the 8052). e) a multi-source two-priority-level nested interrupt structure. f) one serial interface (UART) and g) an on-chip oscillator.

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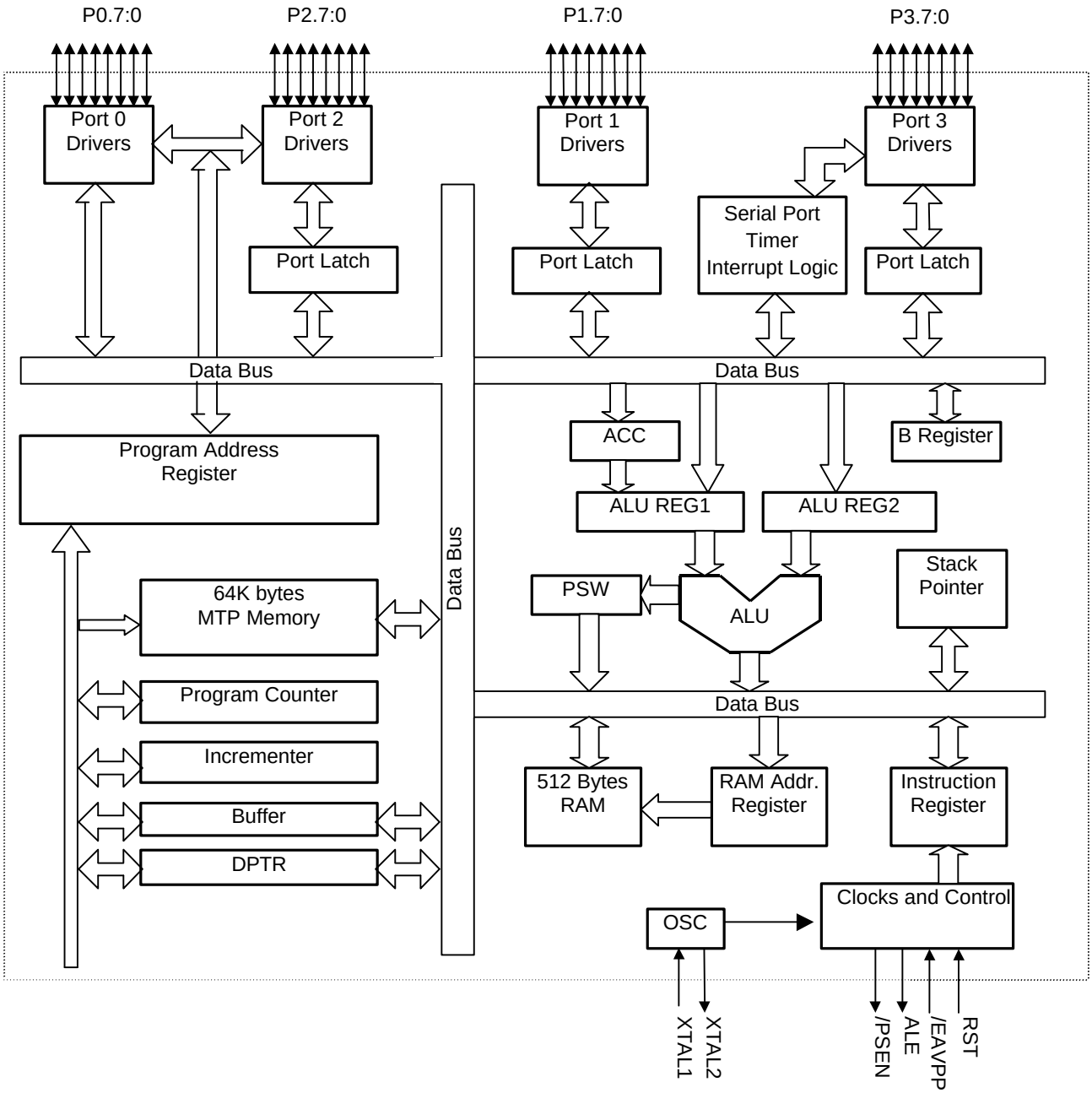
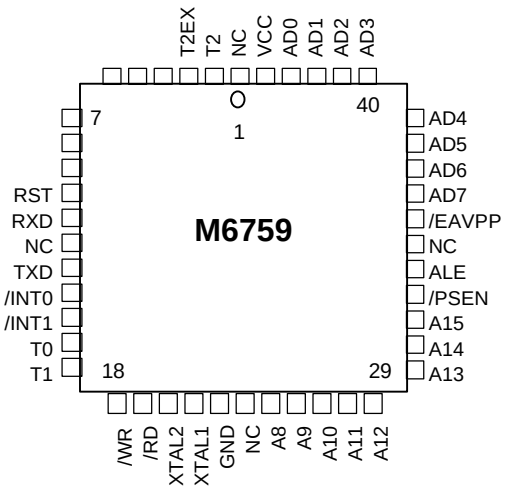
1.2 Block Diagram

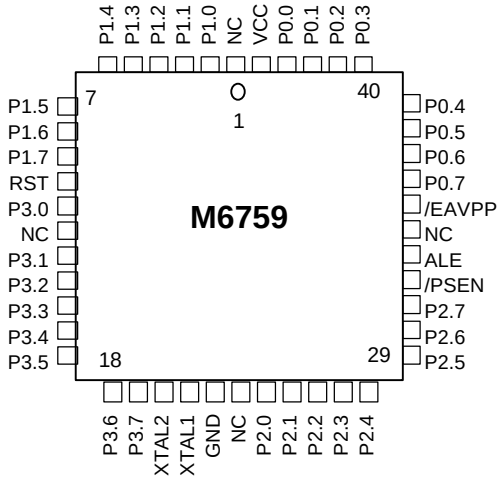


Section 2 : Pin Description

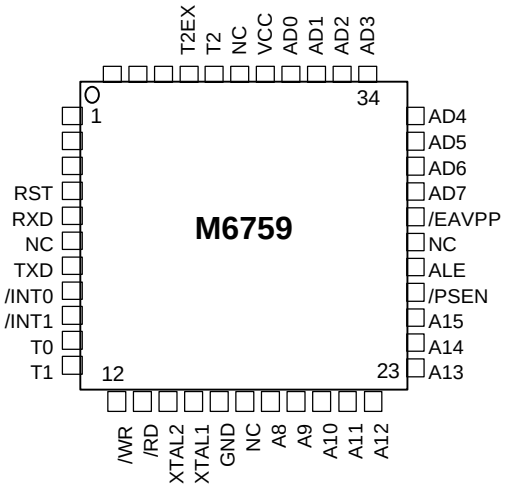
2.1 Pinout Diagram

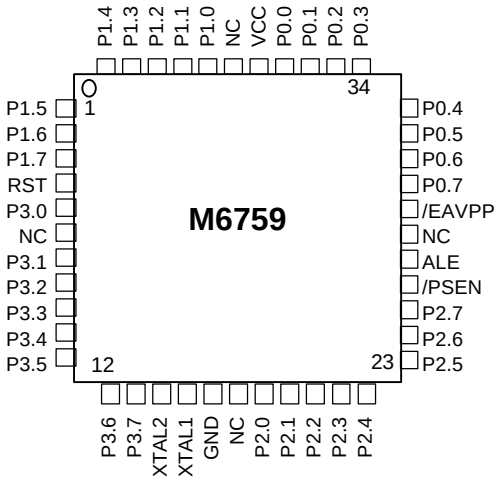
2.1.1 44-pin PLCC Package





2.1.2 44-pin QFP Package





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2.2 Pin Description Table:

Pin assignments shown below are listed based on 44-pin PLCC package. And if not additionally specified, further pin number reference throughout this datasheet is, by default, referred to 44-pin PLCC package. As for the QFP package, the pin number assignment should be shifted accordingly, as comparatively shown in Section 2.1 Pinout Diagram.

Pin Name	No. (PLCC)	Type	Description
VDD	44	IN	Power supply for internal operation, 5V input.
GND	22	IN	Ground.
P0.7-P0.0	36,37,38,39, 40,41,42, 43	I/O	Port 0 is 8 bits bi-directional I/O port with internal pull high.
AD7-0			Multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bi-directional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals.
RST	10	IN	Reset signal of internal circuit, it must be kept 4 clocks to ensure being recognized by internal circuit. This signal will not affect internal SRAM.
XTAL1	21	IN	Crystal In, can be used as external clock input.
XTAL2	20	OUT	Crystal out, feedback of XTAL1.
/PSEN	32	OUT	Program Store Enable Output, commonly connected to external ROM memory as a chip enable during fetching and MOVC operation. /PSEN goes high during a reset condition.
ALE	33	OUT	Address Latch Enable, used to latch external LSB 8 bit address bus from multiplexed address/data bus, commonly connect to the latch enable of 373 family. This signal will be forced high when the device is in a reset condition.
P1.7-P1.0	9,8,7,6,5,4,3 ,2	I/O	Port 1 is 8 bits bi-directional I/O port with internal pull high. All pins have an alternate function shown as below.
T2EX (P1.1)		IN	External timer/counter 2 trigger.
T2 (P1.0)		IN	External timer/counter 2.
P2.7-P2.0	31,30,29,28, 27,26,25, 24	I/O	Port 2 is 8 bits bi-directional I/O port with internal pull high. The alternate function is MSB 8 bit address bus
A15-A8		OUT	This bus emits the high-order address byte during fetches from external Program Memory or during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
P3.7-P3.0	19,18,17,16, 15,14,13, 11	I/O	Port 3 is an 8-bit bi-directional I/O port with internal pull high. The reset condition of this port is with all bits at a logic 1. Port 3 also have alternate function list below
/RD (P3.7)		OUT	External data memory read strobe.
/WR (P3.6)		OUT	External data memory write strobe.
T1 (P3.5)		IN	External timer/counter 1.
T0 (P3.4)		IN	External timer/counter 0.
/INT1 (P3.3)		IN	External interrupt 1 (Negative Edge Detect).
/INT0 (P3.2)		IN	External interrupt 0 (Negative Edge Detect).
TXD (P3.1)		OUT	Serial port output.
RXD (P3.0)		IN	Serial port input.
/EAVPP	35	IN	The pin must be externally held low to enable the device to fetch code from external program memory. If /EAVPP is held high, the device executes from internal program memory. /EAVPP is internal latched on reset. This pin also receives the 12V programming voltage (V_{PP}) during FLASH programming.
NC	1,12,23,34	NC	These pins should not be connected for any purpose

Section 3 : Function Description

3.1 Data Space Addressing

The M6759 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes auxiliary RAM (ARAM).
The four segments are:

1. The Lower 128 bytes of RAM (address 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (address 80H to FFH) are indirectly addressable only.
3. The Special Function Registers SFRs, (address 80H to FFH) are directly addressable only.
4. The 256-bytes auxiliary RAM (ARAM, 0000H-00FFH) are indirectly accessed by move external instruction, MOVX.

Either direct or indirect addressing can access the lower 128 bytes. The upper 128 bytes can be accessed by indirect address only. The upper 128 bytes occupy the same address space as the SFRs. That means they have the same address, but are physically separate from SFR space.
The ARAM can be accessed by indirect addressing and MOVX instructions when ARAM_EN bit is set. This part of memory is physically located on-chip, logically occupied the first 256-bytes of external data memory if ARAM_EN bit is set.
The ARAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ARAM will not affect ports P0, P3.6 (/WR) and P3.7 (/RD).
If ARAM_EN is cleared, the access to external memory will be performed in the same way as standard 8051.
If ARAM_EN is set and DPTR contains value lower than 0100H, the ARAM will be accessed rather than external memory, but if DPTR contains value higher than 00FFH (i.e. 0100H to FFFFH), the external memory will be accessed.
If ARAM_EN is set and P2 SFR contains 00H, the ARAM will be accessed by the MOVX @Ri, #data instruction, but if P2 SFR contains a non-zero value, the external memory will be accessed using MOVX @Ri, #data.

For example,

```
MOVX    DPTR, #data
```

If ARAM_EN is set and DPTR contains 0030H, access the ARAM at address 030H rather than external memory.
If ARAM_EN is set and DPTR contains 0130H, the external memory address 0130H will be accessed
For example:

```
MOVX    @R0, #data
```

If ARAM_EN is set, P2 SFR contains 00H, and R0 contains 30H, an access to the ARAM at address 30H will be performed.
If ARAM_EN is set, P2 SFR contains 01H, and R0 contains 30H, an access to the external memory address 0130H will be performed if P2 is connected to the high byte address bus of external RAM.

3.2 Dual Data Pointer

Data memory block moves can be accelerated using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the M6759, the standard 16-bit data pointer is called DPTR0 and is located at SFR address 82H and 83H. These are the standard locations. The new DPTR is located at SFR 84H and 85H and is called DPTR1. The new DPTR Select bit (DPS) chooses the active pointer and is located at the LSB of the SFR location 86H. No other bits in register 86H have any effect and are set to 0. The user switches between data pointer by toggling the LSB of register 86H. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity.

3.3 Low EMI Mode

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purpose. Note, however, that one ALE pulse is skipped during each access to external Data Memory.
If desired, setting bit 0 of SFR location 8EH can disable ALE operation. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the micro-controller is in external execution mode.

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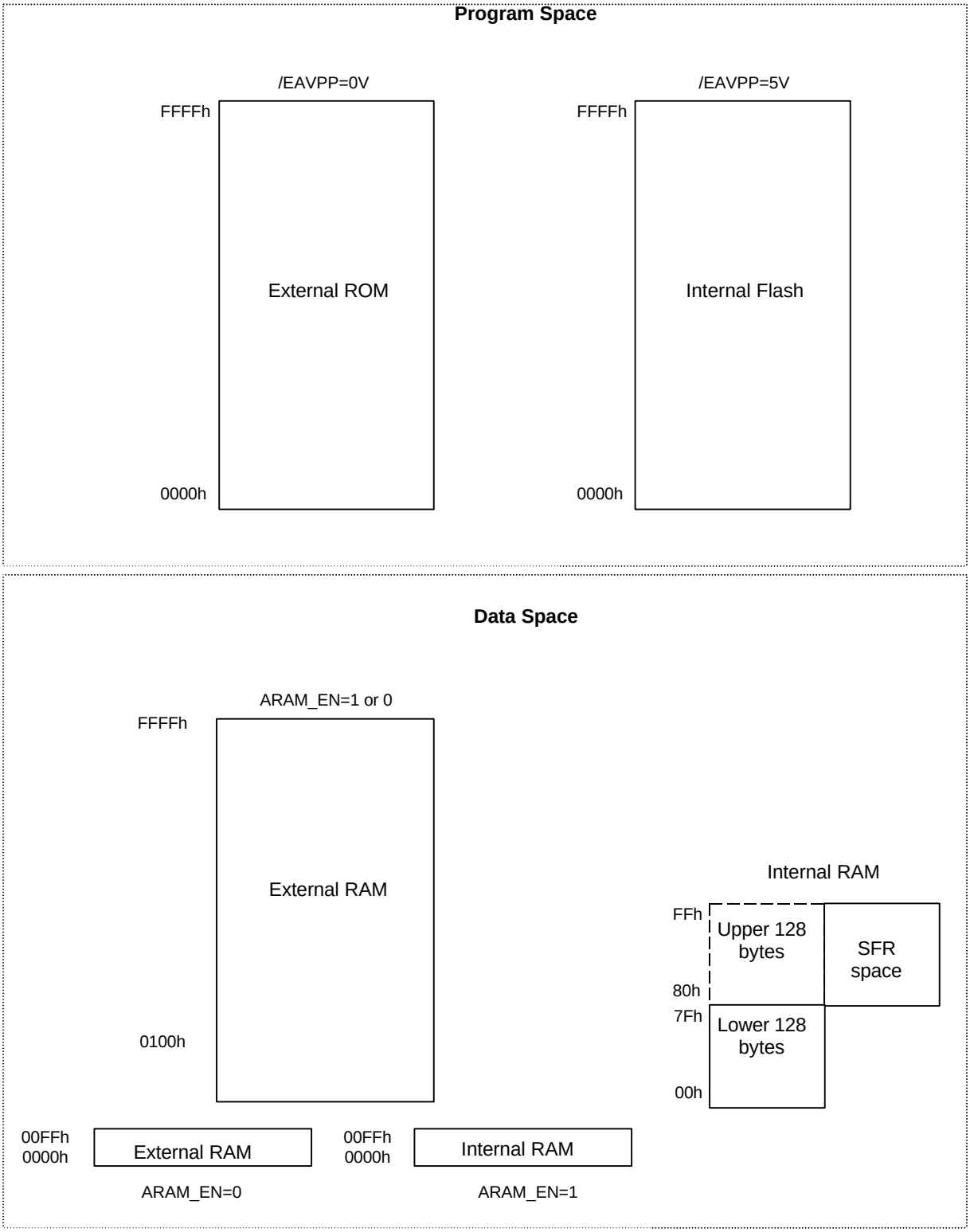
Memory Map


Program Space
/EAVPP=0V
FFFFh
External ROM
0000h
/EAVPP=5V
FFFFh
Internal Flash
0000h
Data Space
ARAM_EN=1 or 0
FFFFh
External RAM
0100h
Internal RAM
FFh
Upper 128 bytes
SFR space
80h
7Fh
Lower 128 bytes
00h
00FFh
0000h
External RAM
ARAM_EN=0
00FFh
0000h
Internal RAM
ARAM_EN=1

3.4 Idle Mode

In Idle mode, CPU put itself into sleep while all the on-chip peripherals remain active. The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. The content of RAM and special functions register remain unchanged, and the status of CPU (includes Stack Point, Program Counter, Program Status Word and Accumulator) is preserved in this mode.

There are two ways to terminate Idle mode:

- Activation of any enabled interrupt will cause IDLE (PCON.0) to be cleared by hardware terminating Idle mode. The interrupt will be serviced, and returned by instruction RETI. The next instruction to be executed is the one which follows the instruction that wrote a logic 1 to PCON.0.
  The flag bits GF0 (PCON.2) and GF3 (PCON.6) can be used to determine whether the interrupt was received during normal execution or during the Idle mode. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

- The second way of terminating the Idle mode is with an external hardware reset.

3.5 PowerDown Mode

Setting PCON.1 (PD) can force CPU enter Power Down mode. In this mode, on-chip oscillator is stopped to save most of power. All functions are stopped due to the clock frozen, but the contents of RAM and special functions register are held.

To terminate Power Down mode, the only way is hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart stably.

3.6 Reset

The RST is the reset input, which is the input to a Schmitt Trigger. A reset is accomplished by holding the RST pin high for at least four oscillator periods while the oscillator is running. The CPU responds by generating an internal reset, with the timing shown in Reset Timing.

The external reset signal is synchronous to the internal clock. The port pins will maintain high by internal pullups for 205 oscillator periods after RST pin goes low. While the RST pin is high, ALE and /PSEN are weakly pulled high. After RST is pulled low, it will take about 205 oscillator periods for ALE and PSEN to start clocking. For this reason, other devices can not be synchronized to the internal timings of the m6759. Driving the ALE and /PSEN pins to 0 while reset is active could cause the device to go into an indeterminate state.

The internal reset algorithm writes 0s to all the SFRs except the port latches, the Stack Pointer, and SBUF. The port latches are initialized to FFH, the Stack Pointer to 07H, and SBUF is indeterminate. The internal RAM is not affected by reset. On power up the RAM content is indeterminate.

3.7 Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt, as listed in Table 11. The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-priority level interrupt can only be interrupted by high-priority level interrupt. An ISR for a high-priority level cannot be interrupted by any other interrupt.

M6759 always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP or IE SFRs, M6759 completes one additional instruction before servicing the interrupt.

3.8 Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts. When EA=1, each interrupt is enabled/masked by its individual enable bit. When EA=0, all interrupts are masked.

3.9 Interrupt Priorities

There are two stages of interrupt priority assignment, interrupt level and natural priority. The interrupt level (high or low) takes precedence over natural priority. All interrupts can be assigned to be high or low priority. In addition to an assigned priority level, each interrupt also has a natural priority, as listed in Table 3-2. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if /INT0 and /INT1 are both programmed as high priority, /INT0 takes precedence.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

Mode	Program Memory	ALE	/PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Table 3-1. Status of the External pins During Idle and Power Down

Reset Timing

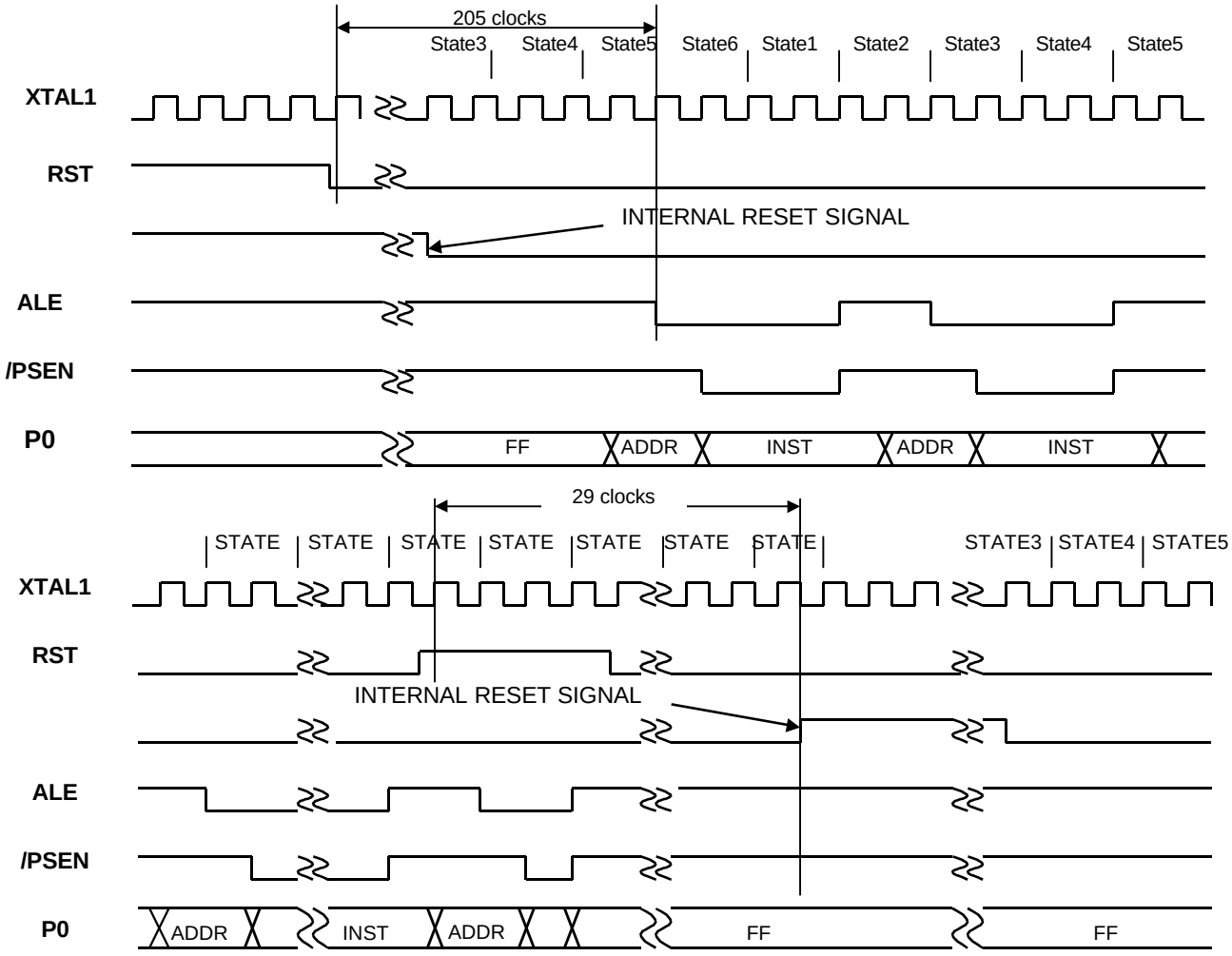


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Table 3-2. Interrupt Natural Vectors and Priorities

Interrupt	Description	Natural Priority	Interrupt Vector
	External interrupt 0	0	
TF0	Timer 0 interrupt		0BH
/INT1		2	13H
	Timer 1 interrupt	3	
TI or RI	Serial Port transmit or receive interrupt		23H
TF2		5	2BH

Interrupt	Description		Enable	Priority Control
	External interrupt 0	TCON.1		IP.0
TF0		TCON.5	IE.1	
/INT1	External interrupt 1		IE.2	IP.2
	Timer 1 interrupt	TCON.7		IP.3
TI or RI		SCON0.0 SCON0.1		IP.5
TF2		T2CON.7	IE.6	

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Section 4 : Special Function Registers

SFR Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
P0									80H
SP									81H
DPL0									82H
DPH0									83H
DPL1									84H
DPH1									85H
DPS	0	0	0	0	0	0	0	SEL	86H
PCON	SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	87H
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88H
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	89H
TL0									8AH
TL1									8BH
TH0									8CH
TH1									8DH
LEMI	0	0	0	0	0	0	0	LOWEMI	8EH
P1									90H
AUXR	ARAM_EN	GF6	GF5	*EB	*BRG1	*BRG0	*INT2I	*INT2E	97H
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	98H
SBUF									99H
P2									A0H
IE	EA	*EX2	ET2	ES0	ET1	EX1	ET0	EX0	A8H
P3									B0H
IP	1	*PX2	PT2	PS0	PT1	PX1	PT0	PX0	B8H
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	C8H
RCAP2L									CAH
RCAP2H									CBH
TL2									CCH
TH2									CDH
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0H
ACC									E0H
*P4									E8H
B									F0H
*P5									F8H

All registers labeled with * can be only used in 68-pin package (not available now)

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SFR Register Initial Value

	Bit 7	Bit 6		Bit 4	Bit 3		Bit 1	Bit 0	
P0	1	1	1	1	1	1	1	1	80H
SP	0	0	0	0	0	1	1	1	81H
DPL0	0	0	0	0	0	0	0	0	82H
DPH0	0	0	0	0	0	0	0	0	83H
DPL1	0	0	0	0	0	0	0	0	84H
DPH1	0	0	0	0	0	0	0	0	85H
DPS	0	0	0	0	0	0	0	0	86H
PCON	0	0	0	0	0	0	0	0	87H
TCON	0	0	0	0	0	0	0	0	88H
TMOD	0	0	0	0	0	0	0	0	89H
TL0	0	0	0	0	0	0	0	0	8AH
TL1	0	0	0	0	0	0	0	0	8BH
TH0	0	0	0	0	0	0	0	0	8CH
TH1	0	0	0	0	0	0	0	0	8DH
LEMI	0	0	0	0	0	0	0	0	8EH
P1	1	1	1	1	1	1	1	1	90H
AUXR	0	0	0	0	1	1	0	0	97H
SCON	0	0	0	0	0	0	0	0	98H
SBUF	0	0	0	0	0	0	0	0	99H
P2	1	1	1	1	1	1	1	1	A0H
IE	0	0	0	0	0	0	0	0	A8H
P3	1	1	1	1	1	1	1	1	B0H
IP	0	0	0	0	0	0	0	0	B8H
T2CON	0	0	0	0	0	0	0	0	C8H
RCAP2L	0	0	0	0	0	0	0	0	CAH
RCAP2H	0	0	0	0	0	0	0	0	CBH
TL2	0	0	0	0	0	0	0	0	CCH
TH2	0	0	0	0	0	0	0	0	CDH
PSW	0	0	0	0	0	0	0	0	D0H
ACC	0	0	0	0	0	0	0	0	E0H
P4	1	1	1	1	1	1	1	1	E8H
B	0	0	0	0	0	0	0	0	F0H
P5	1	1	1	1	1	1	1	1	F8H

Register Definition

SFR 86H : DPS Register, Data Pointer Select Register

Bit	
7-1	0
0	SEL. The DPTR Select bit. When SEL=0, DPTR0 is the active pointer. When SEL=1, DPTR1 is the active pointer.

SFR 87H : PCON Register, Power Control Register

Bit	Description
7	SMOD, Double Baud Rate bit. If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is doubled when the Serial Port is used in modes 1, 2 or 3.
6-2	GF3~GF0, General Purpose Flag bit.
1	PD, Power Down bit.
0	IDLE, Idle Mode bit.

SFR 8EH : LEMI Register, Low EMI Control Register

Bit	Description
7-1	0
0	LOWEMI, The Low EMI Setting bit. If the M6759 operate in the internal access mode, ALE is active only during a MOVX instruction when LOWEMI=1.

SFR 97H : AUXR Register, Auxiliary Register

Bit	Description
7	ARAM_EN, Access Internal Auxiliary RAM Enable bit. When ARMA_EN=0, the access of external RAM will be performed by MOVX. When ARAM_EN=1, access internal auxiliary RAM rather than external RAM.
6-5	GF6-GF5. General Purpose Flag bit.
4-0	Reserved.

SFR D0H : PSW Register, Program Control Register

Bit	Description
7	CY, Carry Flag. Set to 1 when the last arithmetic operation results in a carry into (during addition) or borrow from (during subtraction) the high order nibble. Otherwise, this bit is cleared to 0 by all arithmetic operations.
6	AC, Auxiliary Carry Flag. Set to 1 when the last arithmetic operation results in a carry into (during addition) or borrow from (during subtraction) the high order nibble. Otherwise, this bit cleared to 0 by all arithmetic operations.
5	F0, User Flag 0, user addressable. Generates purpose flag for software control.
4-3	RS1-0, Register Bank Select **RS1 RS0 Bank Selected** 0 0 Register Bank 0, address 00h-07h 0 1 Register Bank 1, address 08h-0Fh 1 0 Register Bank 2, address 10h-17h 1 1 Register Bank 3, address 17h-1Fh
2	OV, Overflow Flag. Set to 1 when the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, this bit is cleared to 0 by all arithmetic operations.
1	GF, User Flag 1, user addressable. Generator purpose flag for software control.
0	F1, Parity Flag. Set to 1 when the modulo-2 sum of the 8 bits in the accumulator is 1 (odd parity), clear to 0 on even parity.

SFR A8H : IE Register

Bit	
7	EA, Global Interrupt Enable. Controls masking of all interrupts except power fail interrupt. EA=0 disable all interrupts (EA overrides individual interrupt enable bits). When EA=1, each interrupt is enabled or masked by its individual enable bit.
6	Reserved.
5	ET2, Enable External Timer 2. ET2=0 disables Timer 2 interrupt (TF2). ET2=1 enables interrupts generated by TF2 flag.
4	ES0, Enable Serial Port 0 Interrupt. ES0=0 disables Serial Port 0 interrupts (TI_0 and RI_0). ES0=1 enables interrupts generated by the TI_0 or RI_0 flag.
3	ET1, Enable External Timer 1. ET1=0 disables Timer 1 interrupt (TF1). ET1=1 enables interrupts generated by TF1 flag.
2	EX1, Enable External Interrupt 1. EX1=0 disables external interrupt 1 (/INT1). EX1=1 enables interrupts generated by /INT1.
1	ET0, Enable External Timer 0. ET0=0 disables Timer 0 interrupt (TF0). ET0=1 enables interrupts generated by TF0 flag.
0	EX0, Enable External Interrupt 0. EX0=0 disables external interrupt 0 (/INT0). EX0=1 enables interrupts generated by /INT0.

SFR B8H : IP Register

Bit	Description
7	Reserved, read as 1.
6	Reserved.
5	PT2, Timer 2 Interrupt Priority Control. PT2=0 sets Timer 2 interrupt (TF2) to low priority. PT2=1 sets Timer 2 interrupt to high priority.
4	PS0, Serial Port 0 Interrupt Priority Control. PS0=0 sets Serial Port 0 interrupts (TI_0 and RI_0) to low priority. PS0=1 sets Serial Port 0 to high priority.
3	PT1, Timer 1 Interrupt Priority Control. PT1=0 sets Timer 1 interrupt (TF1) to low priority. PT1=1 sets Timer 1 interrupt to high priority.
2	PX1, External Interrupt 1 Priority Control. PX1=0 sets external interrupt 1 (/INT1) to low priority. PX1=1 sets external interrupt 1 to high priority.
1	PT0, Timer 0 Interrupt Priority Control. PT0=0 sets Timer 0 interrupt (TF0) to low priority. PT0=1 sets Timer 0 interrupt to high priority.
0	PX0, External Interrupt 0 Priority Control. PX0=0 sets external interrupt 0 (/INT0) to low priority. PX0=1 sets external interrupt 0 to high priority.

4.2 Peripheral Device Registers

Bit	Description
7	TF1, Timer 1 Overflow Flag. Set to 1 when Time 1 count overflows and clears when the processor vectors to the interrupt service routine.
6	TR1, Timer 1 Run Control. Set to 1 to enable counting on Timer 1.
5	TF0, Timer 0 Overflow Flag. Set to 1 when Time 0 count overflows and clears when the processor vectors to the interrupt service routine.
4	TR0, Timer 0 Run Control. Set to 1 to enable counting on Timer 0.
3	IE1, Interrupt 1 Edge Detect. If external interrupt 1 is configured to be edge sensitive (IT1=1), IE1 is set by hardware when a negative edge is detected on the /INT1 and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1=0), IE1 is set when /INT1 is 0 and cleared when /INT1 is 1. In level-sensitive mode, software can not write to IE1.
2	IT1, Interrupt 1 Type Selector, /INT1 is detected on falling edge when IT1=1; /INT1 is detected as a low level when IT1=0.
1	IE0, Interrupt 0 Edge Detect. If external interrupt 0 is configured to be edge sensitive (IT0=1), IE0 is set by hardware when a negative edge is detected on the /INT0 and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In this case, IE0 can also be cleared by software. If external interrupt 0 is configured to be level-sensitive (IT0=0), IE0 is set when /INT0 is 0 and cleared when /INT0 is 1. In level-sensitive mode, software can not write to IE0.
0	IT0, Interrupt 0 Type Selector, /INT0 is detected on falling edge when IT0=1; /INT0 is detected as a low level when IT0=0.

SFR 89H : TMOD Register

Bit	Description
7	GATE. Timer 1 Gate Control, when GATE=1, Timer 1 will clock when /INT1 and TR1 (TCON.6)= 1. When GATE=0, Timer 1 will clock only when TR1=1, regardless of the state of /INT1
6	C/T, Counter/Timer Selector, when C/T=0, Timer 1 is clocked by clk/12, depending on the state of T1M (CKCON.4). When C/T=1, Timer 1 is clocked by T1 pin.
5-4	M1-0, Timer 1 mode select bits **M1 M0 Mode** 0 0 Mode 0: 13 bit counter 0 1 Mode 1: 16 bit counter 1 0 Mode 2: 8 bit counter with auto-reload 1 1 Mode 3: off
3	GATE. Timer 0 Gate Control, when GATE=1, Timer 0 will clock when /INT0 and TR0 (TCON.4)= 1. When GATE=0, Timer 0 will clock only when TR0=1, regardless of the state of /INT0.
2	C/T, Counter/Timer Selector, when C/T=0, Timer 0 is clocked by clk/12, depending on the state of T0M (CKCON.3). When C/T=1, Timer 0 is clocked by T0 pin.
1-0	M1-0, Timer 0 mode select bits **M1 M0 Mode** 0 0 Mode 0: 13 bit counter 0 1 Mode 1: 16 bit counter 1 0 Mode 2: 8 bit counter with auto-reload 1 1 Mode 3: Two 8 bit counter

Bit	Description
7	TF2, Timer 2 Overflow Flag. Hardware will set TF2 when the Timer 2 overflow from FFFFH, TF2 must be cleared to 0 by software. TF2 will only be set to 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
6	EXF2, Timer 2 External Flag. Hardware will set EXF2 when a reload or capture is caused by a high-to-low transition on the T2EX pin, and EXEN2 is set. EXF2 must be cleared to 0 by software. Writing a 1 to EXF2 forces a Timer 2 interrupt if enable.
5	RCLK, Receive Clock Flag. Determine whether Timer 1 or Timer 2 is used for Serial Port 0 timing of receive data in serial mode 1 or 3. RCLK=1 selects Timer 2 overflow as the receive clock. RCLK=0 selects Timer 1 overflow as the receive clock.
4	TCLK, Transmit Clock Flag. Determine whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. RCLK=1 selects Timer 2 overflow as the transmit clock. RCLK=0 selects Timer 1 overflow as the transmit clock.
3	EXEN2, Timer 2 External Enable. EXEN2=1 enables capture or reload to occur as a result of high-to-low transition on T2EX, if Timer 2 is not generating baud rates for the serial port. EXEN2=0 causes Timer 2 to ignore all external events at T2EX.
2	TR2, Timer 2 Run Control Flag. TR2=1 starts Timer 2, TR2=0 stops Timer 2.
1	C/T2 Counter/Timer Selector. C/T2=0 selects a timer function for Timer 2. C/T2=1 selects a counter of falling transitions on the T2 pin. When used as a timer, Timer 2 run at 4 clocks per tick or 12 clocks per tick as programmed by CKCON.5, in all modes except baud rate generator mode. When used in baud rate generator mode, Timer 2 runs at 2 clocks per tick, independent of state of CKCON.5
0	CP/RL2, Capture/Reload Flag. When CP/RL2=1, Timer 2 captures occur on high-to-low transitions of T2EX, if EXEN2=1. When CP/RL2=0, auto-reloads occur when Timer2 overflows or when high-to-low transitions occur on T2EX, if EXEN2=1. If either RCLK or TCLK is set to 1, CP/RL2 will not function and Timer 2 will operate in auto-reload mode following each overflow.

SFR 98H : SCON Register

Bit	Description
7-6	SM1,SM0, Serial Port 0 Mode Select bits **SM1 SM0 Mode** 0 0 0 0 1 1 1 0 2 1 1 3
5	SM2, Multiprocessor Communication Enable. In modes 2 and 3, this bit enables the multiprocessor communication feature. If SM2=1 in mode 2 or 3, the RI will not be activated if the received 9th bit is 0. If SM2=1 is in mode 1, then RI will only be activated if a valid stop is received. In mode 0, SM2 establishes the baud rate: when SM2=0, the baud rate is clk/12; when SM2=1, the baud rate is clk/4.
4	REN, Receive Enable. When REN=1, reception is enabled.
3	TB8, Defined the state of the 9th data bit transmitted in modes 2 and 3.
2	RB8, In modes 2 and 3, RB8 indicates the state of the 9th bit received. In mode 1, RB8 indicates the state of received stop bit. In mode 0, RB8 is not used.
1	TI, Transmit Interrupt Flag. Indicates that the transmit data word has been shifted out. In mode 0, TI is set at the end of the 8th data bit. In all other modes, TI is set when the stop bit is placed on the TXD pin, TI must be cleared by software.
0	RI, Receive Interrupt Flag. Indicates that serial data word has been received. In mode 0, RI is set at the end of the 8th data bit. In mode 1, RI is set after the last sample of the incoming stop bit, subject to the state of SM2. In modes 2 and 3, RI is set at the end of the last sample of RB8, RI must be cleared by the software.

Section 5 : Peripheral Device

The M6759 has three 16-bit timer/counter registers, all three can be configured to operate either as timers or event counters.

oscillator periods. Thus, one can view the register as a counter with count rate 1/12 of oscillator frequency.

When operating as counter function, the register increases according to a 1-to-0 transition at corresponding external input

In this function, the external input pin is sampled at every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the counter increases by 1. Since it takes two machine cycles to determine a transition, the count

machine cycle to ensure the given level to be sampled.

In addition to the timer/counter selection, Timer 0 and Timer 1 have four operating modes, Timer 2 has three operating

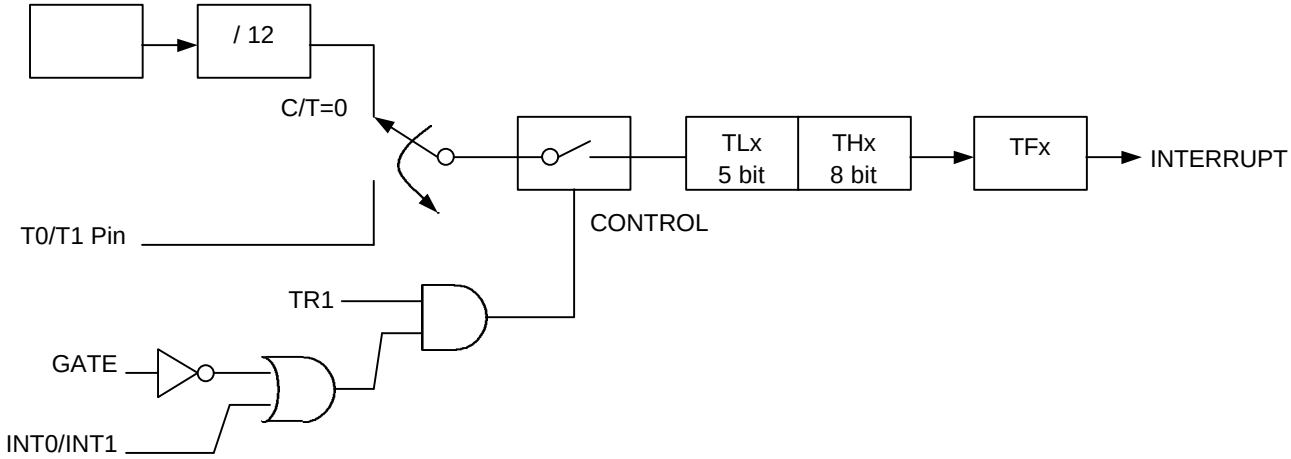
Timer0/Timer1 Mode Control

M1		Operating Mode
0		8 bit Timer/Counter, "THx" with "TLx" as 5 bit prescaler
0		16 bit Timer/Counter, "THx" and "TLx" are cascadent
1		8 bit auto-reload timer/counter, each time "TLx" overflows, store value in "THx" into "TLx".
	1	Timer 0 : TL0 and TH0 indicate two 8-bit counters controlled by Timer 1 : off

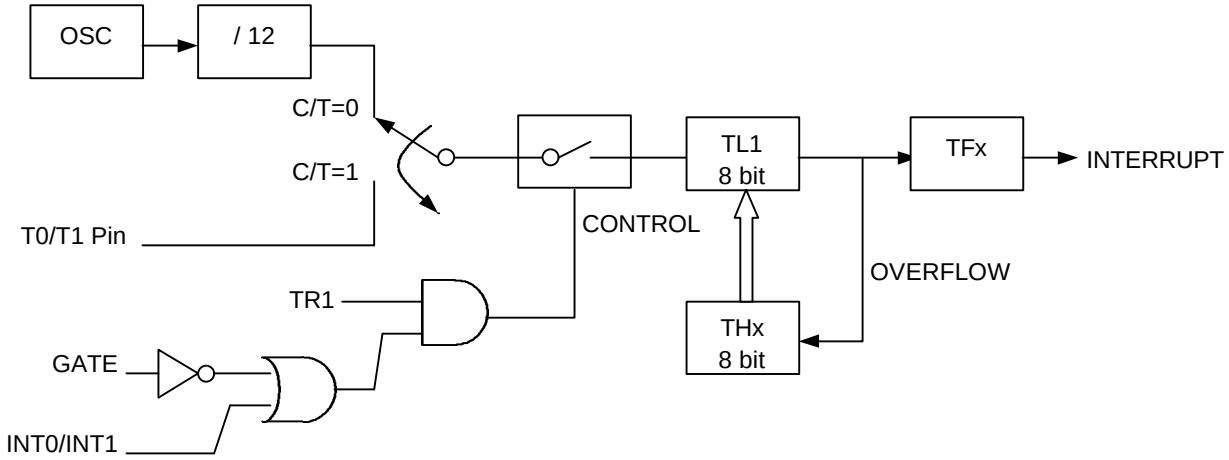
Timer2 Mode Control

	CP/RL2	**TR2**	
0	0		16-bit auto-reload
0		1	16-bit capture
	X	1	
X	X		Non-active

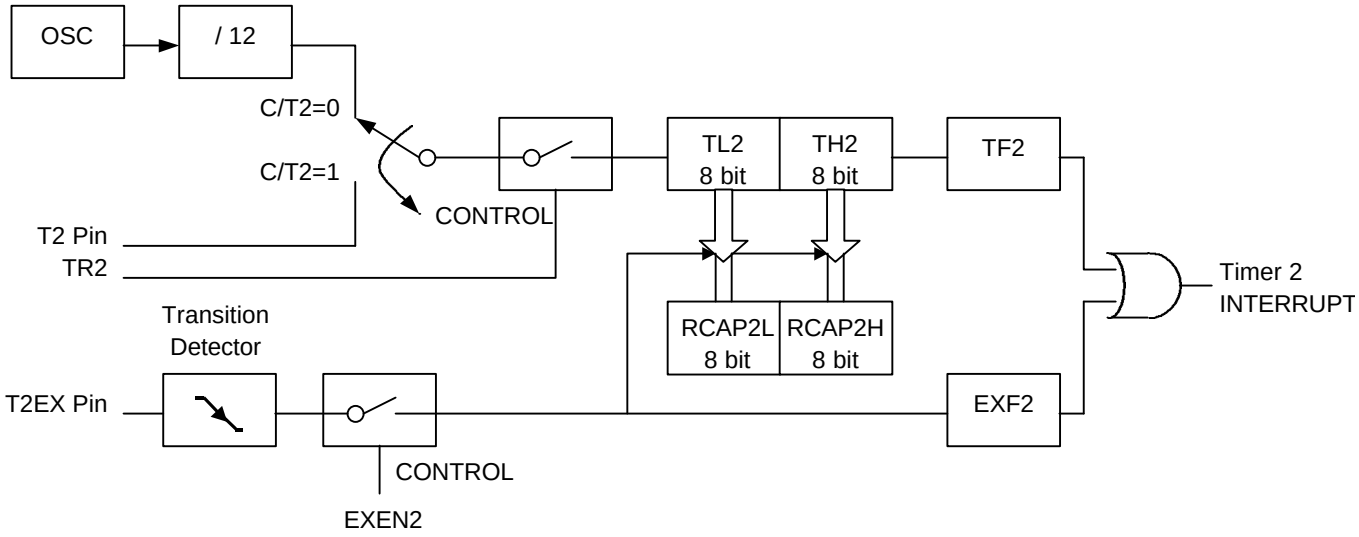
Timer/Counter Mode 0 : 13 bit Counter



Timer/Counter Mode 2 : 8-bit Auto-Reload



Timer 2 in Capture Mode



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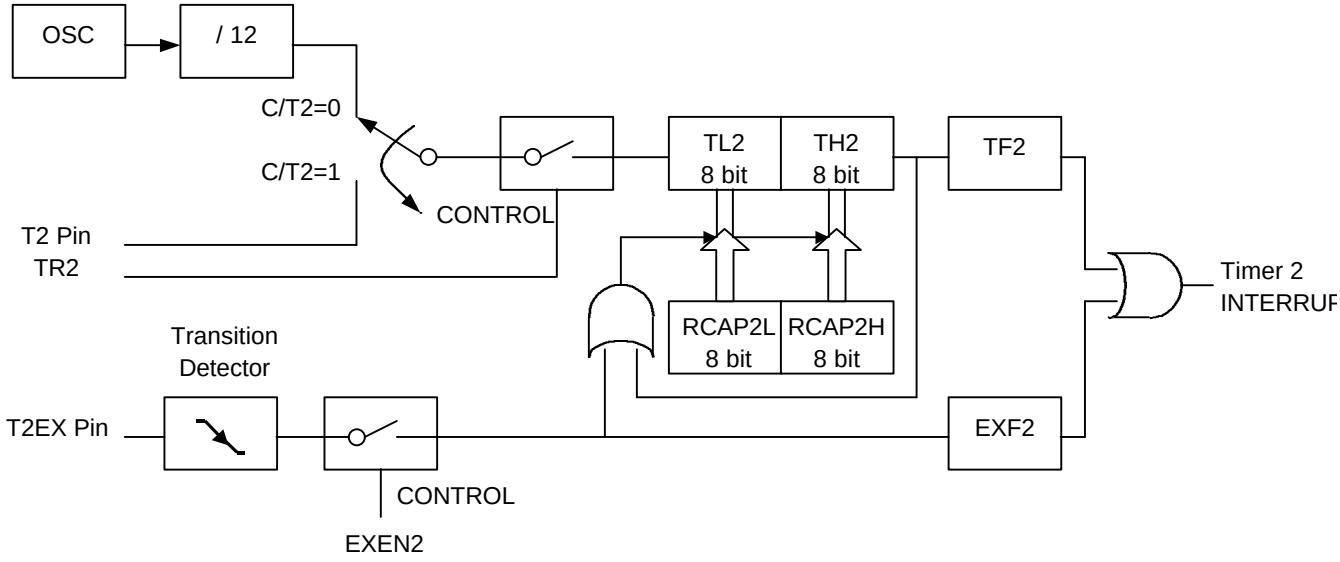
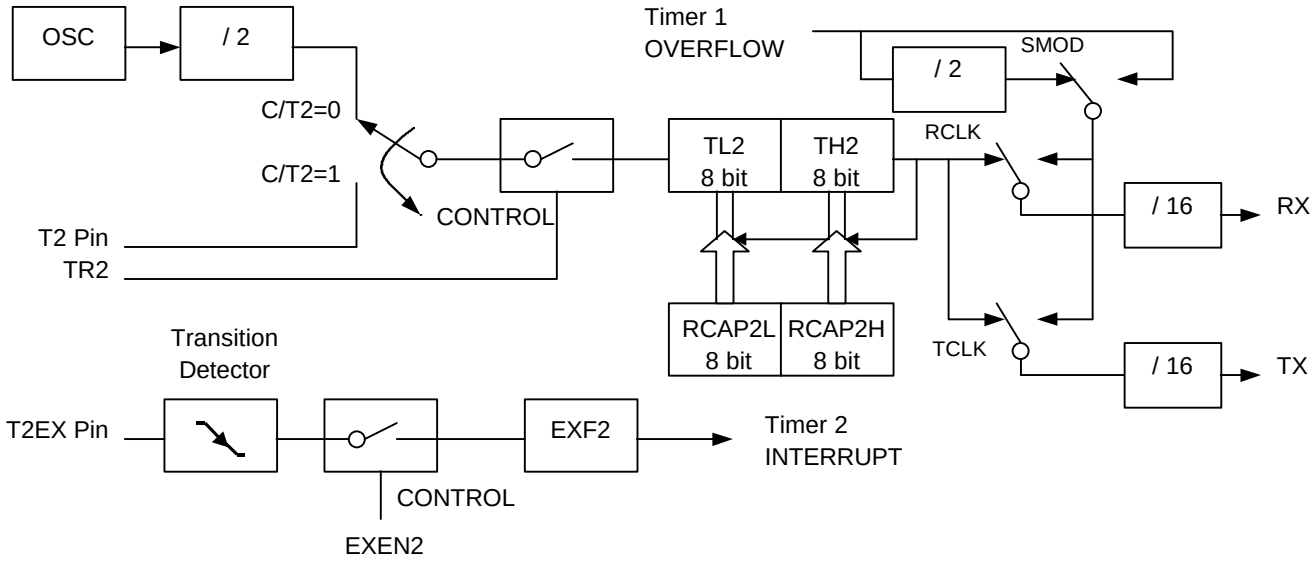
Timer 2 in Auto-reload Mode



Timer 2 In Baud Rate Generator Mode



Timer 2 is a 16-bit Timer/Counter. It can be selected as a timer or an event counter by register T2CON. It has three operating modes: "Capture", "Auto-reload" and "Baud rate generator".

In capture mode, there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 is 0, then Timer2 is a 16-bit timer/counter which sets bit TF2 (timer 2 overflow flag) upon overflowing, TF2 can generate an interrupt when Timer 2 interrupt is enabled. If EXEN2 is 1, above operation is still activated, with added feature that a 1-to-0 transition of external input pin T2EX can cause the content of TL2 and TH2 to be captured into RCAP2L and RCAP2H. In addition, the transition of T2EX set the bit EXF2 (which is in the T2CON register), and EXF2 can generate an interrupt.

In Auto-reload mode, there are two options that can be selected by bit EXEN2 in T2CON. If EXEN2 is 0, when Timer 2 overflows it sets TF2 and Timer 2 load the 16 bits values stored in RCAP2L and RCAP2H. If EXEN2 is 1, Timer2 still does the above, bit with an added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

5.2 Serial Interface

The serial port is full duplex, which means it can transmit and receive data simultaneously. There is a receive buffer to commence reception second byte before previously received byte has been read from the receive register. (If the first byte has not been completely read by the time reception of the second byte, one of the bytes will still be lost). The serial port receive and transmit data are both accessed at SBUF. Writing to SBUF loads the transmit register. Read SBUF accesses a physically separate receive register.

Baud Rates

The Mode 0 Baud rate is fixed:

$$Mode0\ Baud\ Rate = \frac{Oscillator\ Frequency}{12}$$

Baud rate in Mode 2 depends on the bit of SMOD in Special Function Register PCON. If SMOD is 0, baud rate is 1/64 of the oscillator frequency; if SMOD is 1, baud rate is 1/32 of the oscillator frequency.

$$Mode2\ Baud\ Rate = \frac{2^{SMOD} \times (Oscillator\ Frequency)}{64}$$

The Baud rate in Mode 1 and Mode 3 can be determined by overflow rate of Timer 1, Timer 2 or both (one for transmit and other for receive).

When Timer 1 is used to generate Baud rate, it is determined by following equation:

$$Baud\ Rate = \frac{2^{SMOD}}{32} \times (Timer1\ Overflow\ Rate)$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either timer or counter in any of its three running modes.

In the Auto-reload mode (high nibble of TMOD = 0010B), the baud rate is given by:

$$Mode(1,3)\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{Oscillator\ Frequency}{12 \times (256 - TH1)}$$

When Timer 2 is used to generate Baud rate, it is set by TCLK and/or RCLK in T2CON, and the baud rate for transmit and receive can be different.

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The baud rate generator mode is similar to the auto reload mode. A rollover in TH2 cause Timer 2 to be reload with 16 bit value which stored in RCAP2H and RCAP2L.

$$Mode(1,3)\ Baud\ Rate = \frac{Timer2\ Overflow\ Rate}{16}$$

The Timer can be configured for either "timer" or "counter" operation. Normally, as a timer it increments every machine cycle (12 oscillator cycles), as a baud rate generator it increments every state time (2 oscillator cycles). In that case baud rate is give by the following formula:

$$Mode(1,3)\ Baud\ Rate = \frac{Oscillator\ Frequency}{32\times[65536-(RCAP2H, RCAP2L)]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and PCAP2L taken as a 16 bit unsigned integer which is preset by software.

Timer 2 in baud rate generator mode is valid only if RCLK or TCLK in T2CON is 1. The rollover in TH2 does not set TF2, and will not generate interrupt Also note that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L). In this case, T2EX can be used as an extra external interrupt if desire.

Timer 1 Reload Values Common Serial Port Mode 1 Baud Rates

Desired Baud Rate	SMOD	C/T	Timer 1 Mode	TH1 Value for 33 MHz clock	TH1 Value for 25 MHz clock	TH1 Value for 11.0592 MHz clock
57.6 Kb/s	1	0	2	FDH	FEH	FFH
19.2 Kb/s	1	0	2	F7H	F9H	FDH
9.6 Kb/s	1	0	2	EEH	F2H	FAH
4.8 Kb/s	1	0	2	DCH	E5H	F4H
2.4 Kb/s	1	0	2	B8H	CAH	E8H
1.2 Kb/s	1	0	2	71H	93H	D0H

Timer 2 Reload Values Common Serial Port Mode 1 Baud Rates

Desired Baud Rate	C/T2	33 MHz clock		25 MHz clock		11.0592 MHz clock	
		RCAP2H	RCAP2L	RCAP2H	RCAP2L	RCAP2H	RCAP2L
57.6 Kb/s	0	FFH	EEH	FFH	F2H	FFH	FAH
19.2 Kb/s	0	FFH	CAH	FFH	D7H	FFH	EEH
9.6 Kb/s	0	FFH	95H	FFH	AFH	FFH	DCH
4.8 Kb/s	0	FFH	29H	FFH	5DH	FFH	B8H
2.4 Kb/s	0	FEH	52H	FEH	BBH	FFH	70H
1.2 Kb/s	0	FCH	A5H	FDH	75H	FEH	E0H

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Section 6 : Electrical Specifications

6.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics. Unless otherwise specified, all voltages are reference to ground.

Table 6-1 Absolute Maximum Ratings

Item	Ratings
Supply voltage Operating supply voltage (VCC) Operating supply voltage (VDD)	-0.5V to +7V 4.5V to 5.5V 3.0V to 3.6V
All input and output voltages	-0.5V to VCC+0.5V
Storage temperature range (T_{STG})	-60 °C to 150 °C
Operating temperature (T_A)	0°C to 70 °C

6.2 D.C. Characteristics

SYMBOL	PARAMETERS	MIN	MAX	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.4	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.5	V	I_{OL}=4.0 mA
V_{OH}	Output High Voltage	4.0	-	V	I_{OH}= -4.0mA
I_{CC}	Power Supply Current (Active mode)	-	30	mA	VDD=5V, Frequency=10MHz

6.3 AC Characteristics

SYMBOL	PARAMETERS	MIN	MAX	Unit
t_{CLCL}	Oscillator Clock Cycle Period	25	-	ns
1 / t_{CLCL}	Oscillator Frequency	0	40	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL} - 40$	-	ns
t_{HAVL}	High bytes Address Valid to ALE Low	$2t_{CLCL} - 55$	-	ns
t_{AVLL}	Address Valid to ALE Low	$t_{CLCL} - 55$	-	ns
t_{LLAX}	Address Hold After ALE Low	$t_{CLCL} - 35$	-	ns
t_{LLIV}	Address Low to Valid Instruction In	-	$4t_{CLCL} - 100$	ns
t_{LLPL}	ALE Low to /PSEN Low	$t_{CLCL} - 40$	-	ns
t_{PLPH}	PSEN Pulse Width	$3t_{CLCL} - 45$	-	ns
t_{PLIV}	/PSEN Low to Valid Instruction In	-	$3t_{CLCL} - 105$	ns
t_{PXIX}	Input Instruction Hold After /PSEN	0	-	ns
t_{PXIZ}	/PSEN to Address Valid	-	t_{CLCL} - 25	ns
t_{AVIV}	Address to Valid Instruction In	-	$5t_{CLCL}$ - 105	ns
t_{RLRH}	/RD Pulse Width	$6t_{CLCL} - 100$	-	ns
t_{WLWH}	/WR Pulse Width	$6t_{CLCL} - 100$	-	ns
t_{RLDV}	/RD Low to Valid Data In	-	$5t_{CLCL} - 165$	ns
t_{RHDX}	Data Hold After /RD	0	-	ns
t_{LLDV}	ALE Low to Data Valid In	-	$8t_{CLCL} - 150$	ns
t_{AVDV}	Address to Valid Data In	-	$9t_{CLCL} - 165$	ns
t_{LLWL}	ALE Low to /RD or /WR Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to /RD or /WR Low	$4t_{CLCL} - 130$	-	ns
t_{QVWX}	Data Valid to /WR Transition	$t_{CLCL} - 60$	-	ns
t_{QVWH}	Data Valid to /WR High	$7t_{CLCL} - 150$	-	ns
t_{WHQX}	Data Hold After /WR	$t_{CLCL} - 50$	-	ns
t_{WHLH}	/RD or /WR high to ALE High	-	t_{CLCL} + 40	ns

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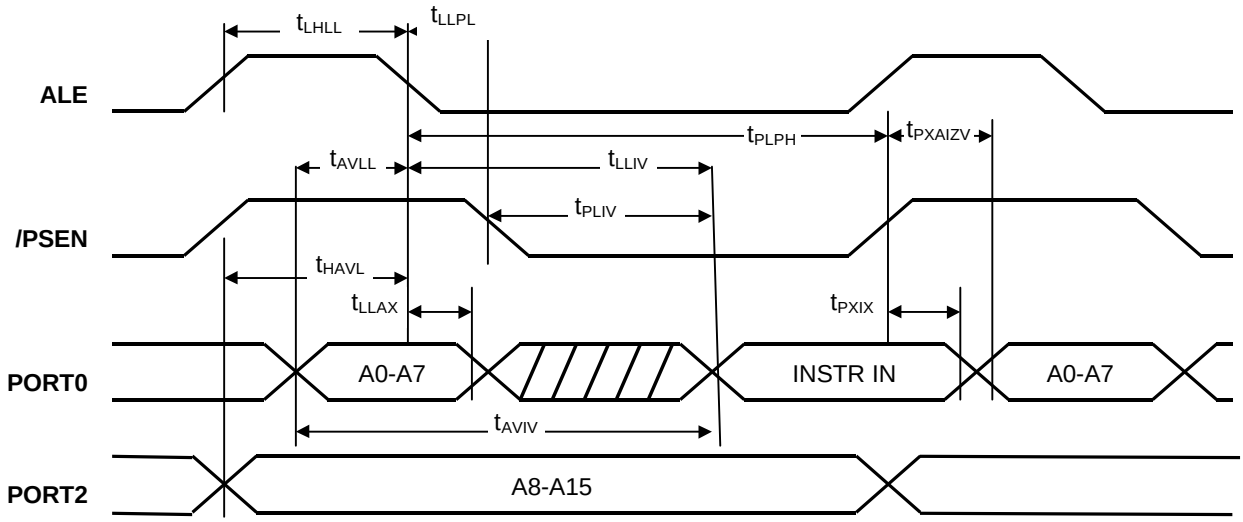
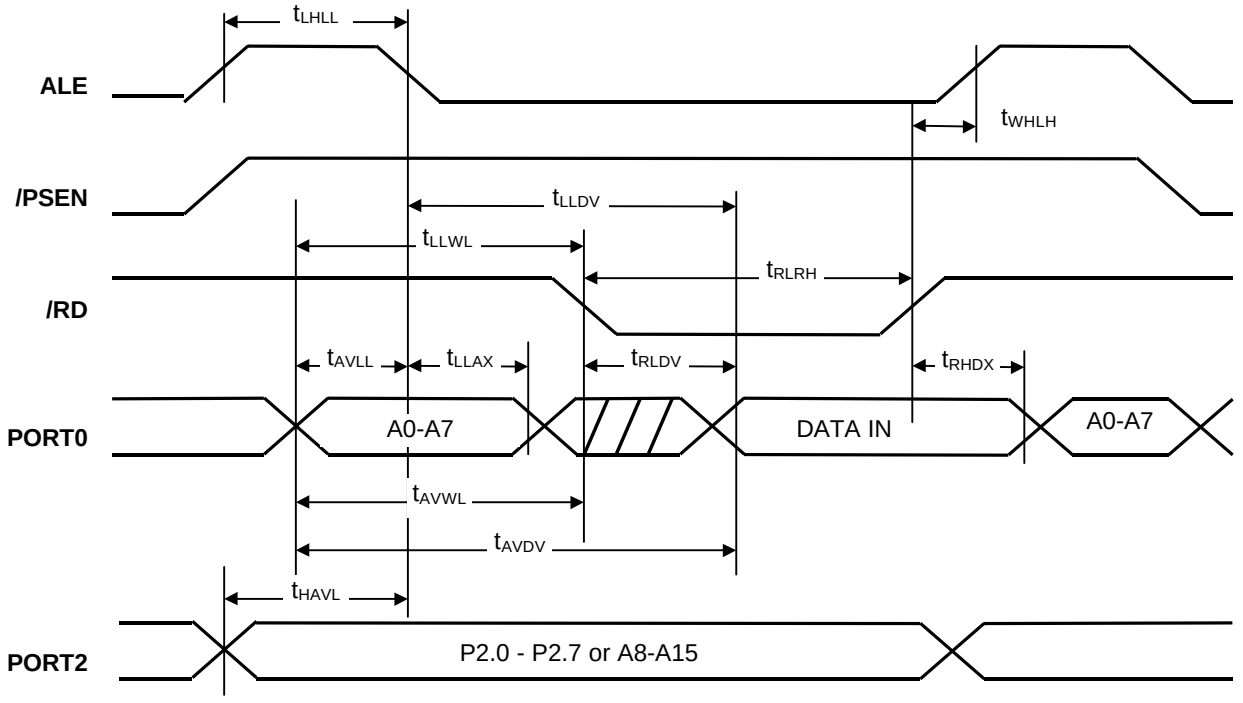
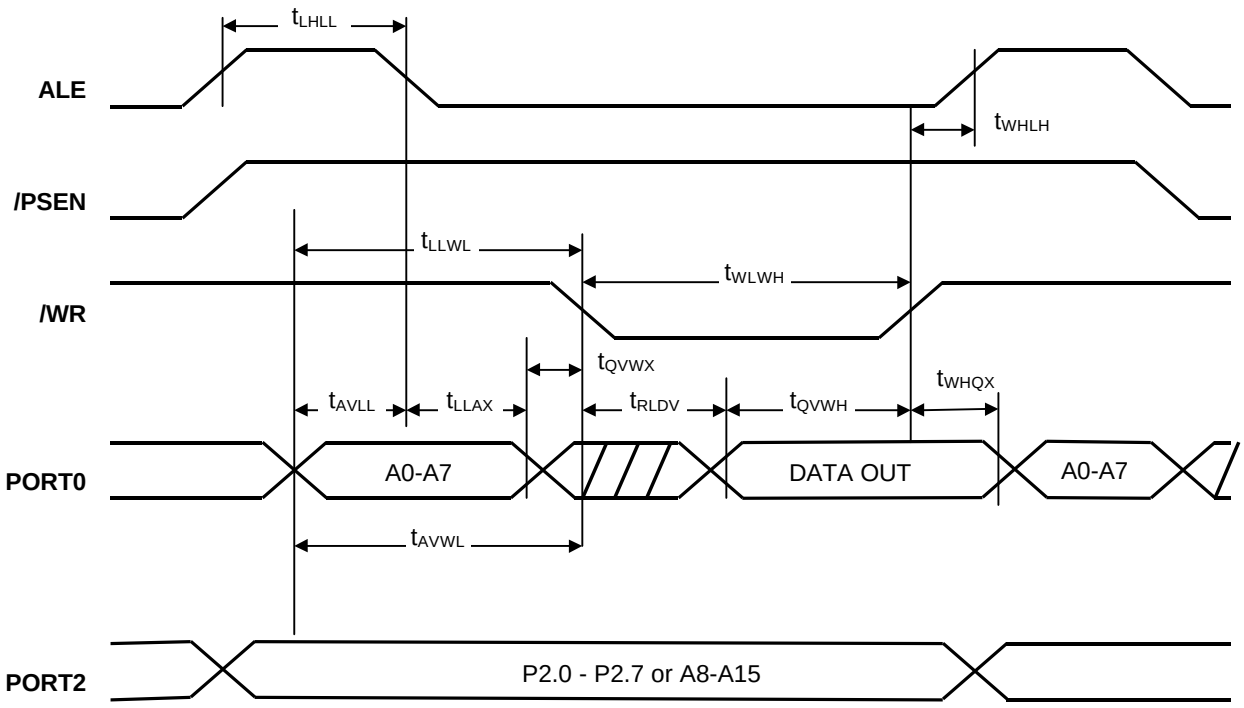
External Program Memory Read Cycle



External Data Memory Read Cycle



External Data Memory Write Cycle



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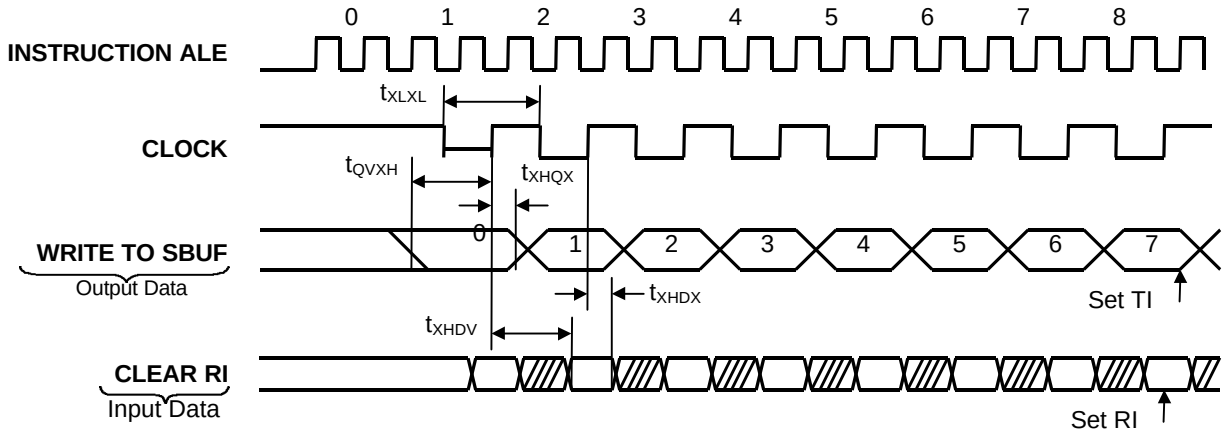
Serial Port Timing : Shift Register Mode Test Conditions

SYMBOL	PARAMETER	MIN	MAX	Unit
t_{XLXL}	Serial Port Clock Cycle Time	$12\ t_{CLCL}$	-	ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	$9t_{CLCL} - 100$	-	ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	$3t_{CLCL} - 100$	-	ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0	-	ns
t_{XHDV}	Clock Rising Edge to Input Data Valid	-	$10t_{CLCL} - 133$	ns

Shift Register Mode Timing Diagram



Section 7 : Flash Programming Guide

Features

- **64 Kbytes electrically erasable internal program memory**
- **Encrypted verifiable**
- **3-level program memory lock**
- **100 program/erase cycles**
- **Fully synchronous operation**
- **High performance CMOS – 100ns read access time**
- **12v external programming voltage**

7.1 Description

The flash module is completely synchronous. All the operations are synchronized to the rising edge of the clock (XTAL1 pin). On the rising edge of the XTAL1, the pins' status is sampled and latched. For writing internal registers operations, the latched information is decoded during the XTAL1 high period, and execution is carried out on the falling XTAL1 edge. The flash module executes commands using an eight bit Instruction Register (IR), that defines the operation to be executed. Using the IR enables reading, programming and erasing main array and OTPR. The IR command is defined as the following table.

Table 7-1. IR Command Definition

Command	Code
Read Array	00h
Read OTPR (Key bytes or lock bits)	08h
Erase Array	80h
Erase OTPR (Key bytes or lock bits)	88h
Program Array	40h
Program OTPR (Key bytes or lock bits)	48h

There are two modules in the flash –main array and OTPR.

Main Array

The module's main array contains 64K bytes of memory that serve as the code storage space for program code. The array occupies address space from 0000H to FFFFH.

OTP Rows
These non-volatile cells contain 2K bytes of memory that serve as a special storage space for protection data (i.e. key bytes and lock bits).

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Note : Pin assignments shown below are listed based on 44-pin PLCC package. As for QFP package, the pin number assignment should be shifted accordingly, as comparatively shown in Section 2.1 Pinout Diagram.

Pin No. (PLCC)	Pin Name	Signal Name	Type	Description
44	VDD		IN	Power supply for internal operation, 5V input
22	GND		IN	Ground
35	/EA	Vpp	IN	Always hold 12V during erase, programming and read flash module
10, 33, 18	RST, ALE, P3.6	High	IN	Always hold high during erase, programming and read flash module
13, 14, 32	P3.1, P3.2, /PSEN	Low	IN	Always hold low during erase, programming and read flash module
31, 30, 29, 28, 27, 26, 25, 24	P2.7 to P2.0	A15 to A8	IN	Input high-order address bits
9, 8, 7, 6, 5, 4, 3, 2	P1.7 to P1.0	A7 to A0	IN	Input low-order address bits
36, 37, 38, 39, 40, 41, 42, 43	P0.7 to P0.0	D7 to D0	IN/OUT	Command/Data bus
11	P3.0	/RESET	IN	Flash reset
15	P3.3	IR_EN	IN	Instruction register access enable
16	P3.4	RDY	OUT	Ready signal
17	P3.5	/OE	IN	Output enable
19	P3.7	RD/WR_b	IN	Read/write selection

Program Lock Bits

The M6759 has 3 programmable lock bits that when programmed according to Table 7-2 will provide different levels of protection for the on-chip code and data. The lock bits are in the bit 4, bit 5 and bit 6 of OTPR address 0004. Refer to Figure 7-1 - OTPR arrangement.

Table 7-2. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	1	1	1	No Program Lock features enabled. (Code verify will be encrypted by the Encryption Array if programmed.)
2	0	1	1	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the flash is disabled.
3	0	0	1	Same as 2, also verify is disabled.
4	0	0	0	Same as 3, also external execution is disabled.

Encryption Array (key bytes)

There are 4 bytes of encryption array that are initially unprogrammed (all 1s). Every time that a byte is addressed during verify, 2 address lines are used to select a byte of the encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an encryption verify byte. The key bytes are in the address 0000, 0001, 0002 and 0003 of OTPR space.

The encryption function is available only when LB1 is programmed.

Status Bits

There are two status bits to constrain protection function in M6759. After whole chip is erased (include array and OTPR), ST0 must be programmed to 0. After key bytes and lock bits are programmed, ST1 must be programmed to 0. The status bits are in the bit1 and bit 0 of OTPR address 0004.

Status bits	Program Condition
ST0	The bit needs to be programmed after erased.
ST1	The bit needs to be programmed after protection function bytes (lock bits, key bytes) is programmed

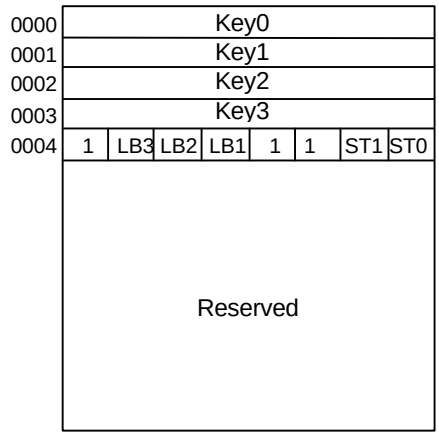

Figure 7-1. OTPR Arrangement Map

Programming

This mode enables the user to program the main memory and verify its contents. It also allows programming the OTPR. The cells to be programmed are defined by the IR command. In order to program, the required address is applied to the address bus, the required data byte is applied to the data bus and an IR program/verify instruction is executed. /OE signal must be set to high in order to avoid bus contention. This mode is operated through the Instruction Register, and requires the IR to be loaded prior to execution. Several programming pulses may be required to program a cell. Note that in order to succeed in programming, a byte must be fully erased prior to programming it. Erased byte holds the value of FFh. A written bit holds a value of zero. When programming is started. The RDY signal becomes low and remains low until the programming is over. During the period in which RDY signal is low, the module logic inputs are not sampled. The clock signal must be kept during RDY pin low period to ensure RDY is synchronized with the clock signal. Verify operation should be done following each byte programming. It is a read operation with built in margins performed using the IR (RD/WR_b is high). If the verify fails, an additional programming cycle must be applied to the same address. Programming failure to a specific address is defined as 30 consecutive attempts to program the same address without a successful verify.

Erasing

This mode enables the user to erase the array and the OTPR. The cells to be erased are defined by the IR command. The command is executed upon the rising edge of the XTAL1, following writing the erase command into the IR. During erase, /OE signal must be high to avoid bus contention. The RDY signal becomes low and remains low until the erase operation is over. During the period in which RDY signal is low, the module logic inputs are not sampled. The clock signal must be kept during RDY pin low period to ensure RDY is synchronized with the clock signal. Verify procedure is a read operation with built in margins, required to confirm that all the word were successfully erased. To perform verify the user must revert the RD/WR_b state to high, and apply an address to the address bus. Verify is carried out on the following rising edge of the XTAL1 signal. All addresses have to be applied sequentially in order to verify the entire array. During verify, /OE must be low to enable reading the erased cells. An erased cell has a value of ' 1', thus an erased byte contains FFh.

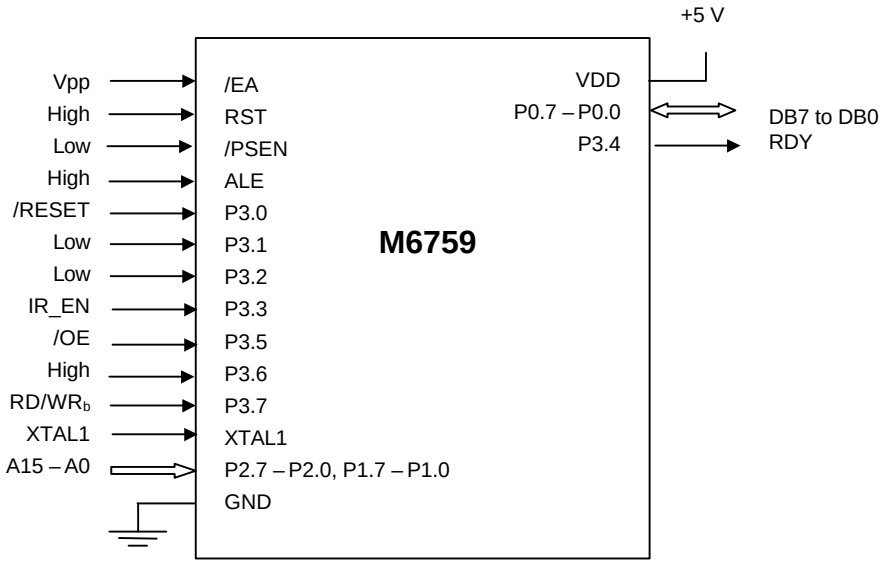

Fig.7-2. Flash Programming Configuration

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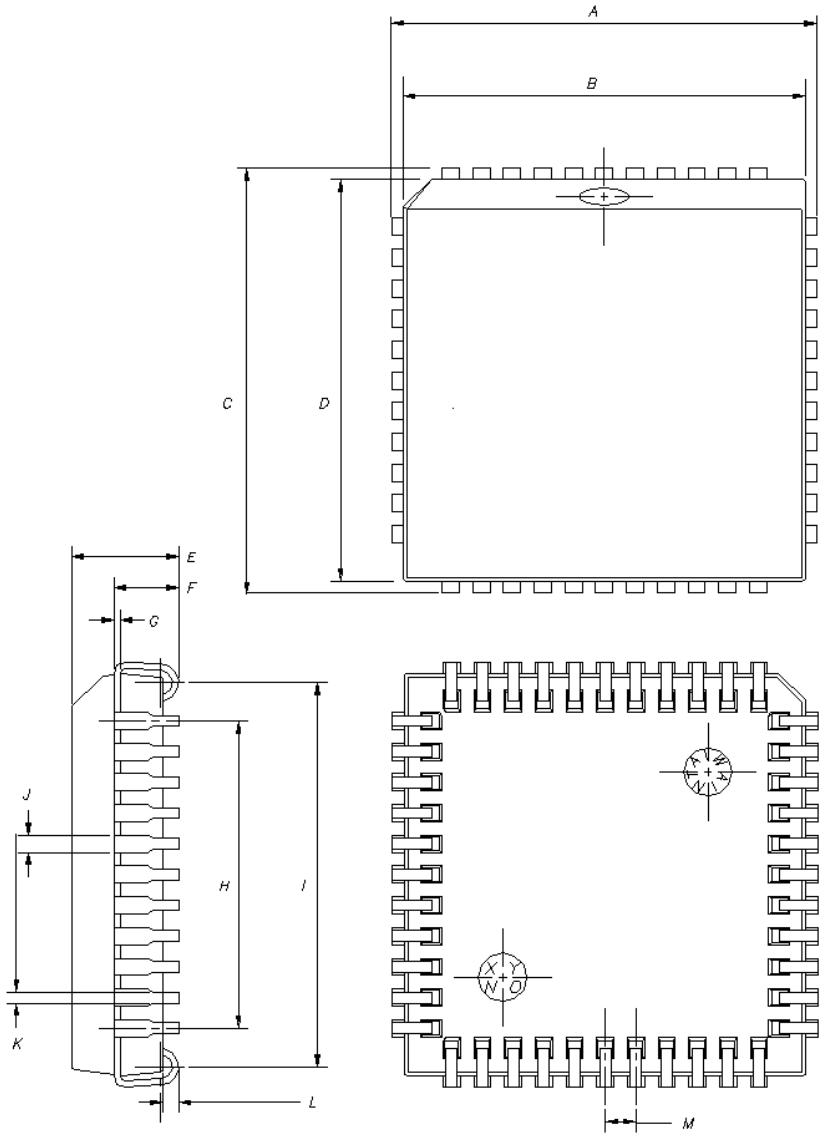
Section 8 : Packaging Information

44-pin PLCC Package



SYMBOL	Dimension in Inches			SYMBOL	Dimension in Inches		
	Min	Typ	Max		Min	Typ	Max
A	0.685	0.690	0.695	H	-	0.5	-
B	0.650	0.653	0.656	I	0.595	0.610	0.625
C	0.685	0.690	0.695	J	0.026	-	0.032
D	0.650	0.653	0.656	K	0.013	-	0.021
E	0.168	0.174	0.180	L	0.02	-	0.04
F	0.102	0.105	0.108	M	0.045	0.05	0.055
G	-	0.010	-				

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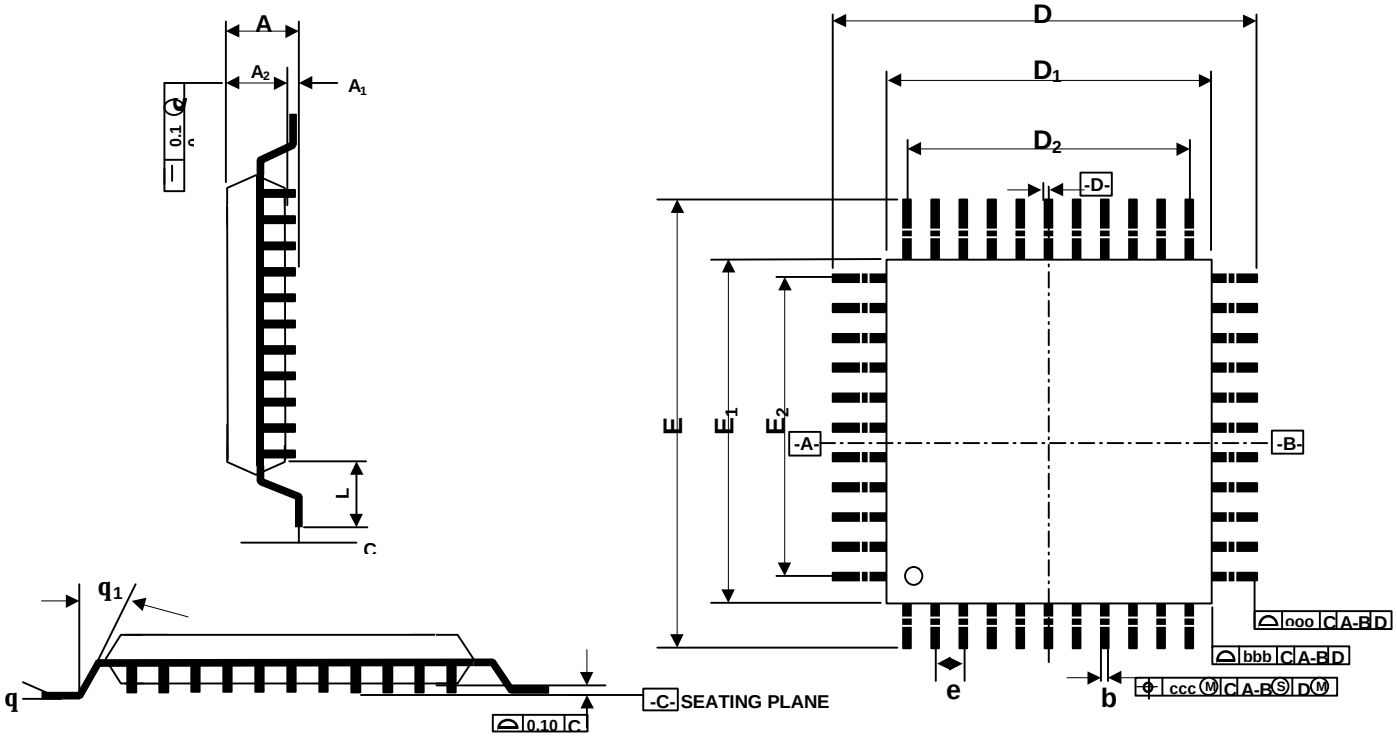
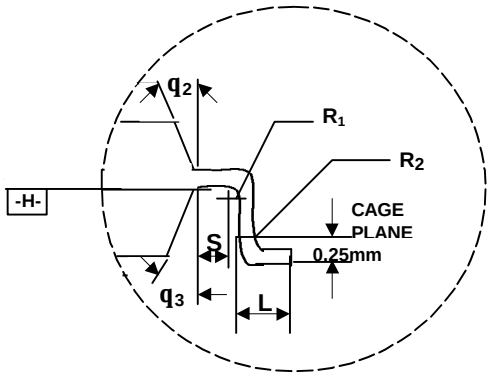
44-pin QFP Package



CONTROL DIMENSIONS ARE IN MILLIMETERS

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.55	-	-	0.100
A_1	0.15	0.25	0.35	0.006	0.010	0.014
A_2	1.90	2.05	2.20	0.075	0.081	0.087
D	13.20 BASIC			0.520 BASIC		
D_1	10.00 BASIC			0.394 BASIC		
E	13.20 BASIC			0.520 BASIC		
E_1	10.00 BASIC			0.394 BASIC		
R_2	0.13	-	0.30	0.005	-	0.012
R_1	0.13	-	-	0.005	-	-
θ	0°	-	7°	0°	-	7°
θ_1	0°	-	-	0°	-	-
θ_2	10° REF			10° REF		
θ_3	7° REF			7° REF		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
S	0.20	-	-	0.008	-	-



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	8.0			0.315		
E2	8.0			0.315		
ooo	0.25			0.010		
bbb	0.20			0.008		
ccc	-	0.20	-	-	0.008	-

NOTES : 1, DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE (-H-). 2, DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL. IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

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