CMOS single-chip 8-bit MCU with LCD Driver

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 8Kbytes Flash Code Memory
  - 256bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16 MHz RC oscillator (±1.5%,T_A= 0°C ~ +50 °C)
  - Watchdog Timer RC oscillator (5kHz)
- **Peripheral Features**
  - UART, SIO
  - LCD Driver (24Segment x 8Common)
- **I/O and Packages**
  - Up to 49 Programmable I/O lines with 52-PELLET
  - 52-PELLET, 48LQFP, 48TQFP
- **Operating Conditions**
  - 1.8 V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - LCD Remote Control Unit

MC96F6508A
MC96F6408A

User's manual

V 1.8

Revised 11 May, 2017

Revision history

Version	Date	Revision list
0.0	2012.12.28	Published this book.
1.0	2013.05.23	Revised this book. Change “1.3/2.6mA (Typ/Max)” to “IDD2@12MHz x-tal” in DC electrical characteristics. Change “0.7/1.4mA (Typ/Max)”to “IDD2@10MHz x-tal” in DC electrical characteristics. Change “0.8/1.6mA (Typ/Max)” to “IDD2@IRC16MHz” in DC electrical characteristics. Change “100,000” to “10,000” in Flash endurance Add contents, “Writing “1” has no effect” in all interrupt flag bits.
1.1	2013.07.15	Add a Programmer Type “PGMplusLC Writer”. Fixed a typo.
1.2	2013.12.02	Remove contents about “byte erase” in Flash Memory.
1.3	2014.07.09	Change “Read Protection” to “Code Read Protection” in Configure Option. Change “Hard-Lock” to “Code Write Protection” in Configure Option. Change “Vector Area Protection” to “Vector Area Write Protection” in Configure Option. Change “RESETB select” to “Select RESETB pin” in Configure Option. Change “Protection Area” to “Specific Area Write Protection” in Configure Option. Add note of “Specific Area Write Protection” in Configure Option, “When PAEN = ‘1’, it is applied.” Fix the byte count of instruction “DJNZ Rn,rel”. Remove a Programmer Type “PGMplusLC Writer”. Fix the typo.
1.4	2014.09.02	Add a note in “P0DB Register.”
1.5	2015.04.13	Change a Figure 10.3 Interrupt sequence flow. Add contents of Flash, “Protection for Invalid Erase/Write”.
1.6	2016.04.06	Change Tolerance spec max value from ±4% to ±1% in 7.5 Phase Locked Loop Characteristics. Add Flash Data Retention Time in Chapter 7.14 Internal Flash Rom Characteristics Add a chapter 7.22 Recommended Circuit and Layout with SMPS Power. Modify the program tips in Chapter 15. Flash Memory. Add an appendix about “Flash Protection for invalid Erase/Write” Fixed typos.
1.7	2017.02.01	Added the note on the flash memory erase and write in Chapter 15. Flash Memory. Updated OCD dongle image and writing tool images in Chapter 1.3 Development tools.
1.8	2017.05.11	Revised this book. Add 48TQFP(MC96F6408ATBN) package type. Updated 48LQFP package diagram in Chapter 4. Package Diagram. Change Device name of 52-PELLET from MC96F6508A to MC96F6508AC.

Version 1.8

Published by FAE team

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1 Overview

1.1 Description

The MC96F6508A and MC96F6408A are an advanced CMOS 8-bit microcontroller with 8Kbytes of FLASH memory. Theseare powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. These provide the following features : 8Kbytes of FLASH, 256bytes of IRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timercounter, carrier generation, watch timer, buzzer driving port, SIO, UART, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry.

Device Name	FLASH	IRAM	I/O PORT	Package
MC96F6508AC	8Kbytes	256bytes	49	52-PELLET
MC96F6408AL			45	48LQFP
MC96F6408ATBN			45	48TQFP

Table 1-1. Ordering Information of MC96F6508A

1.2 Feature

- **CPU**
  - 8-bit CISC Core(M8051, 2clocks per cycle)
- **ROM (FLASH) Capacity**
  - 8Kbytes
  - Flash with self-read/write capability
  - On chip debug and In-system programming (ISP)
  - Endurance : 10,000 times
  - Retention : 10 years
- **256bytes IRAM**
  - (30bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 17 Ports (P0[3:0], P1[7:0], P6[4:0])
  - LCD shared I/O : 32 Ports (P2[7:0], P3[7:0], P4[7:0], P5[7:0])
- **Basic Interval Timer (BIT)**
  - 8-bit× 1-ch
- **Watch Dog Timer (WDT)**
  - 8-bit× 1-ch
  - 5kHz internal RC oscillator
- **Timer/ Counter**
  - 8-bit× 4-ch(T0/T1/T2/T3), 16-bitx 2-ch (T0/T2)
- **Carrier Generation**
  - Carrier Generation (by T1), T2 Clock source
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s interval at 32.768kHz
- **Buzzer**
  - 8-bit× 1-ch
- **SIO**
  - 8-bit× 1-ch
- **UART**
  - 8-bit× 1-ch
- **LCD Driver**
  - 24Segments and 8Common terminals
  - 60kΩ and 120kΩ internal dividing resistor selectable
  - 1/2, 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable
  - 1/2, 1/3, and 1/4 bias selectable
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60V/ 2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
- **Low Voltage Indicator**
  - 13 level detect (2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
- **Interrupt Sources**
  - External Interrupts (EINT10, EINT12) (2)
  - Key Interrupts (8)
  - Timer (0/1/2/3) (4)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SIO (1)
  - UART(Tx/Rx) (2)
- **Internal RC Oscillator**
  - Internal RC frequency: 16MHz ± 1.5% (T_A= 0°C ~ +50°C, V_{DD}=2.0V ~ 5.5V)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@ 32 ~ 38kHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal)
  - 2.7V ~ 5.5V (@ 0.4 ~ 12.0MHzwith X-tal)
  - 2.0V ~ 5.5V (@ 0.5 ~ 16.0MHz with internal RC)
  - 2.0V ~ 5.5V (@ 1.0 ~ 16.4MHz with PLL)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 122ns at 16.4MHz CPU clock
- **Operating Temperature:** –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
  - Phase Locked Loop (Max. 16.4MHz with sub clock)
- **Package Type**
  - 52-PELLET
  - 48 LQFP-0707
  - 48 TQFP-0707

1.3 Development Tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F6508Ais Mentor 8051. And,device ROM size is smaller than 8Kbytes.Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system.The OCD can read or change the value of MCU internal memory and I/O peripherals.And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual.You can download debugger program and manual from ABOV web-site.

Connection:

- DSCL (MC96F6508AP16 port)
- DSDA (MC96F6508AP17 port)

OCD connector diagram: Connect OCD with user system

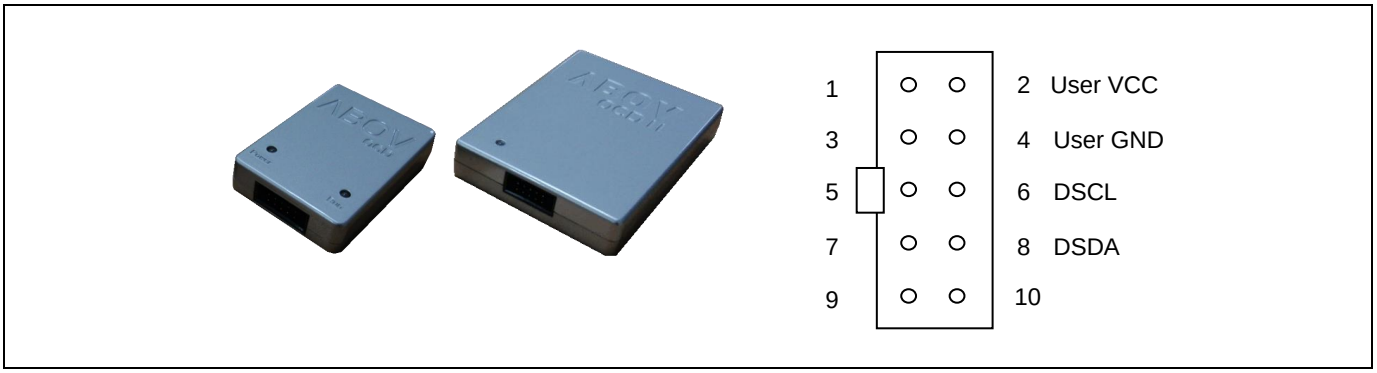


Figure 1.1 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

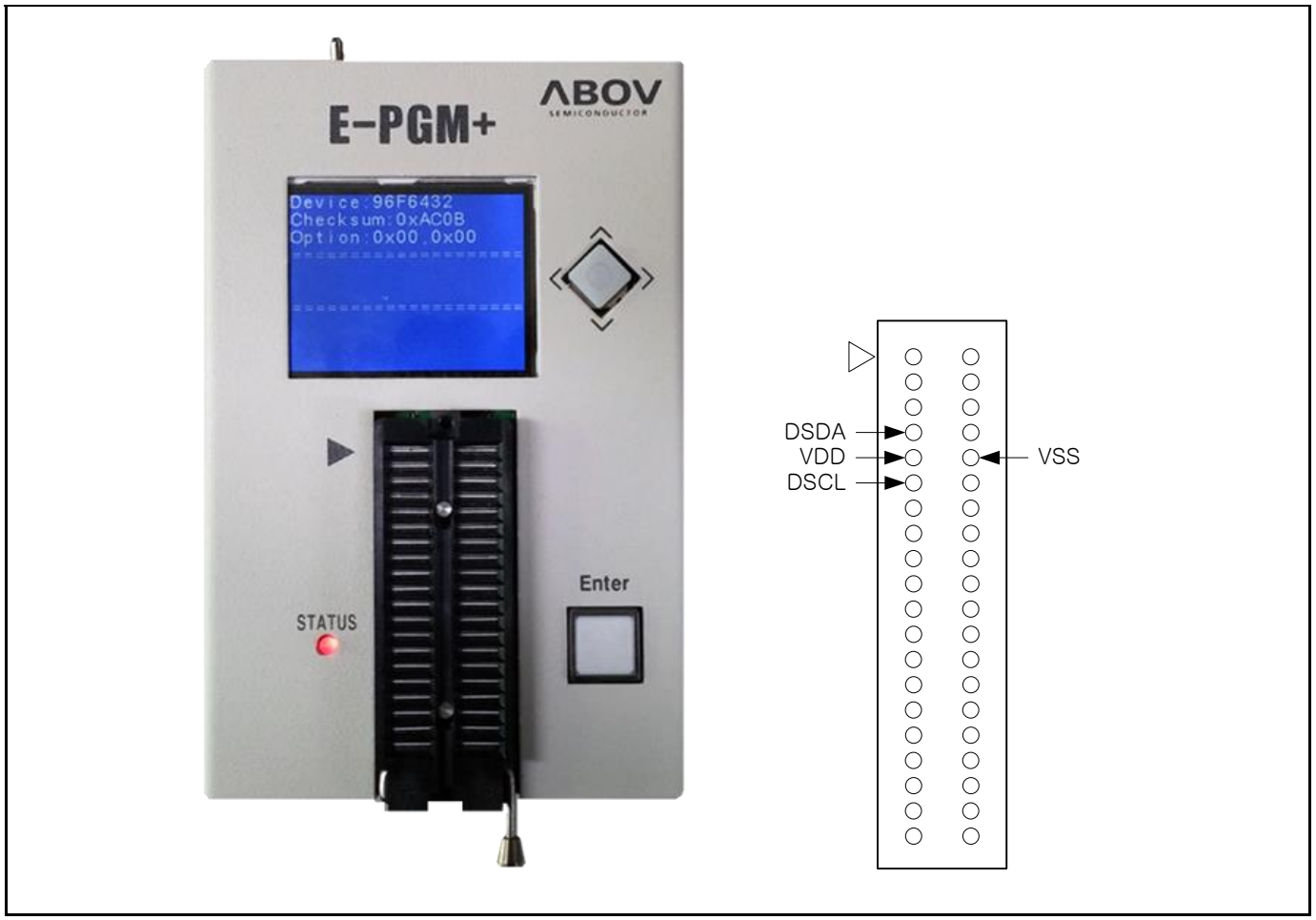


Figure 1.2 E-PGM+(Single writer)

OCD emulator:

It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.3 E-GANG4 and E-GANG6 (for Mass Production)

2 Block diagram

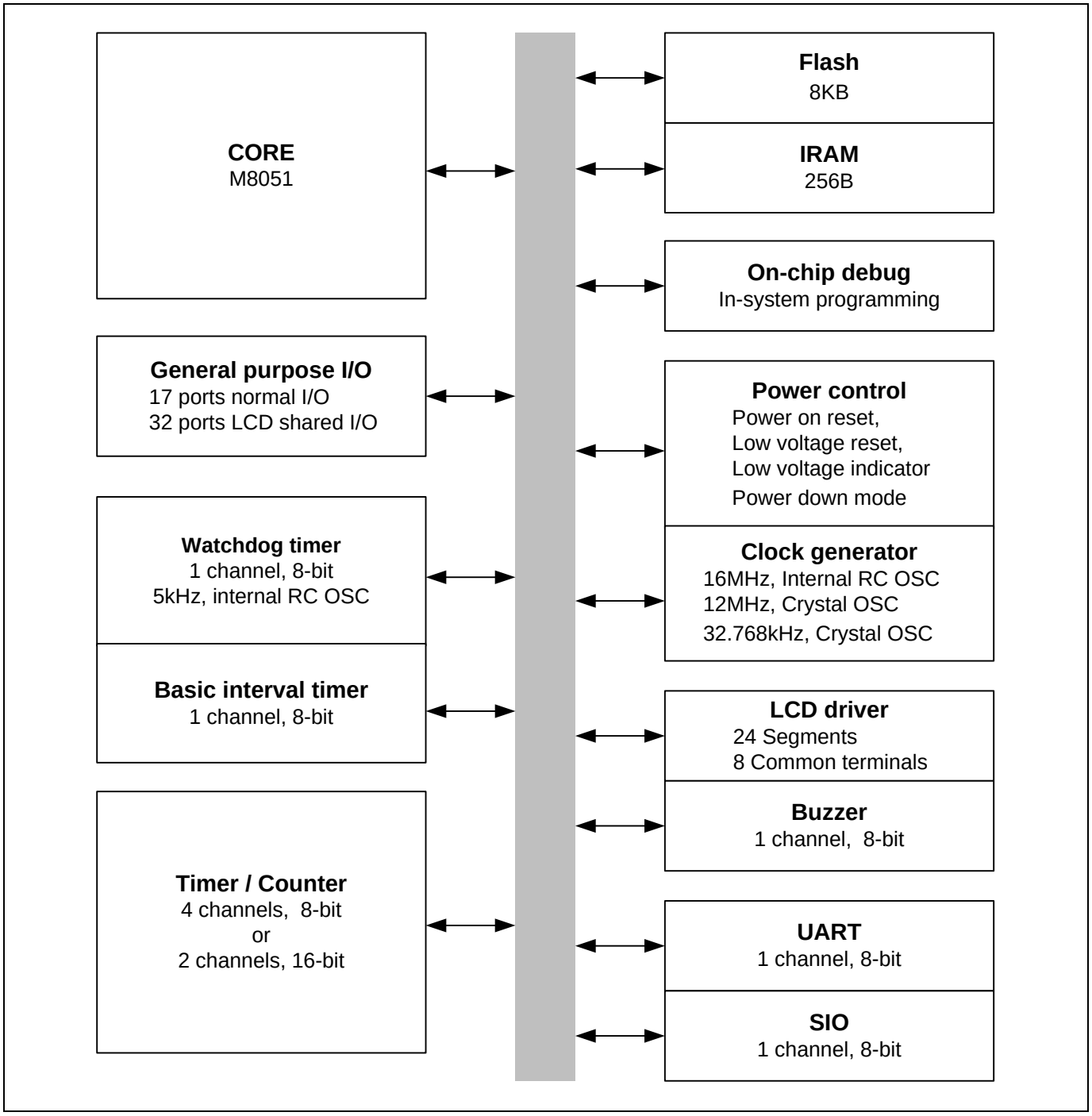


Figure 2.1 MC96F6508A Block Diagram

3 Pin assignment

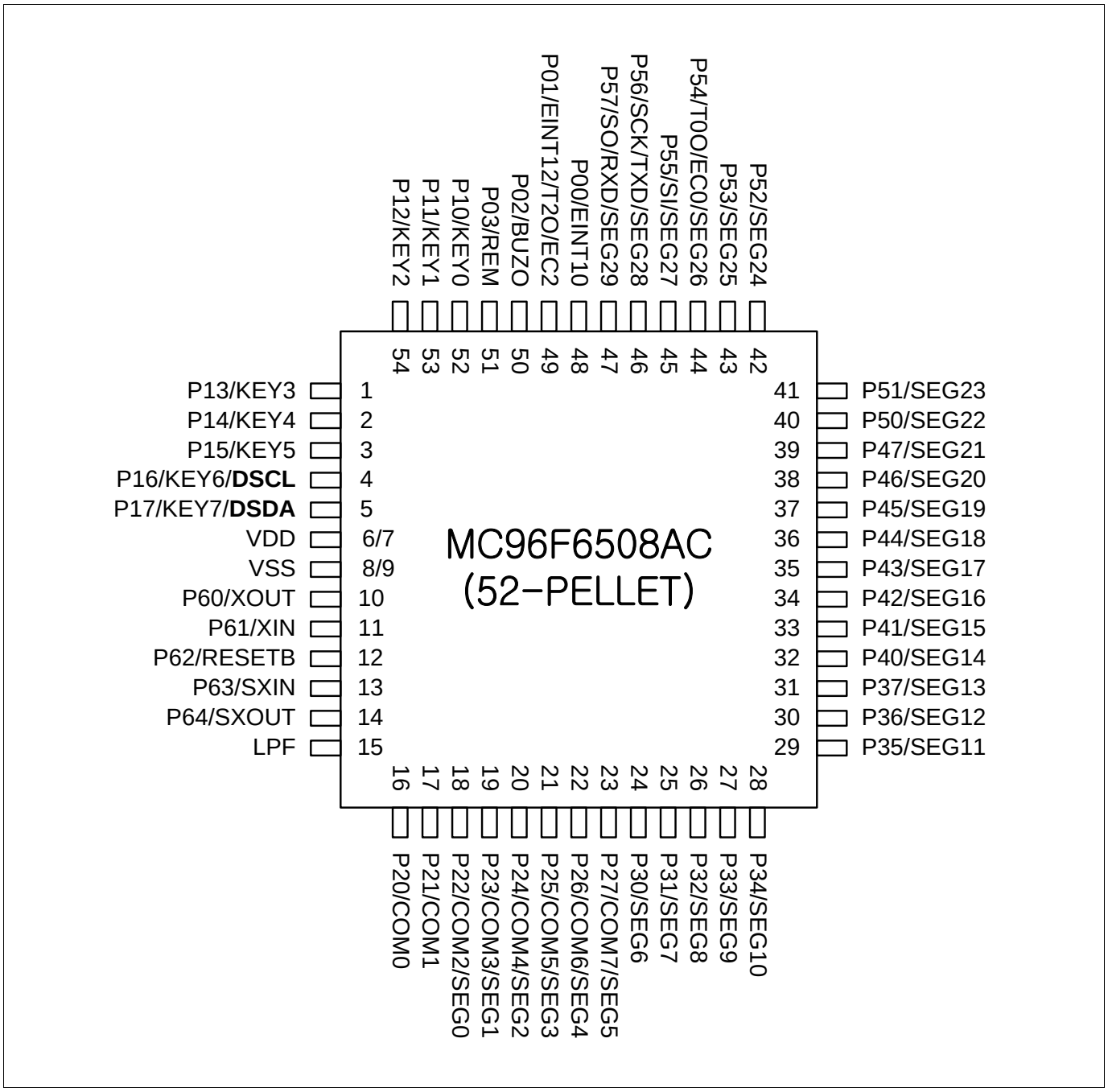


Figure 3.1 MC96F6508AC 52-PELLET Pin Assignment

NOTE)

1. On On-Chip Debugging, ISP uses P1[6:7] pin as DSCL, DSDA.

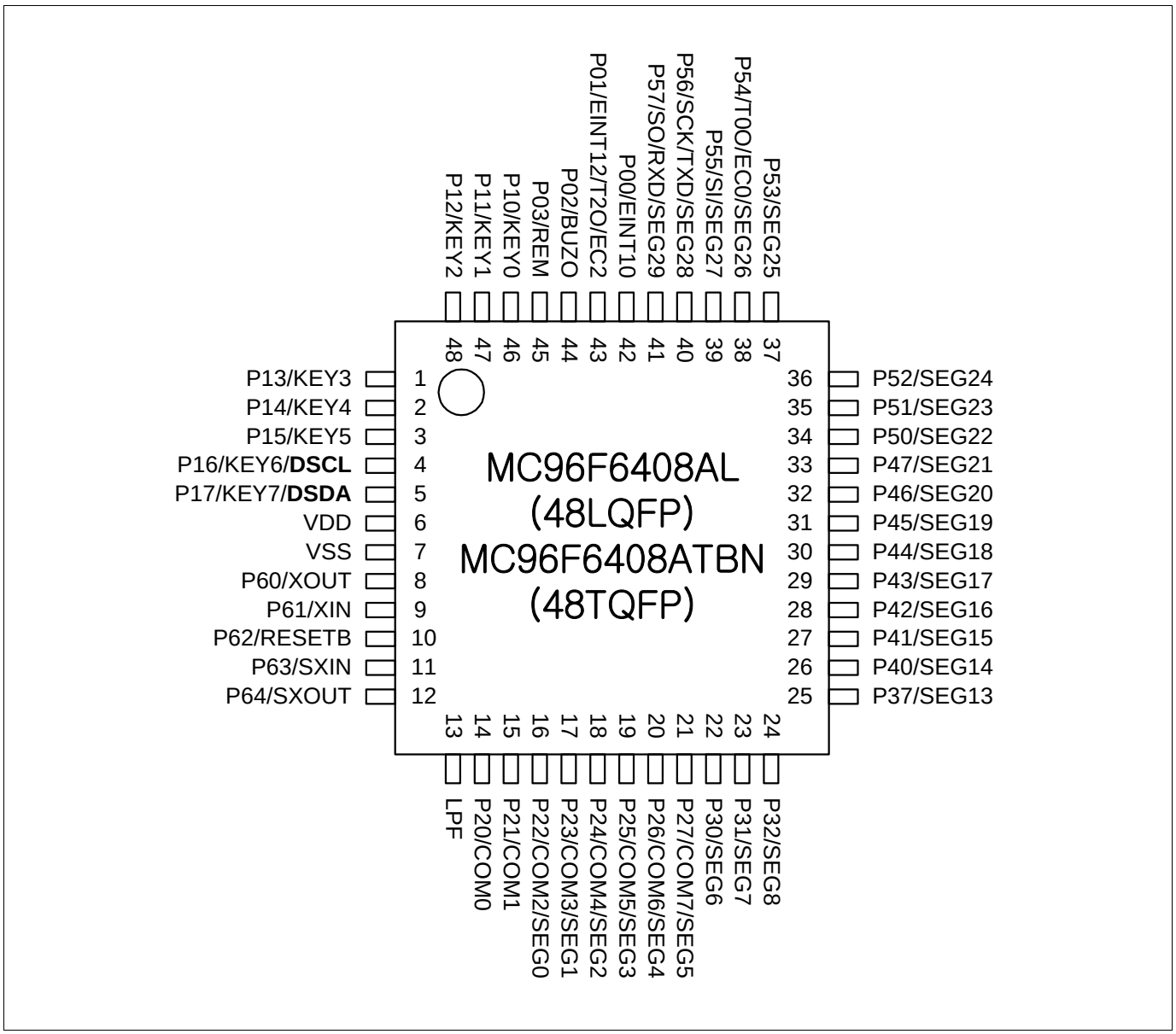


Figure 3.2 MC96F6408AL 48LQFP/MC96F6408ATBN 48TQFP Pin Assignment

NOTE)

1. On On-Chip Debugging, ISP uses P1[6:7] pin as DSCL, DSDA.
2. The P33-P36isnot in the 48-pin package.
3. The P33-P36 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package is used.

4 Package Diagram

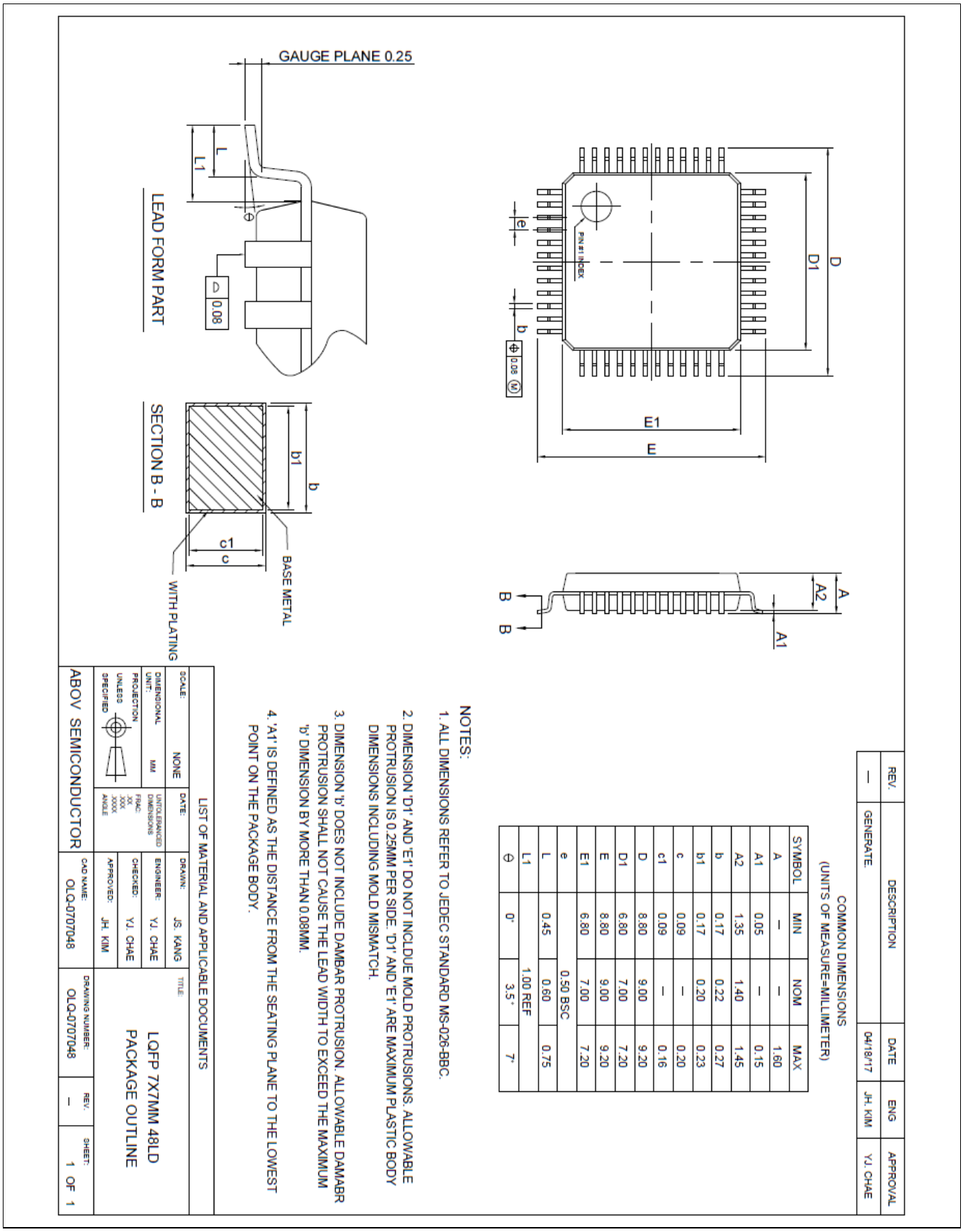
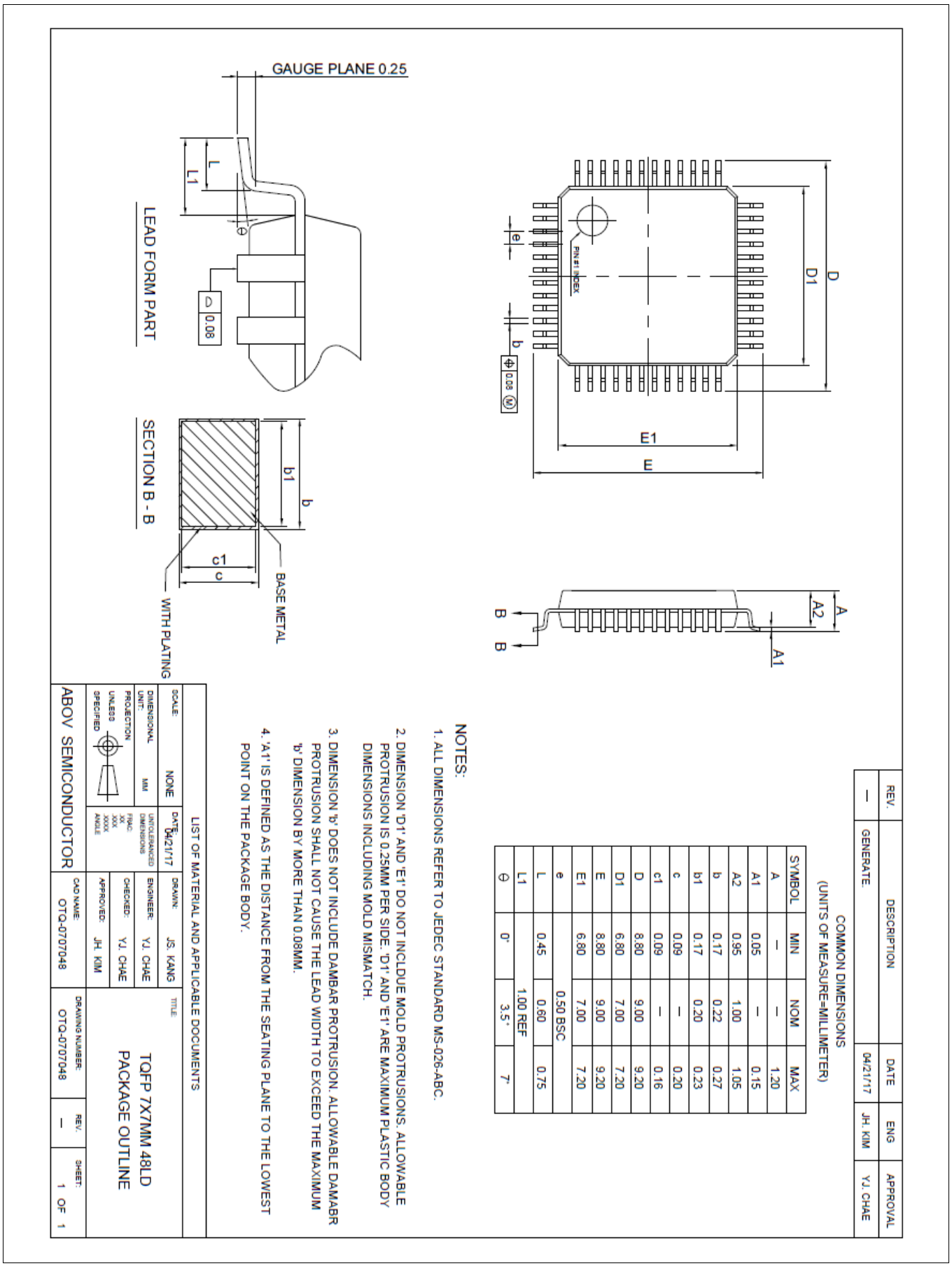


Figure 4.1 48-Pin LQFP Package



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/21/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-ABC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/21/17	DRAWN: JS. KANG	TITLE: TQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: YJ. CHAE	
PROJECTION	FRAC: XX: XXX: ANGLE:	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: JH. KIM	
ABOV SEMICONDUCTOR	CAD NAME: OTQ-0707048	DRAWING NUMBER: OTQ-0707048	REV: —
			SHEET: 1 OF 1

Figure 4.2 48-Pin TQFP Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	The P00 and P01 are a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT10
P01				EINT12/T2O/EC2
P02	I/O	The P02 and P03 are a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	BUZO
P03				REM
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	KEY0
P11				KEY1
P12				KEY2
P13				KEY3
P14				KEY4
P15				KEY5
P16				KEY6/DSCL
P17				KEY7/DSDA
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	COM0
P21				COM1
P22				COM2/SEG0
P23				COM3/SEG1
P24				COM4/SEG2
P25				COM5/SEG3
P26				COM6/SEG4
P27				COM7/SEG5
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P33-P36 is not in the 48-pin package.	Input	SEG6
P31				SEG7
P32				SEG8
P33				SEG9
P34				SEG10
P35				SEG11
P36				SEG12
P37				SEG13

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG14
P41				SEG15
P42				SEG16
P43				SEG17
P44				SEG18
P45				SEG19
P46				SEG20
P47				SEG21
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG22
P51				SEG23
P52				SEG24
P53				SEG25
P54				T0O/EC0/SEG26
P55				SI/SEG27
P56				SCK/TXD/SEG28
P57				SO/RXD/SEG29
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT
P61				XIN
P62				RESETB
P63				SXIN
P64				SXOUT
EINT10	I/O	External interrupt input/Timer 0 capture input	Input	P00
EINT12	I/O	External interrupt input/Timer 2 capture input	Input	P01/T2O/EC2
KEY0	I/O	External Key interrupt input	Input	P10
KEY1				P11
KEY2				P12
KEY3				P13
KEY4				P14
KEY5				P15
KEY6				P16/DSCL
KEY7				P17/DSDA
T0O	I/O	Timer 0 interval output	Input	P54/EC0/SEG26
T2O	I/O	Timer 2 interval output	Input	P01/EINT12/EC2
EC0	I/O	Timer 0 event count input	Input	P54/T0O/SEG26
EC2	I/O	Timer 2 event count input	Input	P01/EINT12/T2O
REM	I/O	Carrier generation output	Input	P03
BUZO	I/O	Buzzer signal output	Input	P02
SCK	I/O	Serial clock input/output	Input	P56/TXD/SEG28
SI	I/O	Serial data input	Input	P55/SEG27
SO	I/O	Serial data output	Input	P57/RXD/SEG29
TXD	I/O	UART data output	Input	P56/SCK/SEG28
RXD	I/O	UART data input	Input	P57/SO/SEG29

Table 5.2 Normal Pin Description (Continued)

PIN Name	I/O	Function	@RESET	Shared with
COM0–COM1	I/O	LCD common signal output	Input	P20–P21
COM2–COM7				P22/SEG0–P27/SEG5
SEG0–SEG5	I/O	LCD segment signal output	Input	P22/COM2–P27/COM7
SEG6–SEG21				P30–P47
SEG22–SEG25				P50–P53
SEG26				P54/T0O/EC0
SEG27				P55/SI
SEG28				P56/SCK/TXD
SEG29				P57/SO/RXD
DSDA	I/O	On chip debugger data input/output(NOTE4, 5)	Input	P17/KEY7
DSCL	I/O	On chip debugger clock input(NOTE4, 5)	Input	P16/KEY6
RESETB	I	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P62
XIN	I/O	Main oscillator pins	Input	P61
XOUT				P60
SXIN	I/O	Sub oscillator pins	Input	P63
SXOUT				P64
LPF	–	Loop filter pump output of PLL.	–	–
VDD, VSS	–	Power input pins	–	–

Table 5.3 Normal Pin Description (Continued)

NOTE)

1. The P33-P36isnot in the 48-pin package.
2. The P62/RESETB pin is configured as one of the P62 and the RESETB pin by the “CONFIGURE OPTION”.
3. The P60/XOUT, P61/XIN, P63/SXIN, and P64/SXOUT pins are configured as a function pin by software control.
4. If the P16/KEY6/DSCL and P17/KEY7/DSDA pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
5. The P16/KEY6/DSCL and P17/KEY7/DSDA pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.

6 Port Structures

6.1 General Purpose I/O Port

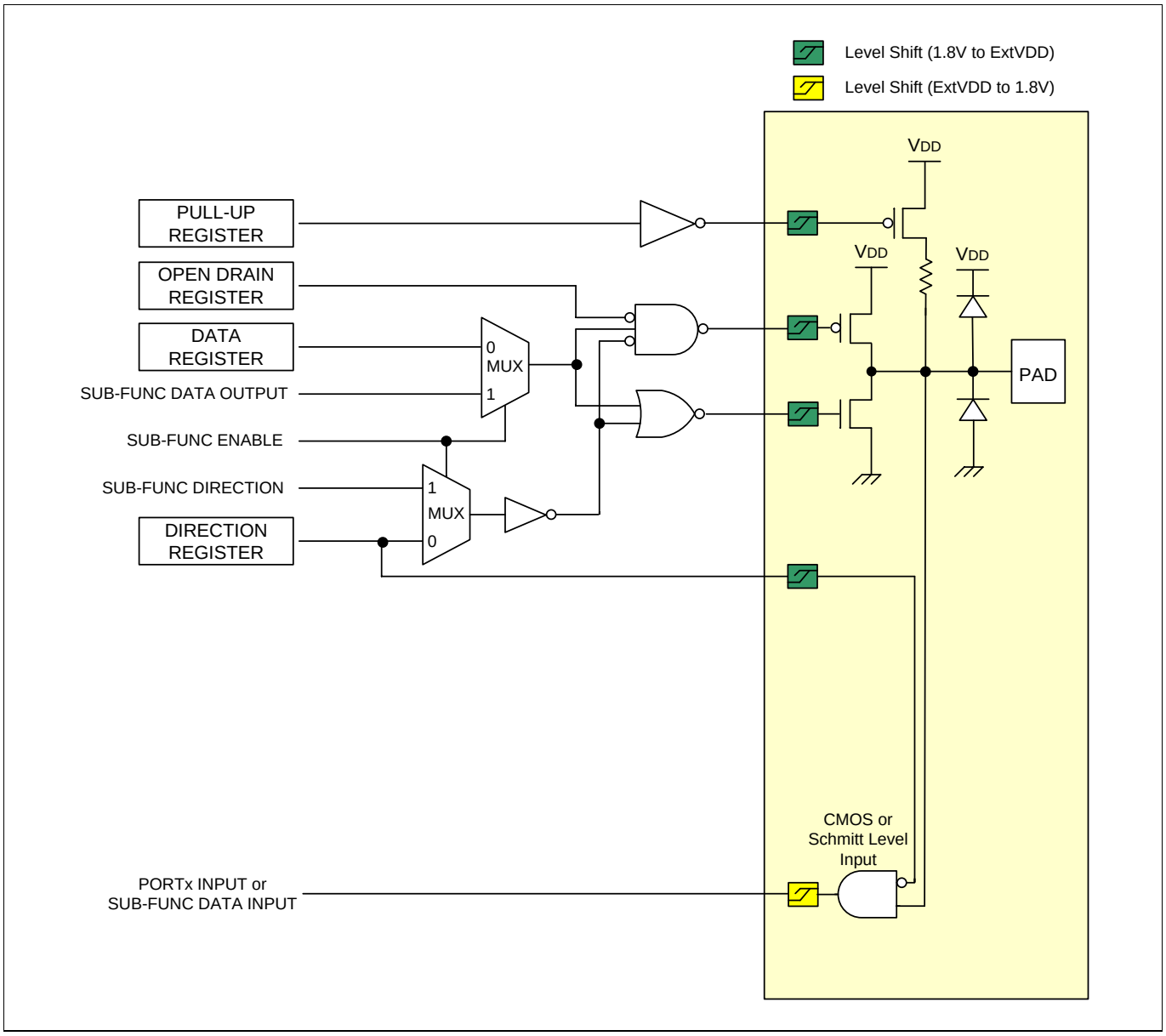


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

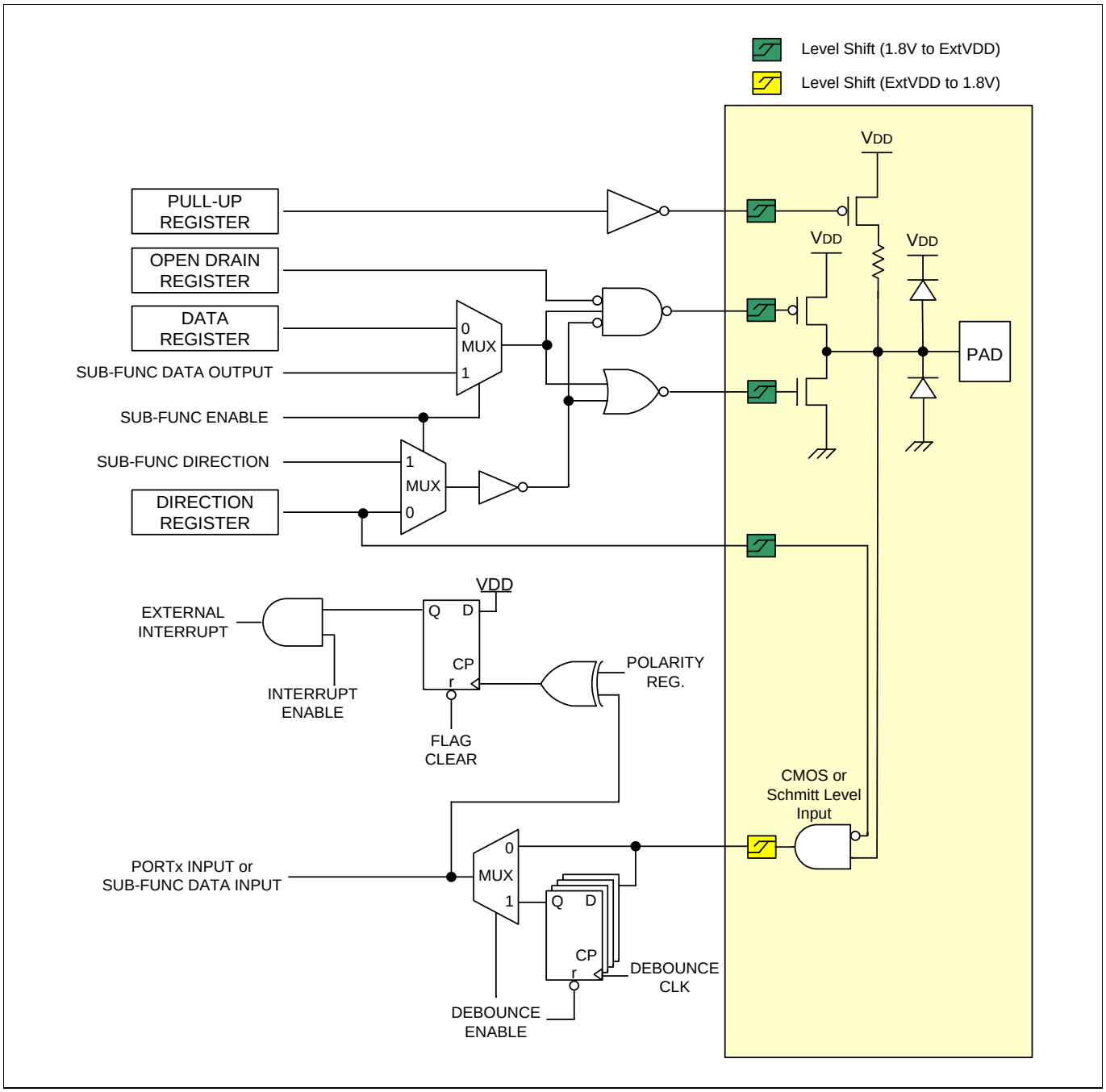


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7-1. Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Supply Voltage	VDD	f_X= 32 ~ 38kHz	Sub crystal	1.8	–	5.5	V
		f_X= 0.4 ~ 4.2MHz	Main Crystal	1.8	–	5.5	
		f_X=0.4~12.0MHz		2.7	–	5.5	
		f_X=0.5~8.0MHz	Internal RC	1.8	–	5.5	
		f_X=0.5~16.0MHz		2.0	–	5.5	
		f_X=1.0~16.4MHz	PLL	2.0	–	5.5	
Operating Temperature	T_{OPR}	VDD=1.8V~5.5V		-40	–	85	°C

Table 7-2. Recommended Operating Conditions

7.3 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7-3. Power-On Reset Characteristics

7.4 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V.		–	1.60	1.79	V
				1.85	2.00	2.15	
				1.95	2.10	2.25	
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

Table 7-4. LVR and LVI Characteristics

7.5 Phase Locked Loop Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

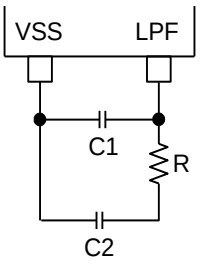
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Frequency Range	–		–	32.768	–	kHz
Output Frequency Range	f_{VCO}		1.024	–	16.384	MHz
Clock Duty Ratio	T_{OD}		45	50	55	%
Tolerance	–		–	–	±1	%
Settling Time	t_D		–	10	100	ms
PLL Current	I_{PLL}	Enable, f_{VCO}=16.384MHz	–	0.5	1.0	mA
		Disable	–	–	0.1	uA

Table 7-5. Phase Locked Loop Characteristics

NOTE)

1. Where R= 6.8kΩ, C1=820pF, and C2= 10nF.

7.6 Internal RC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	VDD = 2.0V ~ 5.5V		–	16.0	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -20°C to +85°C		–	–	±2.5	
		T_A = -40°C to +85°C		–	–	±3.5	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{FS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7-6. Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS. Refer to the“7.21 Recommended Circuit and Layout".

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7-7. Internal WDTRC Oscillator Characteristics

7.8 LCD Voltage Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
LCD Voltage	V_{LC0}	LCD contrast disabled,1/4 bias		Typx0.95	VDD	Typx1.05	V
		LCD contrast enabled, 1/4 bias, R_{LCD1} No panel load, VDD = 2.7V to 5.5V	LCDCCR=00H	Typx0.9	VDDx16/31	Typx1.1	V
			LCDCCR=01H		VDDx16/30		
			LCDCCR=02H		VDDx16/29		
			LCDCCR=03H		VDDx16/28		
			LCDCCR=04H		VDDx16/27		
			LCDCCR=05H		VDDx16/26		
			LCDCCR=06H		VDDx16/25		
			LCDCCR=07H		VDDx16/24		
			LCDCCR=08H		VDDx16/23		
			LCDCCR=09H		VDDx16/22		
			LCDCCR=0AH		VDDx16/21		
			LCDCCR=0BH		VDDx16/20		
			LCDCCR=0CH		VDDx16/19		
			LCDCCR=0DH		VDDx16/18		
			LCDCCR=0EH		VDDx16/17		
			LCDCCR=0FH		VDDx16/16		
LCD Mid Bias Voltage(note)	V_{LC1}	VDD=2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	V_{LC2}			Typ-0.2	2/4xVLC0	Typ+0.2	
	V_{LC3}			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	VLCD=3V, ILOAD=±10uA		–	5	10	kΩ
LCD Bias Dividing Resistor	R_{LCD1}	T_A = 25°C		40	60	80	
	R_{LCD2}			80	120	160	

Table 7-8. LCD Voltage Characteristics

NOTE)

1. It is middle output voltage when the VDD and the V_{LC0} node are connected.

7.9 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P00–P01, P1, P6, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P00–P01, P1, P6, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	V
Output High Voltage	V_{OH}	All output ports; I_{OH}=-2mA, VDD=4.5V		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	All output ports; I_{OL}= 15mA, VDD=4.5V		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1.0	uA
Input Low Leakage Current	I_{IL}	All input ports		-1.0	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25 °C ,VDD=5V		2500	5000	10000	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz	VDD= 5V±10%	–	3.0	6.0	mA
		f_{XIN}= 10MHz	VDD= 3V±10%	–	2.2	4.4	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	3.0	6.0	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz	VDD= 5V±10%	–	1.3	2.6	mA
		f_{XIN}= 10MHz	VDD= 3V±10%	–	0.7	1.4	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	0.8	1.6	
	I_{DD3}	f_{SUB}=32.768kHz VDD= 3V±10% T_A= 25°C	Sub RUN	–	60.0	90.0	uA
	I_{DD4}		Sub IDLE	–	8.0	16.0	uA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	uA

Table 7-9. DC Characteristics

NOTE)

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB Input Low Width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt Input High, Low Width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5 V (n=0 and 2)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5 V (n=0 and 2)	20	–	–	
REM port High, Low Width	t_{REMWH}, t_{REMWL}	REM, VDD = 5 V	5	–	–	us

Table 7-10. AC Characteristics

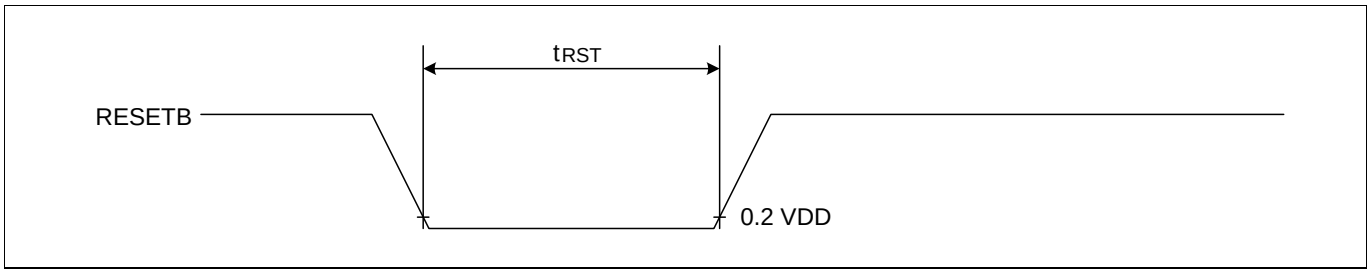


Figure 7.1 Input Timing for RESETB

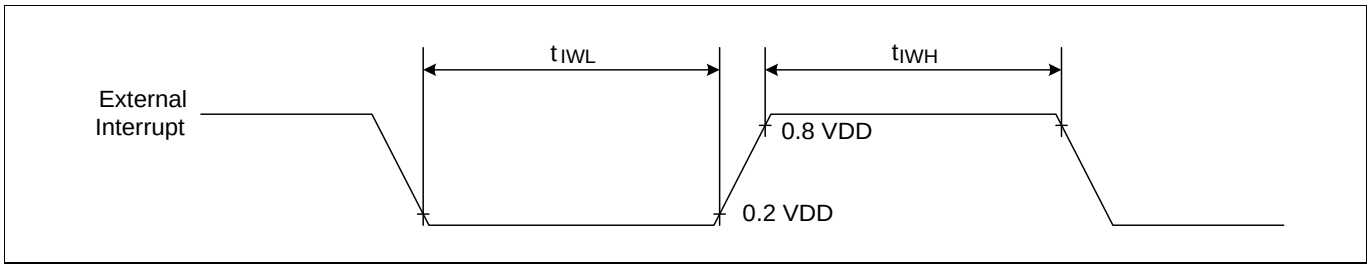


Figure 7.2 Input Timing for External Interrupts

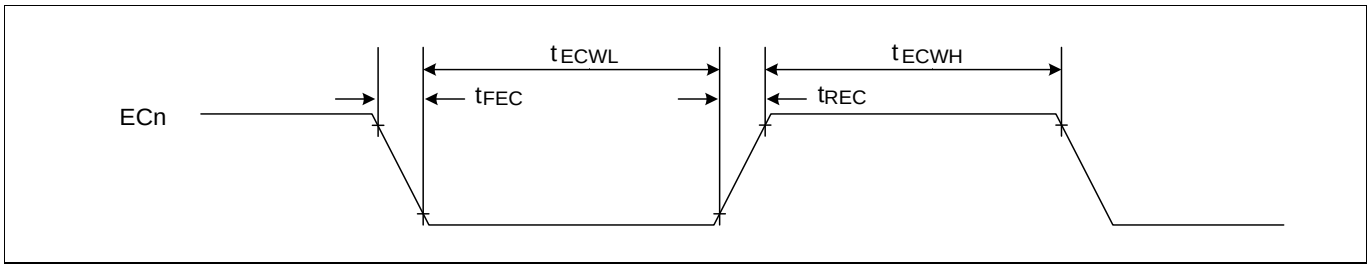


Figure 7.3 Input Timing for EC0 and EC2

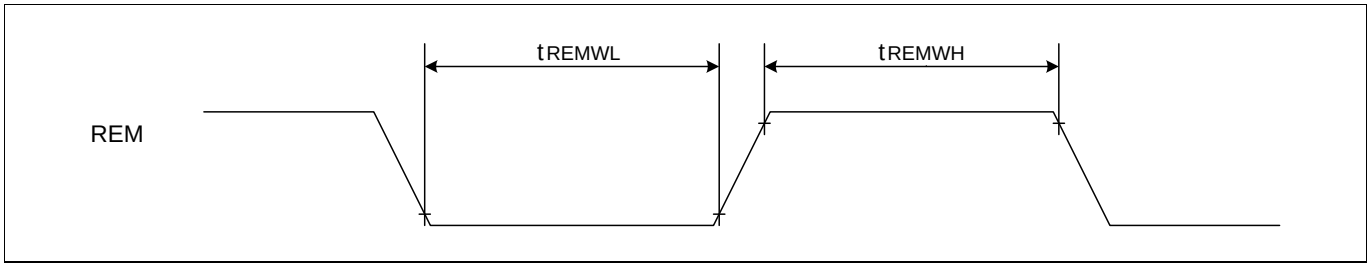


Figure 7.4 REM Timing

7.11 UART Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial Port Clock Cycle Time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output Data Setup to Clock Rising Edge	t_{S1}	590	t_{CPU} x 13	–	ns
Clock Rising Edge to Input Data Valid	t_{S2}	–	–	590	ns
Output Data Hold after Clock Rising Edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input Data Hold after Clock Rising Edge	t_{H2}	0	–	–	ns
Serial Port Clock High, Low Level Width	t_{HIGH},t_{LOW}	470	t_{CPU} x 8	970	ns

Table 7-11. UART Characteristics

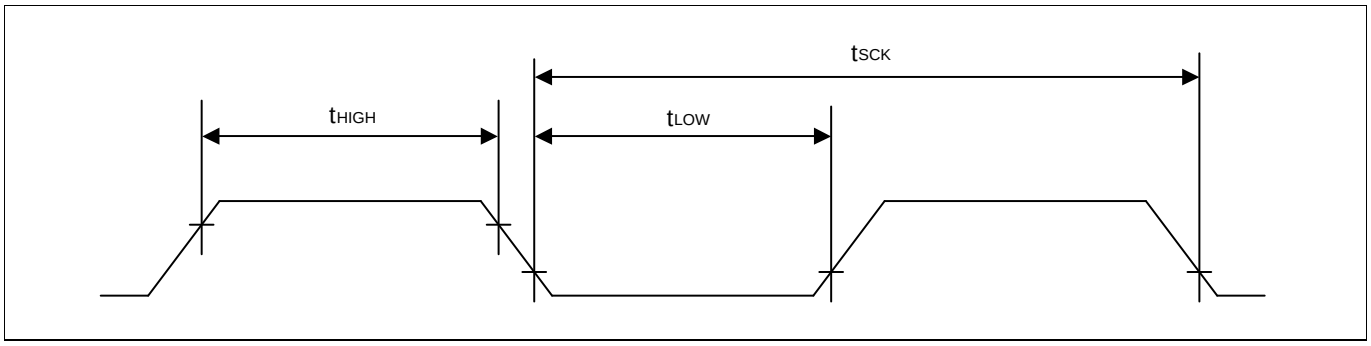


Figure 7.5 Waveform for UART Timing Characteristics

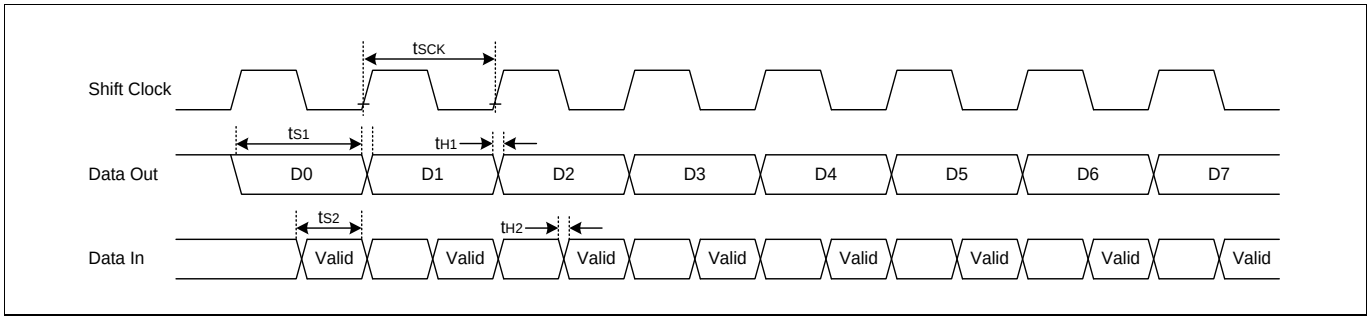


Figure 7.6 Timing Waveform for the UART Module

7.12 Serial I/O Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCK cycle time	t_{KCY}	External SCK source	1,000	–	–	ns
		Internal SCK source	1,000			
SCK high, low width	t_{KH}, t_{KL}	External SCK source	500			ns
		Internal SCK source	t_{KCY}/2-50			
SI setup time to SCK high	t_{SIK}	External SCK source	250			ns
		Internal SCK source	250			
SI hold time to SCK high	t_{KSI}	External SCK source	400			ns
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	ns
		Internal SCK source			250	

Table 7-12. Serial I/O Characteristics

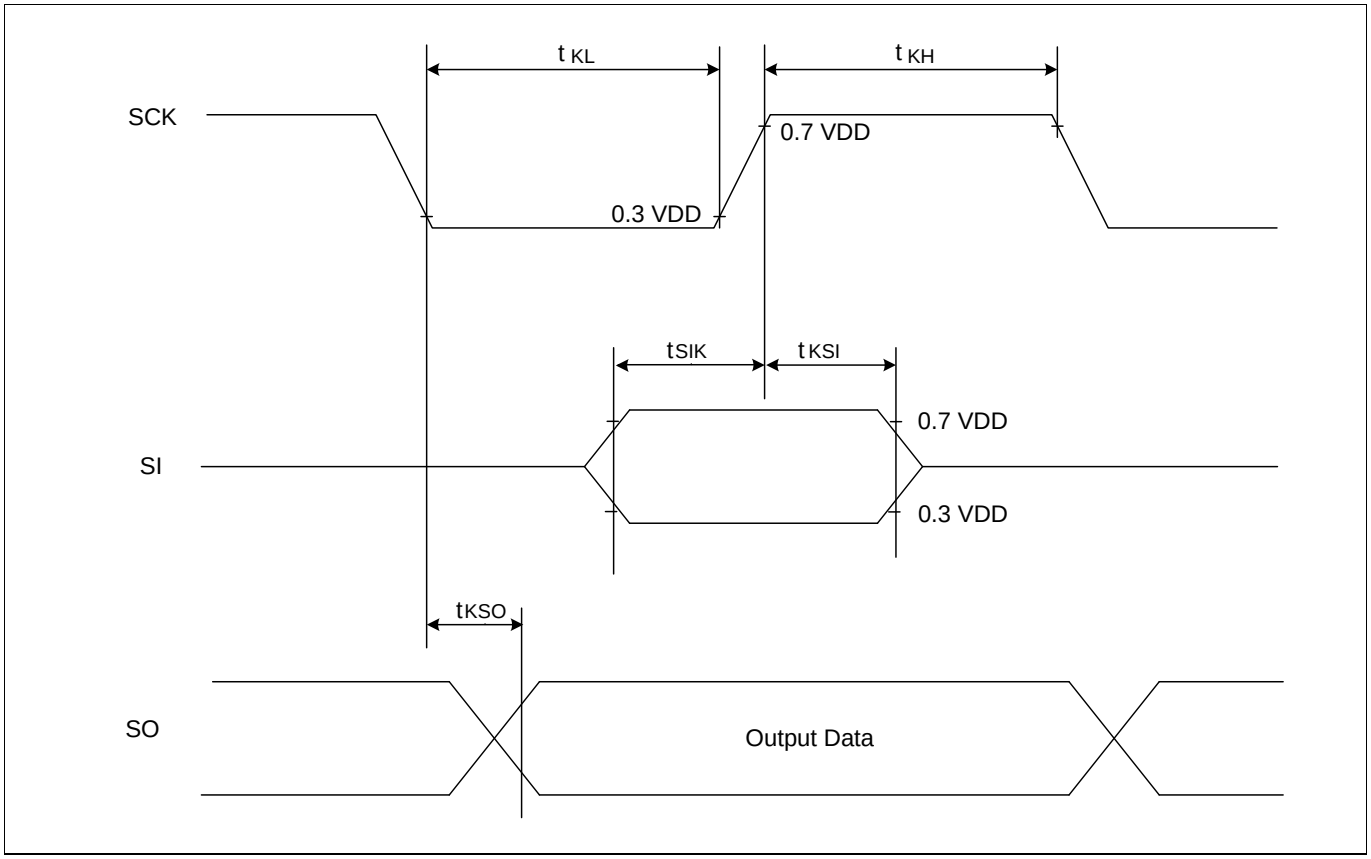


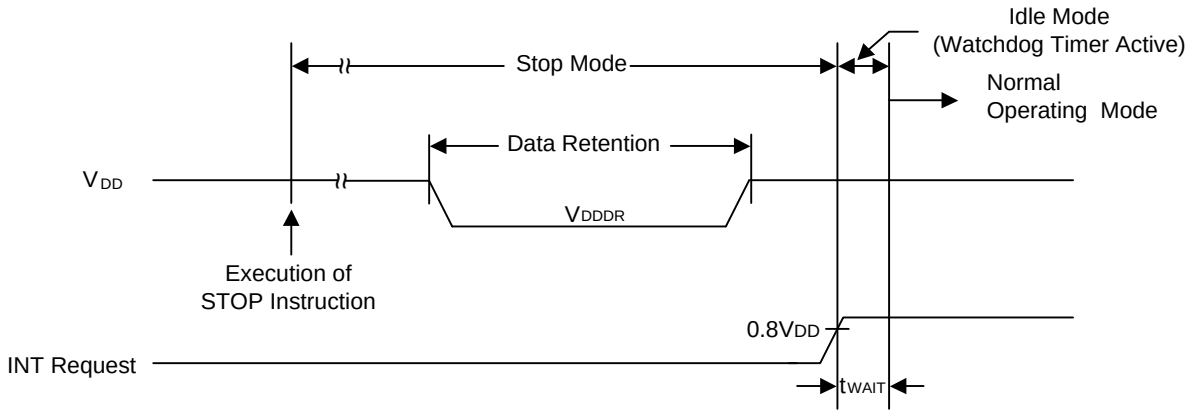
Figure 7.7 Serial Interface Data Transfer Timing

7.13 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

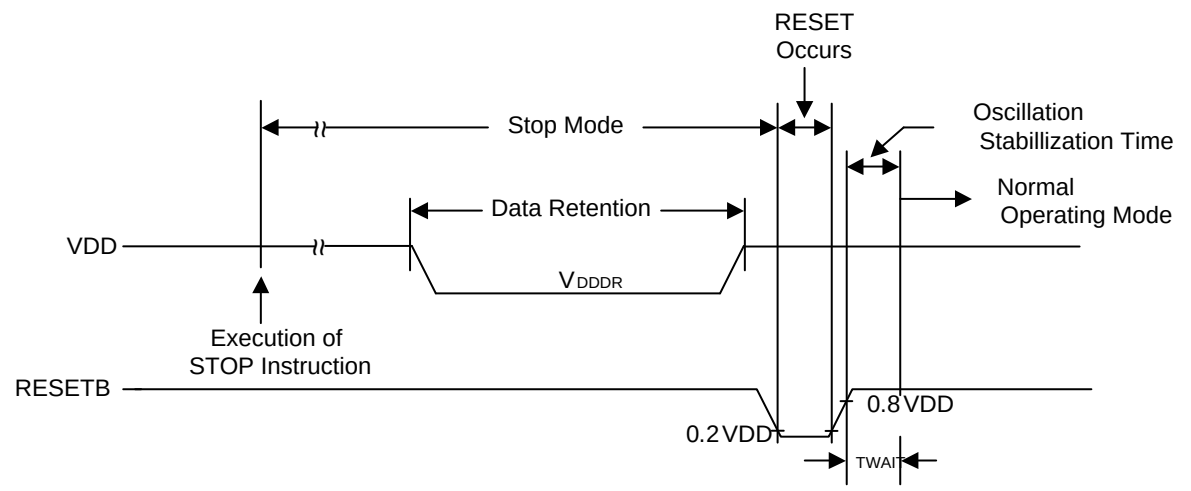
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7-13. Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.8 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (16.4 ms at fx=1MHz).

Figure 7.9 Stop Mode Release Timing when Initiated by RESETB

7.14 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	Times
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Table 7-14. Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must not be set to “10b” (Sub X-TAL for system clock).

7.15 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7-15. Input/Output Capacitance

7.16 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	

Table 7-16. Main Clock Oscillator Characteristics

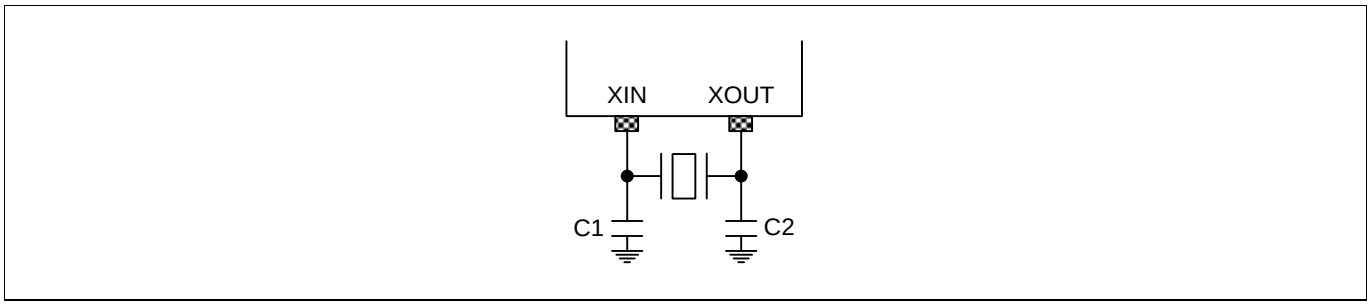


Figure 7.10 Crystal/Ceramic Oscillator

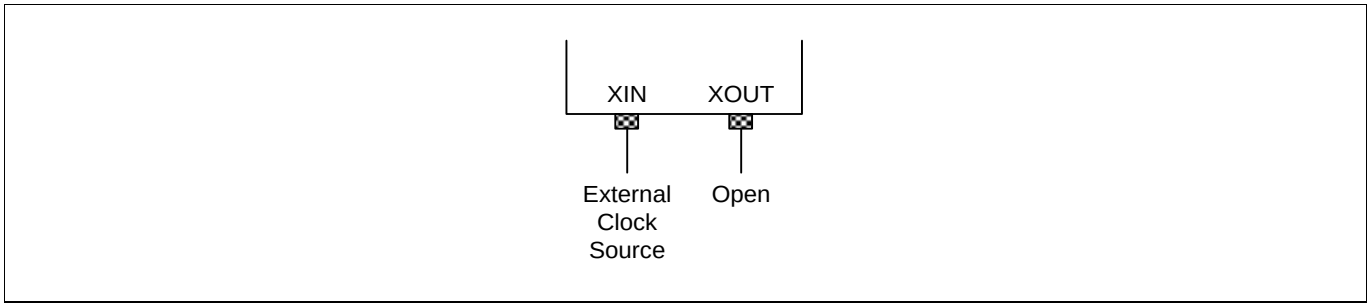


Figure 7.11 External Clock

7.17 Sub Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

Table 7-17. Sub Clock Oscillator Characteristics

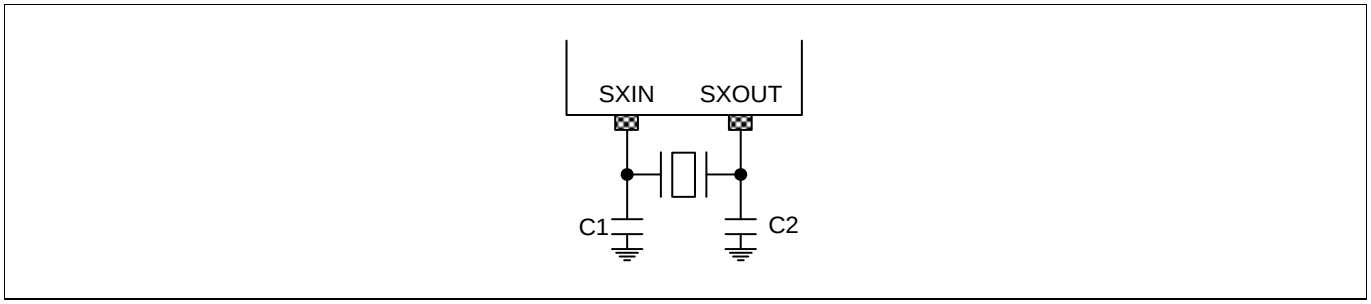


Figure 7.12 Crystal Oscillator

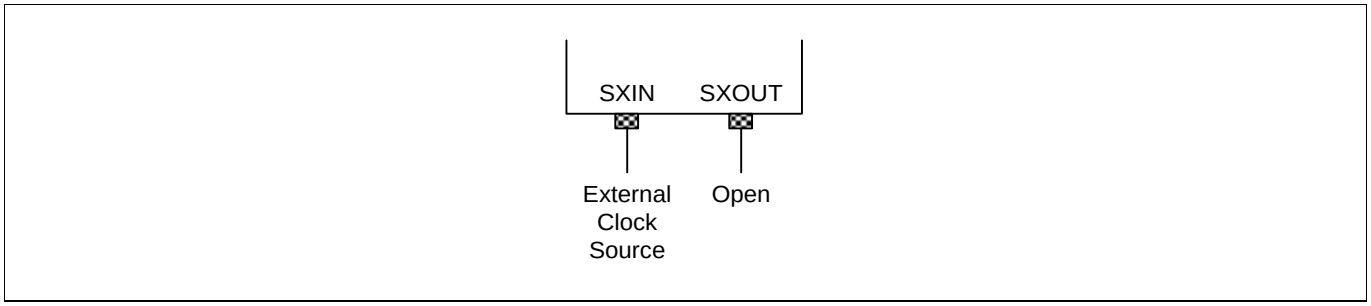


Figure 7.13 External Clock

7.18 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx> 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

Table 7-18. Main Oscillation StabilizationCharacteristics

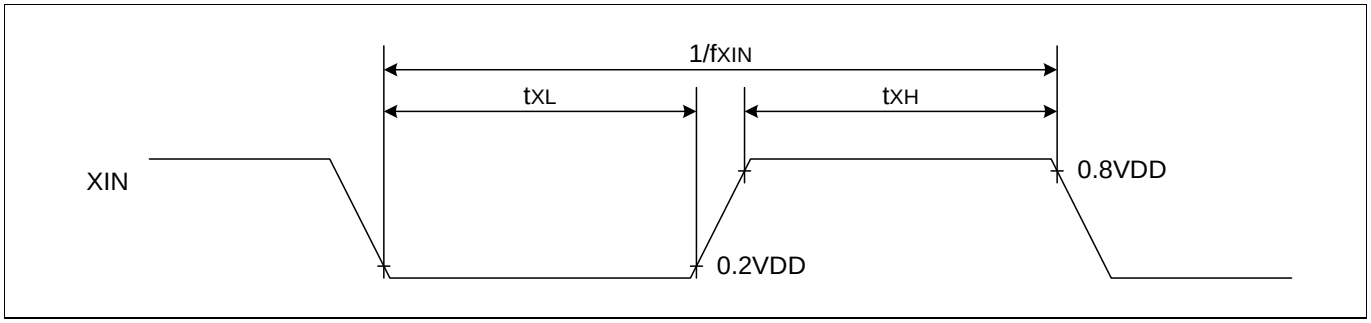


Figure 7.14 Clock Timing Measurement at XIN

7.19 Sub Oscillation Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

Table 7-19. Sub Oscillation StabilizationCharacteristics

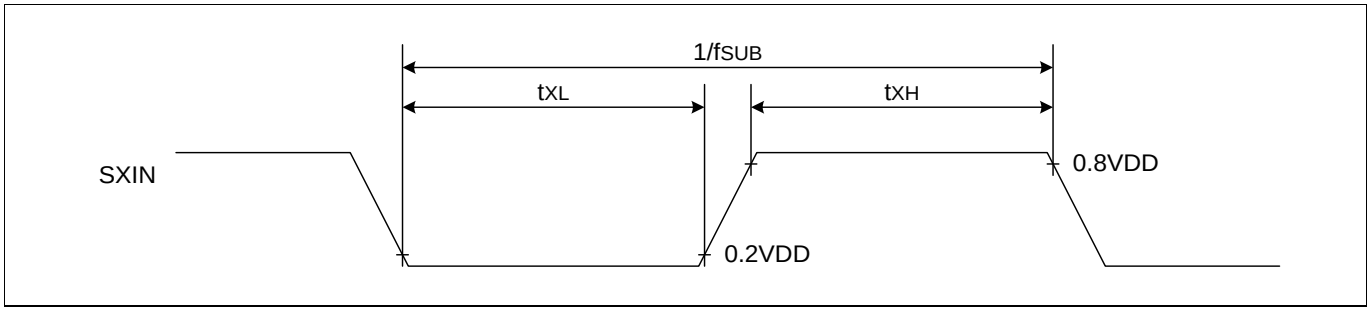


Figure 7.15 Clock Timing Measurement at SXIN

7.20 Operating Voltage Range

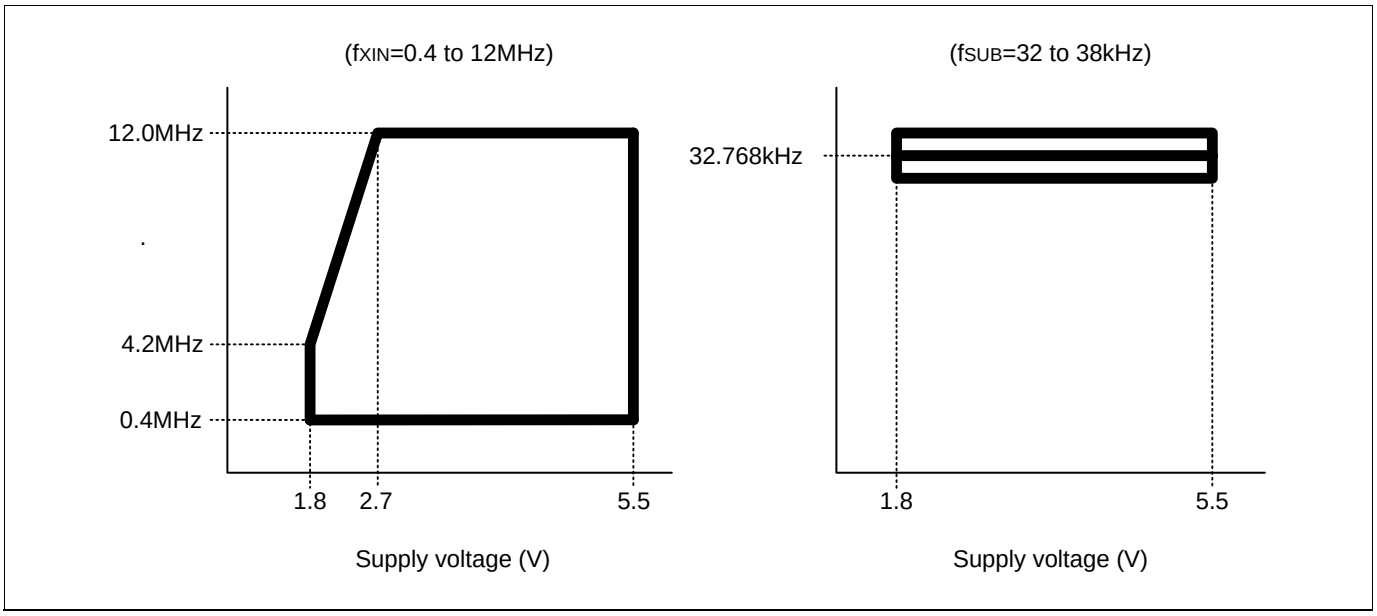


Figure 7.16 Operating Voltage Range

7.21 Recommended Circuit and Layout

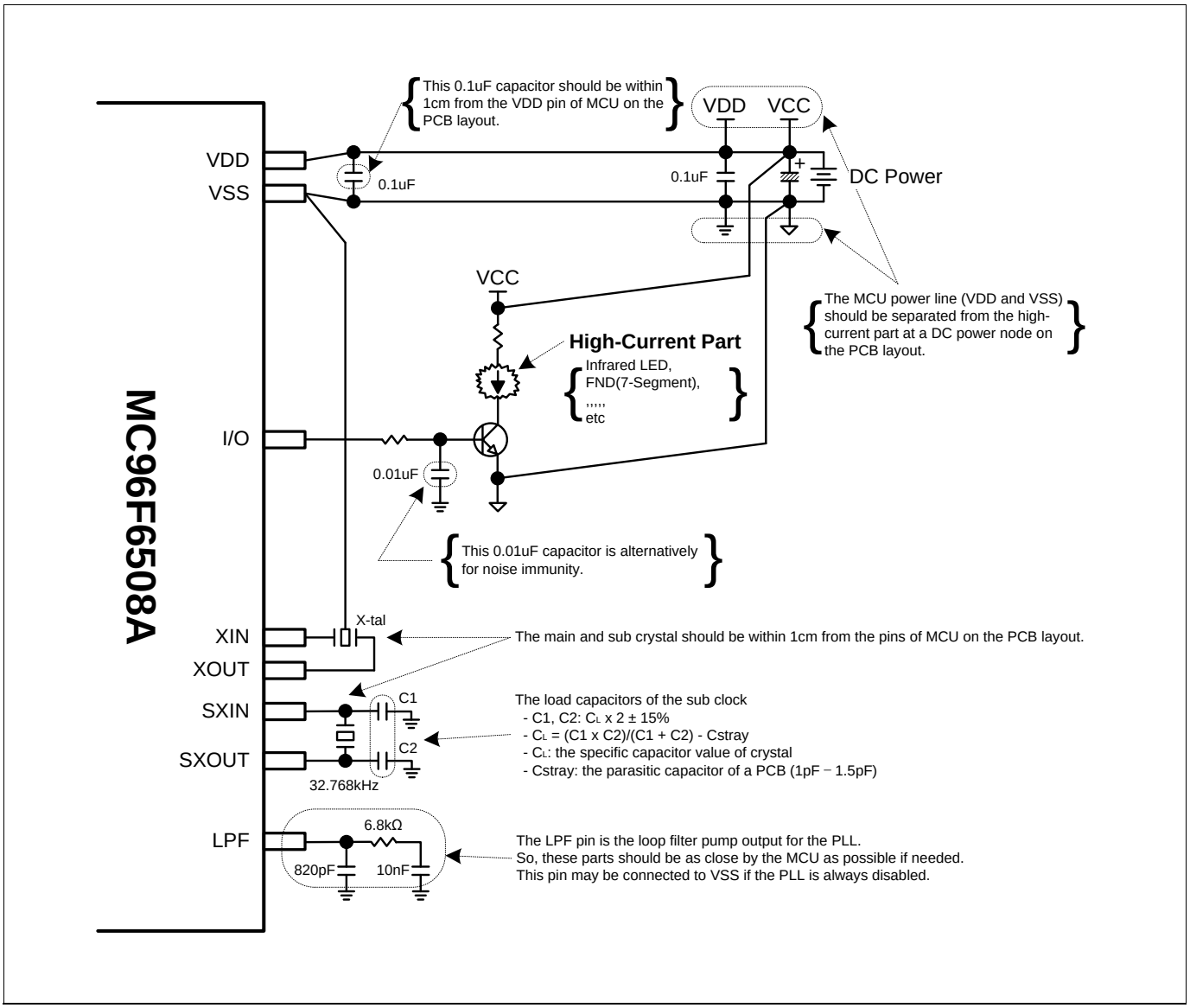
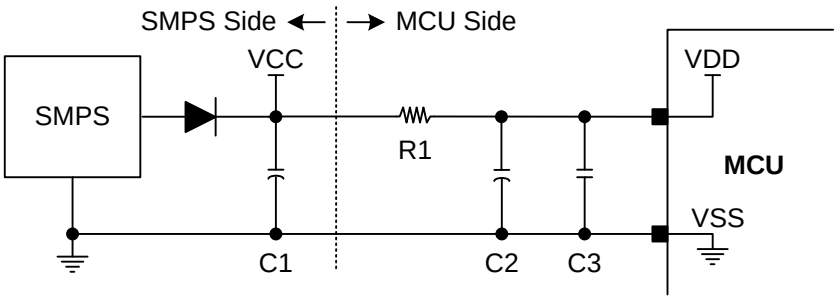


Figure 7.17 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.18 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

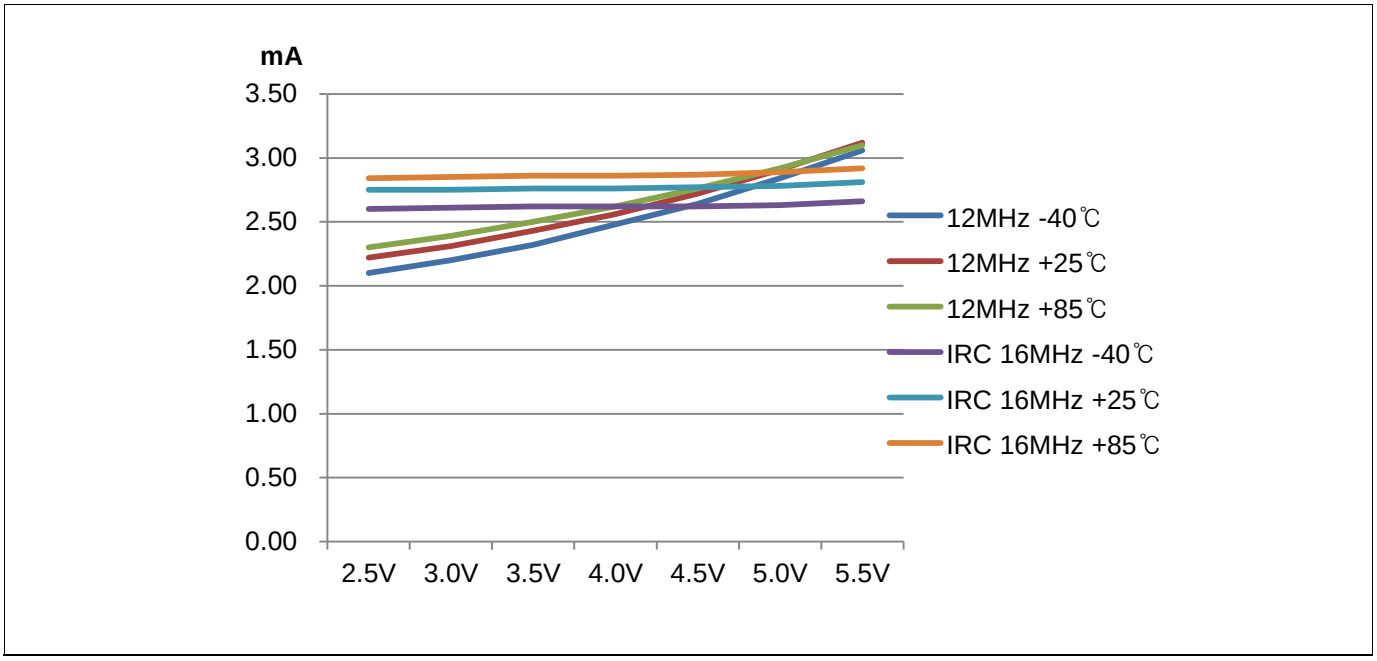


Figure 7.19 RUN (IDD1) Current

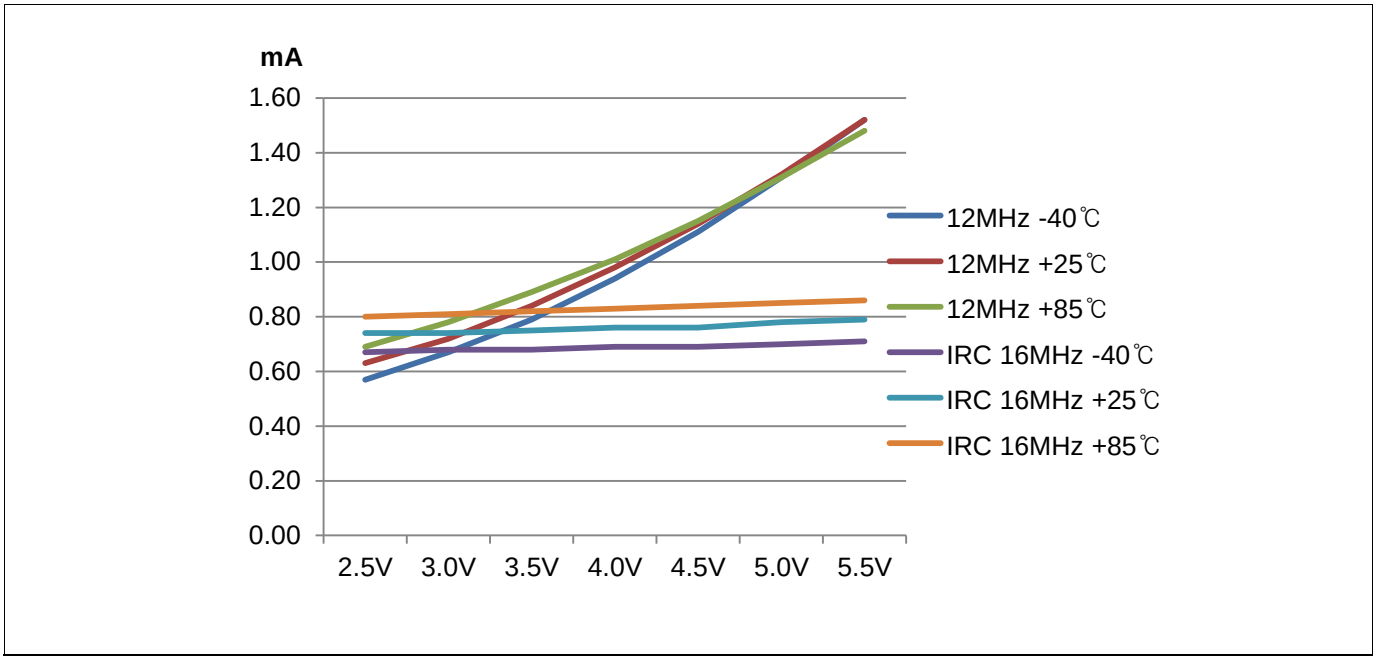


Figure 7.20 IDLE (IDD2) Current

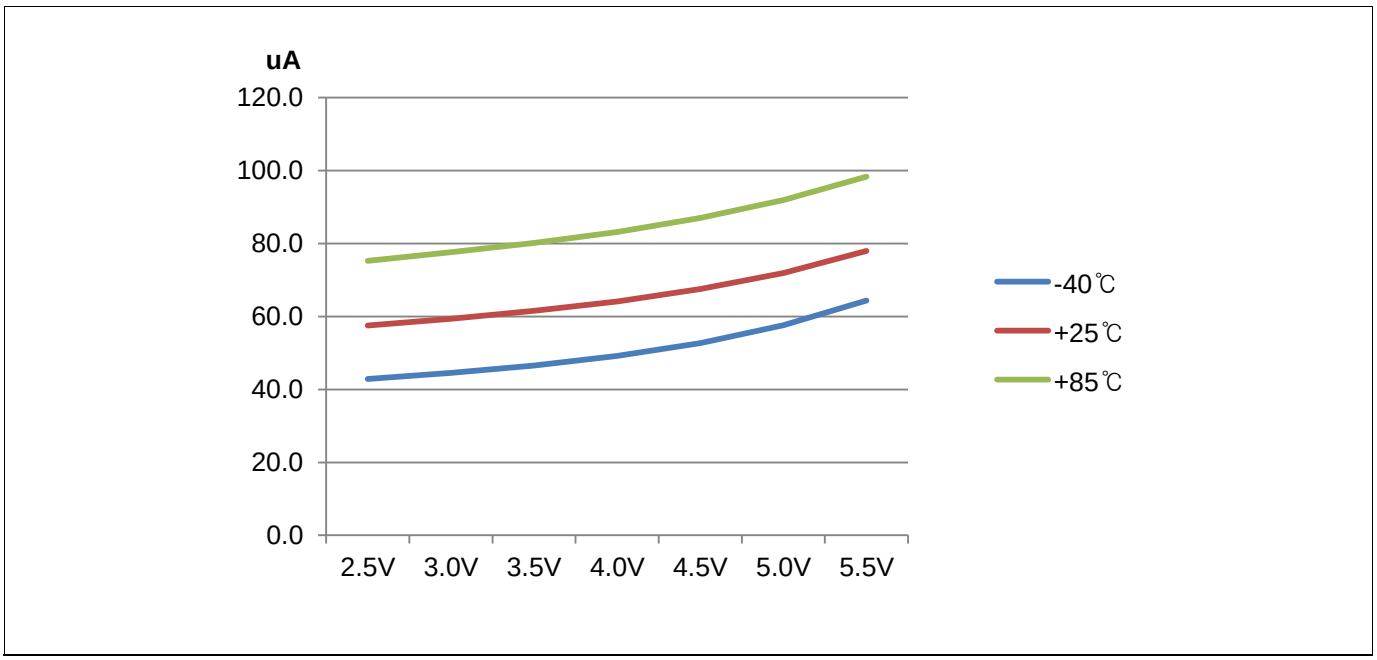


Figure 7.21 SUB RUN (IDD3) Current

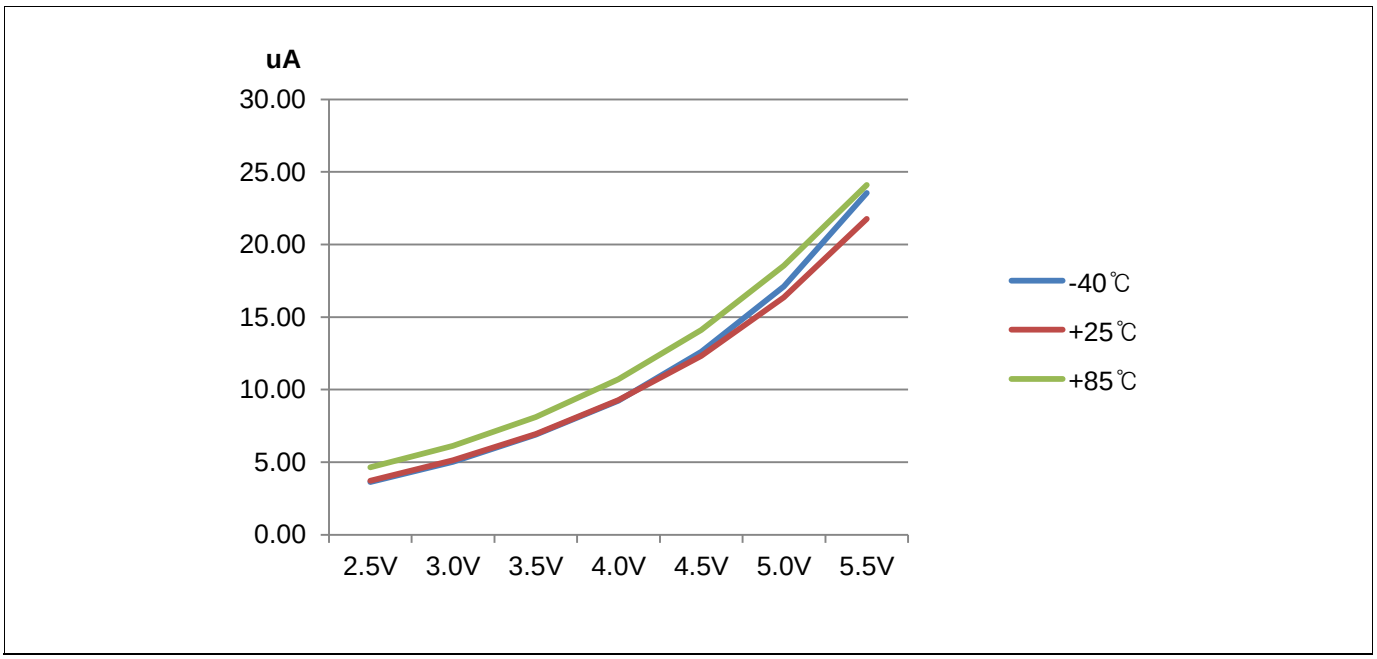


Figure 7.22 SUB IDLE (IDD4) Current

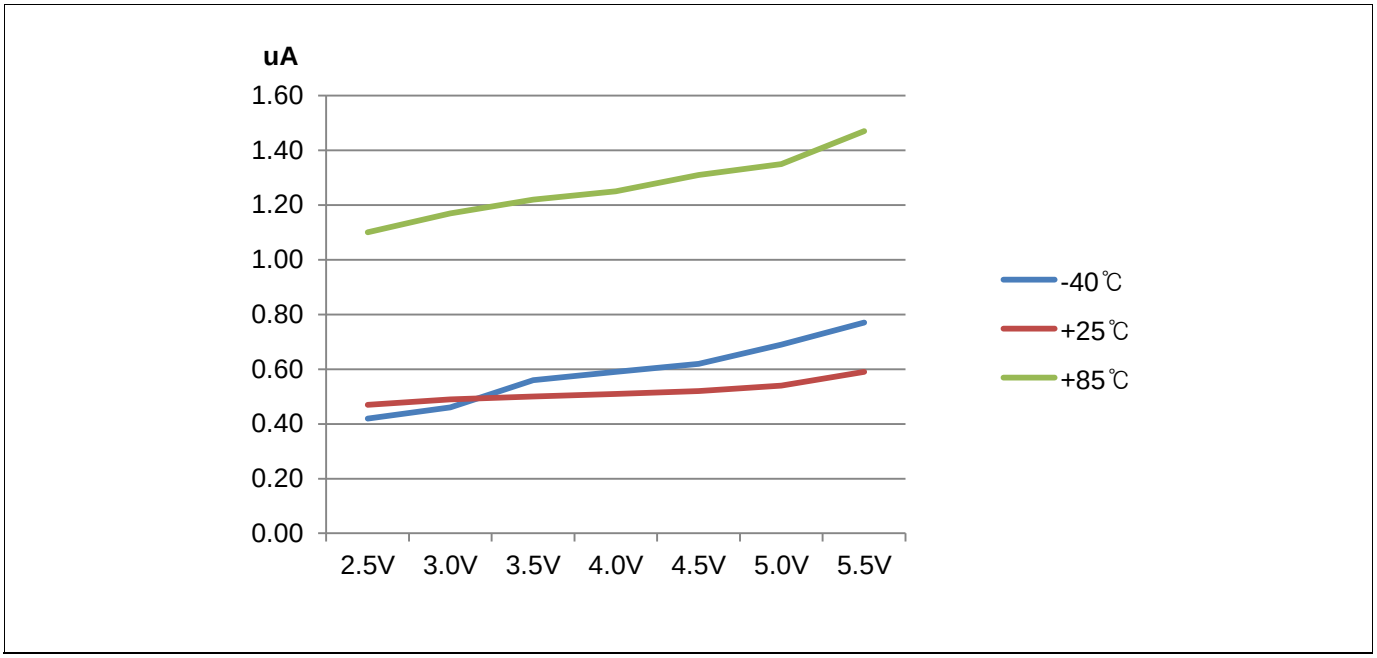


Figure 7.23 STOP (IDD5) Current

8 Memory

The MC96F6508A addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

MC96F6508A provides on-chip 8Kbytes of the ISP type flash program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes and it includes the stack area and 30 bytes of LCD display RAM.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64Kbytes, but this device has just 8Kbytes program memory space.

Figure 8-1 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 10, for example, is assigned to location 000BH. If external interrupt 10 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

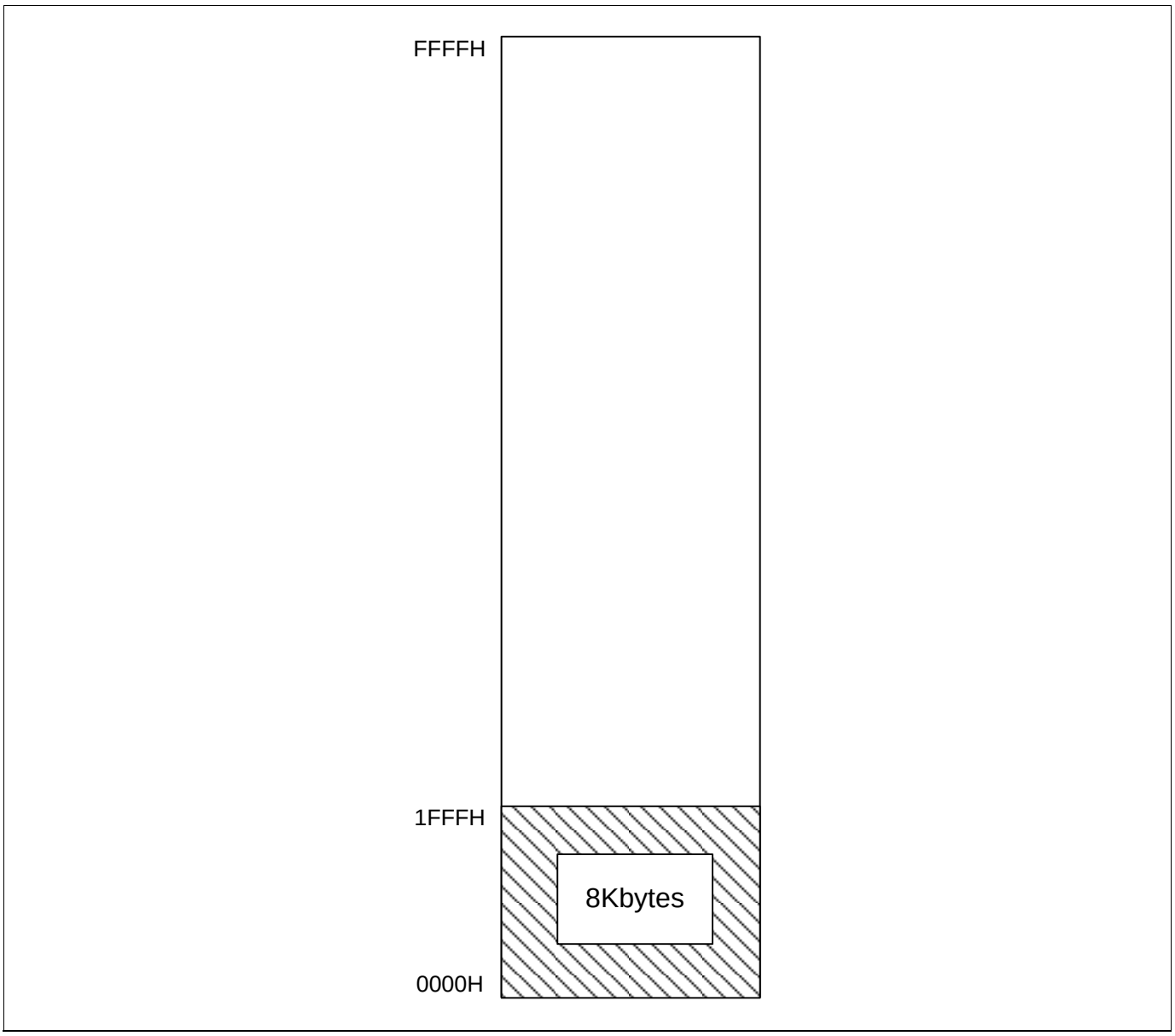


Figure 8.1 Program Memory

NOTE)

1. 8Kbytes Including Interrupt Vector Region

8.2 Data Memory

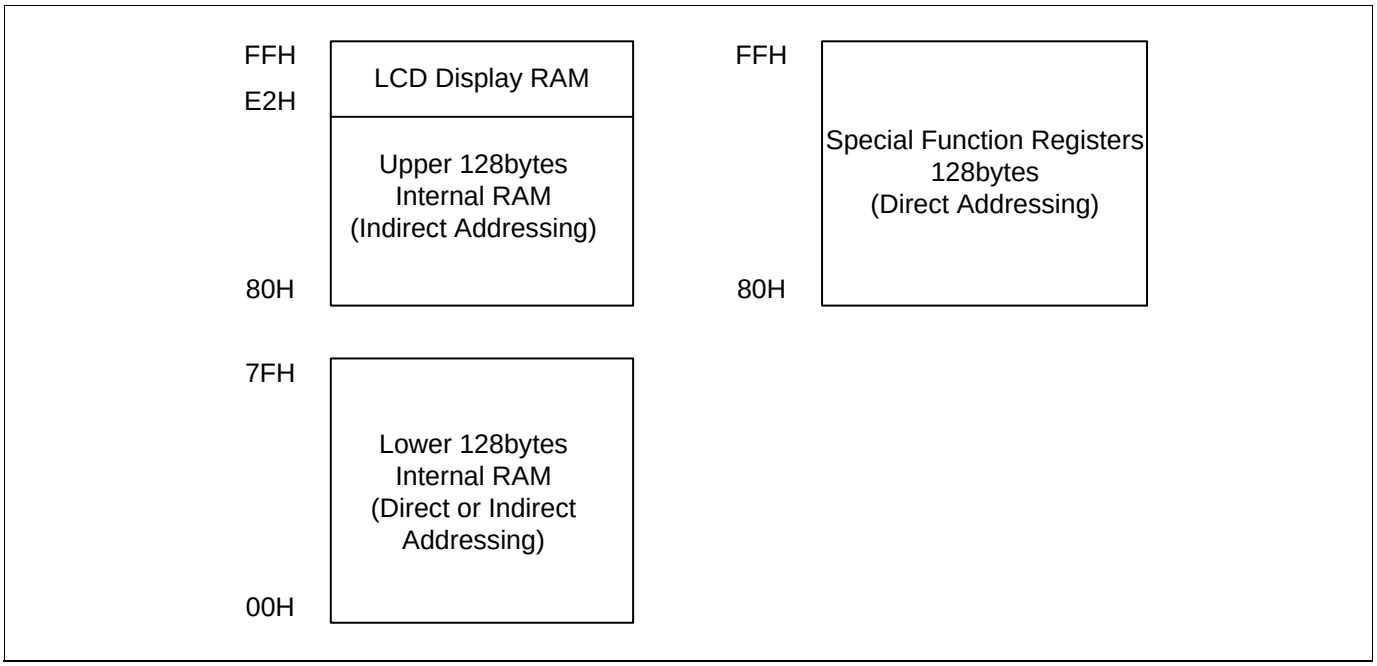


Figure 8.2 shows the internal data memory space available

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128bytes, upper 128 bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256bytes. However, in fact the addressing modes for internal RAM can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 8-2 shows the upper 128bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 8-3. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack and LCD Display RAM.

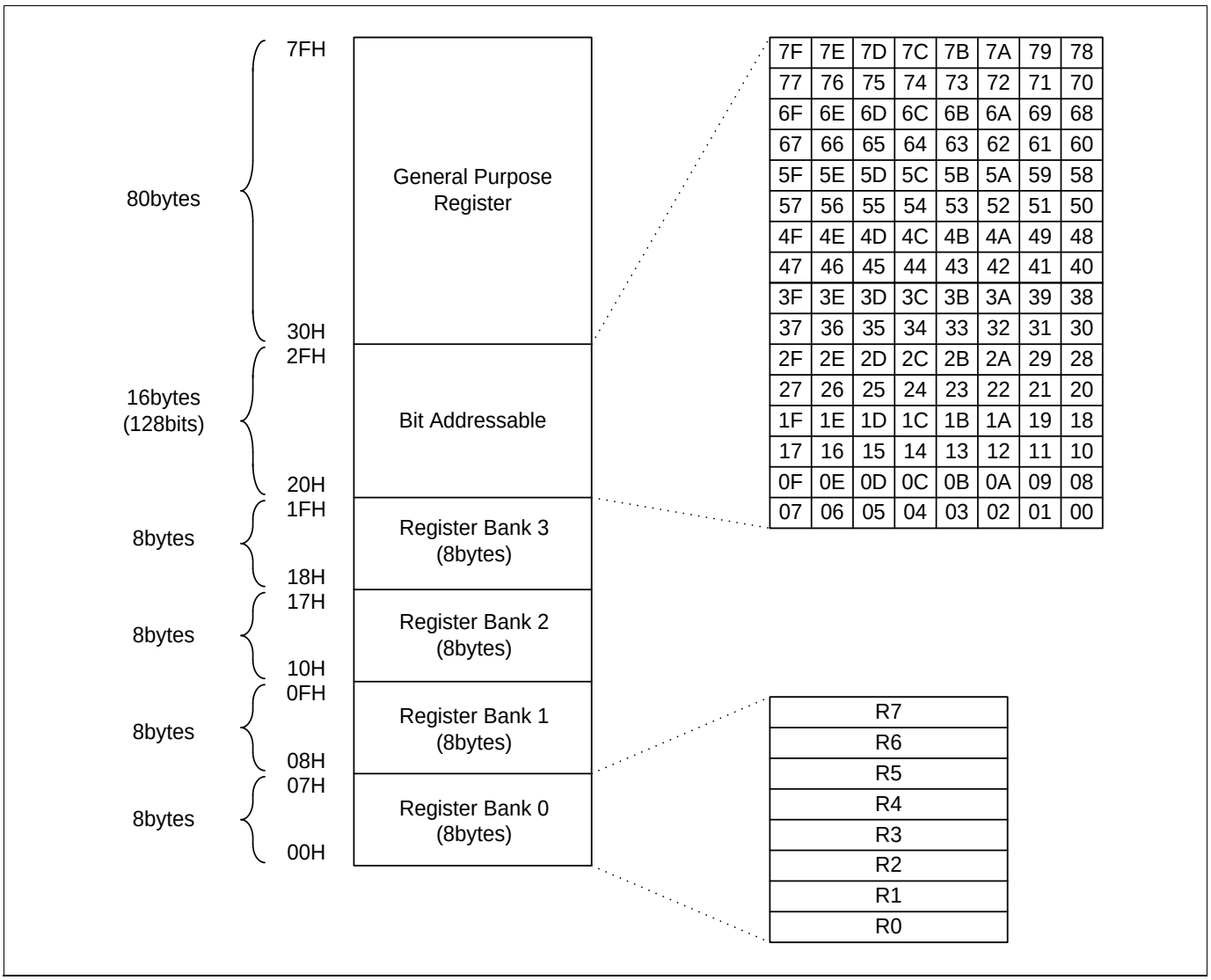


Figure 8.3 Lower 128bytes RAM

8.3 SFR Map

8.3.1 SFR Map Summary

- Reserved
M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	PLLCR
0F0H	B	P4FSR	P5FSRL	P5FSRH	P6FSR	LCDCCR	–	–
0E8H	KFLAG	P0DB	P1DB	LCDCRL	LCDCRH	P0FSR	P2FSR	P3FSR
0E0H	ACC	LVICR	UARTCR1	UARTCR2	UARTCR3	UARTST	UARTBD	UARTDR
0D8H	LVRCR	OSCCR	P4PU	P5PU	P6PU	–	–	–
0D0H	PSW	–	–	–	P0PU	P1PU	P2PU	P3PU
0C8H	–	–	T1CR	T1CNT	T1DRL	T1DRH/ T1CDR	CARCR	–
0C0H	P6	P6IO	T3CR	TIFR	T3CNT	–	T3DR/ T3CDR	–
0B8H	IP	P5IO	T2CR	–	T2CNT	–	T2DR/ T2CDR	–
0B0H	P5	P4IO	T0CR	T0CNT	T0DR/ T0CDR	SIOCR	SIODR	SIOPS
0A8H	IE	IE1	IE2	IE3	–	–	KPOL0	KPOL1
0A0H	P4	P3IO	EO	–	EIFLAG	EIPOL	–	–
98H	P3	P2IO	P5OD	P6OD	–	–	WTCR	WTDR/ WTCNT
90H	P2	P1IO	P0OD	P1OD	P2OD	P3OD	P4OD	BUZCR
88H	P1	P0IO	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	RSTFR	PCON

Table 8-1. SFR Map Summary

NOTE)

1. (1)These registers are bit-addressable.

8.3.2 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	–	–	–	–	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	P0 Direction Register	P0IO	R/W	–	–	–	–	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	–	–	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
92H	P0 Open-drain Selection Register	P0OD	R/W	–	–	–	–	0	0	0	0
93H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
94H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
95H	P3 Open-drain Selection Register	P3OD	R/W	0	0	0	0	0	0	0	0
96H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
99H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
9AH	P5 Open-drain Selection Register	P5OD	R/W	0	0	0	0	0	0	0	0
9BH	P6 Open-drain Selection Register	P6OD	R/W	–	–	–	0	0	0	0	0
9CH	Reserved	–	–	–							
9DH	Reserved	–	–	–							
9EH	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
9FH	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0

Table 8-2. SFR Decsription

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	0	0	0	0	0	0	0	0
A1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	External Interrupt Flag Register	EIFLAG	R/W	–	–	–	–	–	–	0	0
A5H	External Interrupt Polarity Register	EIPOL	R/W	–	–	–	–	0	0	0	0
A6H	Reserved	–	–	–							
A7H	Reserved	–	–	–							
A8H	Interrupt Enable Register	IE	R/W	0	–	0	–	–	0	0	–
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	–	–	–
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	–	0	0	0	0	–
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	0	–	–
ACH	Reserved	–	–	–							
ADH	Reserved	–	–	–							
AEH	Key Interrupt Polarity 0 Register	KPOL0	R/W	0	0	0	0	0	0	0	0
AFH	Key Interrupt Polarity 1 Register	KPOL1	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	0	0	0	0	0	0	0	0
B1H	P4 Direction Register	P4IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	SIO Control Register	SIOCR	R/W	0	0	0	0	0	0	0	0
B6H	SIO Data Register	SIODR	R/W	0	0	0	0	0	0	0	0
B7H	SIO Pre-scale Register	SIOPS	R/W	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P5 Direction Register	P5IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 2 Control Register	T2CR	R/W	0	–	0	0	0	0	0	0
BBH	Reserved	–	–	–							
BCH	Timer 2 Counter Register	T2CNT	R	0	0	0	0	0	0	0	0
BDH	Reserved	–	–	–							
BEH	Timer 2 Data Register	T2DR	R/W	1	1	1	1	1	1	1	1
	Timer 2 Capture Data Register	T2CDR	R	0	0	0	0	0	0	0	0
BFH	Reserved	–	–	–							

Table 8-3. SFR Decsription (continue)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	P6 Data Register	P6	R/W	–	–	–	0	0	0	0	0
C1H	P6 Direction Register	P6IO	R/W	–	–	–	0	0	0	0	0
C2H	Timer 3 Control Register	T3CR	R/W	0	0	–	0	0	0	0	0
C3H	Timer Interrupt Flag Register	TIFR	R/W	0	–	–	–	0	0	0	0
C4H	Timer 3 Counter Register	T3CNT	R	0	0	0	0	0	0	0	0
C5H	Reserved	–	–	–							
C6H	Timer 3 Data Register	T3DR	R/W	1	1	1	1	1	1	1	1
	Timer 3 Capture Data Register	T3CDR	R	0	0	0	0	0	0	0	0
C7H	Reserved	–	–	–							
C8H	Reserved	–	–	–							
C9H	Reserved	–	–	–							
CAH	Timer 1 Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
CBH	Timer 1 Counter Register	T1CNT	R	0	0	0	0	0	0	0	0
CCH	Timer 1 Data Low Register	T1DRL	R/W	1	1	1	1	1	1	1	1
CDH	Timer 1 Data High Register	T1DRH	R/W	1	1	1	1	1	1	1	1
	Timer 1 Capture Data Register	T1CDR	R	0	0	0	0	0	0	0	0
CEH	Carrier Mode Control Register	CARCR	R/W	–	–	0	0	–	–	0	0
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	P0 Pull-up Resistor Selection Register	P0PU	R/W	–	–	–	–	0	0	0	0
D5H	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
D6H	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
D7H	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	0	–	–	0	0	0	0	0
D9H	Oscillator Control Register	OSCCR	R/W	–	–	0	0	1	0	0	0
DAH	P4 Pull-up Resistor Selection Register	P4PU	R/W	0	0	0	0	0	0	0	0
DBH	P5 Pull-up Resistor Selection Register	P5PU	R/W	0	0	0	0	0	0	0	0
DCH	P6 Pull-up Resistor Selection Register	P6PU	R/W	–	–	–	0	0	0	0	0
DDH	Reserved	–	–	–							
DEH	Reserved	–	–	–							
DFH	Reserved	–	–	–							

Table 8-4. SFR Description (continue)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
E2H	UART Control Register 1	UARTCR1	R/W	–	–	0	0	0	0	0	–
E3H	UART Control Register 2	UARTCR2	R/W	0	0	0	0	0	0	0	0
E4H	UART Control Register 3	UARTCR3	R/W	–	0	–	–	–	0	0	0
E5H	UART Status Register	UARTST	R/W	1	0	0	0	0	0	0	0
E6H	UART Baud Rate Generation Register	UARTBD	R/W	1	1	1	1	1	1	1	1
E7H	UART Data Register	UARTDR	R/W	0	0	0	0	0	0	0	0
E8H	Key Interrupt Flag Register	KFLAG	R/W	0	0	0	0	0	0	0	0
E9H	P0 De-bounce Enable Register	P0DB	R/W	0	0	–	–	–	–	0	0
EAH	P1 De-bounce Enable Register	P1DB	R/W	0	0	0	0	0	0	0	0
EBH	LCD Driver Control Low Register	LCDCRL	R/W	0	–	0	0	0	0	0	0
ECH	LCD Driver Control High Register	LCDCRH	R/W	–	–	–	–	–	–	–	0
EDH	Port 0 Function Selection Register	P0FSR	R/W	–	–	–	–	–	0	0	0
EEH	Port 2 Function Selection Register	P2FSR	R/W	0	0	0	0	0	0	0	0
EFH	Port 3 Function Selection Register	P3FSR	R/W	0	0	0	0	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Port 4 Function Selection Register	P4FSR	R/W	0	0	0	0	0	0	0	0
F2H	Port 5 Function Selection Low Register	P5FSRL	R/W	–	–	–	–	0	0	0	0
F3H	Port 5 Function Selection High Register	P5FSRH	R/W	–	0	0	0	0	0	0	0
F4H	Port 6 Function Selection Register	P6FSR	R/W	–	–	–	0	0	0	0	0
F5H	LCD Contrast Control Register	LCDCCR	R/W	0	–	–	–	0	0	0	0
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0
FFH	Phase Locked Loop Control Register	PLLCR	R/W	–	–	0	0	0	0	0	0

Table 8-5. SFR Description (continue)

8.3.3 Compiler Compatible SFR

ACC (Accumulator Register): E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ACC	Accumulator

B (B Register): F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

B	B Register

SP (Stack Pointer): 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 07H

SP	Stack Pointer

DPL (Data Pointer Register Low): 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL	Data Pointer Low Byte

DPH (Data Pointer Register High): 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH	Data Pointer High Byte

DPL1 (Data Pointer Register Low 1): 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL1 Data Pointer Low 1 Byte

DPH1 (Data Pointer Register High 1): 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH1 Data Pointer High 1 Byte

PSW (Program Status Word Register): D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CY Carry Flag

AC Auxiliary Carry Flag

F0 General Purpose User-Definable Flag

RS1 Register Bank Select bit 1

RS0 Register Bank Select bit 0

OV Overflow Flag

F1 User-Definable Flag

P Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator

EO (Extended Operation Register):A2H

7	6	5	4	3	2	1	0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value:00H

TRAP_EN Select the Instruction **(Keep always '0')**.

0 Select MOVC @(DPTR++), A

1 Select Software TRAP Instruction

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	SPSEL0	Description
0	0	0	DPTR0
0	0	1	DPTR1
Reserved			

9 I/O Ports

9.1 I/O Ports

The MC96F6508A has seven groups of I/O ports (P0 ~ P6). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. Also P1, P00 and P01 includes function that can generate interrupt according to change of state of the pin.

9.2 Port Register

9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

9.2.2 Direction Register (PxIO)

Each I/O pin can be independently used as an input or an output through the PxIO register. Bits cleared in this register will make the corresponding pin ofPx to input mode. Set bits of this register will make the pin to output mode. Almost bits are cleared by a system reset, but some bits are set by a system reset.

9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to I/O ports individually with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset.

9.2.4 Open-drain Selection Register (PxOD)

There are internally open-drain selection registers (PxOD) for P0 ~ P6. The open-drain selection register controls the open-drain enable/disable of each port. Almost ports become push-pull by a system reset, but some ports become open-drain by a system reset.

9.2.5 De-bounce Enable Register (PxDB)

P1[0:7], P00, and P01 support debounce function. Debounce clocks of each ports are fx/1, fx/4, and fx/4096.

9.2.6 Port Function Selection Register (PxFSR)

These registers define alternative functions of ports. Please remember that these registers should be set properly for alternative port function. A reset clears the PxFSR register to ‘00H’, which makes all pins to normal I/O ports.

9.2.7 Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	89H	R/W	00H	P0 Direction Register
P0PU	D4H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	92H	R/W	00H	P0 Open-drain Selection Register
P0DB	E9H	R/W	00H	P0 De-bounce Enable Register
P0FSR	EDH	R/W	00H	Port 0 Function Selection Register
P1	88H	R/W	00H	P1 Data Register
P1IO	91H	R/W	00H	P1 Direction Register
P1PU	D5H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	93H	R/W	00H	P1 Open-drain Selection Register
P1DB	EAH	R/W	00H	P1 De-bounce Enable Register
P2	90H	R/W	00H	P2 Data Register
P2IO	99H	R/W	00H	P2 Direction Register
P2PU	D6H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	94H	R/W	00H	P2 Open-drain Selection Register
P2FSR	EEH	R/W	00H	Port 2 Function Selection Register
P3	98H	R/W	00H	P3 Data Register
P3IO	A1H	R/W	00H	P3 Direction Register
P3PU	D7H	R/W	00H	P3 Pull-up Resistor Selection Register
P3OD	95H	R/W	00H	P3 Open-drain Selection Register
P3FSR	EFH	R/W	00H	Port 3 Function Selection Register
P4	A0H	R/W	00H	P4 Data Register
P4IO	B1H	R/W	00H	P4 Direction Register
P4PU	DAH	R/W	00H	P4 Pull-up Resistor Selection Register
P4OD	96H	R/W	00H	P4 Open-drain Selection Register
P4FSR	F1H	R/W	00H	Port 4 Function Selection Register
P5	B0H	R/W	00H	P5 Data Register
P5IO	B9H	R/W	00H	P5 Direction Register
P5PU	DBH	R/W	00H	P5 Pull-up Resistor Selection Register
P5OD	9AH	R/W	00H	P5 Open-drain Selection Register
P5FSRH	F3H	R/W	00H	Port 5 Function Selection High Register
P5FSRL	F2H	R/W	00H	Port 5 Function Selection Low Register
P6	C0H	R/W	00H	P6 Data Register
P6IO	C1H	R/W	00H	P6 Direction Register
P6PU	DCH	R/W	00H	P6 Pull-up Resistor Selection Register
P6OD	9BH	R/W	00H	P6 Open-drain Selection Register
P6FSR	F4H	R/W	00H	Port 6 Function Selection Register

Table 9-1. Port Register Map

9.3 P0 Port

9.3.1 P0 Port Description

P0 is 4-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), P0 open-drain selection register (P0OD), and port 0 function selection register (P0FSR).

9.3.2 Register description for P0

P0 (P0 Data Register) : 80H

7	6	5	4	3	2	1	0
–	–	–	–	P03	P02	P01	P00
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P0[3:0] I/O Data

P0IO (P0 Direction Register) :89H

7	6	5	4	3	2	1	0
–	–	–	–	P03IO	P02IO	P01IO	P00IO
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P0IO[3:0] P0 Data I/O Direction.

0 Input

1 Output

NOTE)

1. EINT10/EINT12/EC2 function possible when input.

P0PU (P0 Pull-up Resistor Selection Register) :D4H

7	6	5	4	3	2	1	0
–	–	–	–	P03PU	P02PU	P01PU	P00PU
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P0PU[3:0] Configure Pull-up Resistor of P0 Port

0 Disable

1 Enable

P0OD (P0 Open-drain Selection Register) :92H

7	6	5	4	3	2	1	0
–	–	–	–	P03OD	P02OD	P01OD	P00OD
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P0OD[3:0] Configure Open-drain of P0 Port

0 Push-pull output

1 Open-drain output

P0DB (P0 De-bounce Enable Register) :E9H

7	6	5	4	3	2	1	0
DBCLK1	DBCLK0	–	–	–	–	P01DB	P00DB
R/W	R/W	–	–	–	–	R/W	R/W

Initial value :00H

DBCLK[1:0] Configure De-bounce Clock of Port

DBCLK1	DBCLK0	Description
0	0	fx/1(NOTE1)
0	1	fx/4
1	0	fx/4096
1	1	Reserved

P01DB Configure De-bounce of P01 Port

0	Disable
1	Enable

P00DB Configure De-bounce of P00 Port

0	Disable
1	Enable

NOTE)

1. "DBCLK[1:0] = 00b" setting(De-bounce clock of port = fx/1) should not use during IDLE mode.
2. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
3. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.
4. The port de-bounce is automatically disabled at stop mode and recovered after stop mode release.

P0FSR (Port 0 Function Selection Register) :EDH

7	6	5	4	3	2	1	0
–	–	–	–	–	P0FSR2	P0FSR1	P0FSR0
–	–	–	–	–	R/W	R/W	R/W

Initial value :00H

P0FSR2 P03 Function Select

0	I/O Port
1	REM Function

P0FSR1 P02 Function Select

0	I/O Port
1	BUZO Function

P0FSR0 P01 Function Select

0	I/O Port
1	T2O Function

9.4 P1 Port

9.4.1 P1 Port Description

P1 is 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), andP1 open-drain selection register (P1OD) .

9.4.2 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P1[7:0] I/O Data

P1IO (P1 Direction Register) :91H

7	6	5	4	3	2	1	0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P1IO[7:0] P1 Data I/O Direction

0 Input

1 Output

NOTE)

1. KEY0 – KEY7 function possible when input.

P1PU (P1 Pull-up Resistor Selection Register) :D5H

7	6	5	4	3	2	1	0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P1PU[7:0] Configure Pull-up Resistor of P1 Port

0 Disable

1 Enable

P1OD (P1 Open-drain Selection Register) : 93H

7	6	5	4	3	2	1	0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P1OD[7:0] Configure Open-drain of P1 Port

0 Push-pull output

1 Open-drain output

P1DB (P1 De-bounce Enable Register): EAH

7	6	5	4	3	2	1	0
P17DB	P16DB	P15DB	P14DB	P13DB	P12DB	P11DB	P10DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1DB[7:0] Configure De-bounce of P1 Port

0 Disable

1 Enable

NOTE)

1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.
3. The port de-bounce is automatically disabled at stop mode and recovered after stop mode release.
4. Refer to the port 0 de-bounce enable register (P0DB) for the de-bounce clock of port 1.

9.5 P2 Port

9.5.1 P2 Port Description

P2 is 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU),P2 open-drain selection register (P2OD), and port 2 function selection register (P2FSR)

9.5.2 9.5.2 Register description for P2

P2 (P2 Data Register) : 90H

7	6	5	4	3	2	1	0
P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P2[7:0] I/O Data

P2IO (P2 Direction Register) : 99H

7	6	5	4	3	2	1	0
P27IO	P26IO	P25IO	P24IO	P23IO	P22IO	P21IO	P20IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P2IO[7:0] P2 Data I/O Direction

0 Input

1 Output

P2PU (P2 Pull-up Resistor Selection Register) :D6H

7	6	5	4	3	2	1	0
P27PU	P26PU	P25PU	P24PU	P23PU	P22PU	P21PU	P20PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P2PU[7:0] Configure Pull-up Resistor of P2 Port

0 Disable

1 Enable

P2OD (P2 Open-drain Selection Register) :94H

7	6	5	4	3	2	1	0
P27OD	P26OD	P25OD	P24OD	P23OD	P22OD	P21OD	P20OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P2OD[7:0] Configure Open-drain of P2 Port

0 Push-pull output

1 Open-drain output

P2FSR (Port 2 Function Selection Register) :EEH

7	6	5	4	3	2	1	0
P2FSR7	P2FSR6	P2FSR5	P2FSR4	P2FSR3	P2FSR2	P2FSR1	P2FSR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value :00H

P2FSR7 P27 Function select
- 0 I/O Port
- 1 COM7/SEG5 Function

P2FSR6 P26 Function select
- 0 I/O Port
- 1 COM6/SEG4 Function

P2FSR5 P25 Function select
- 0 I/O Port
- 1 COM5/SEG3 Function

P2FSR4 P24 Function select
- 0 I/O Port
- 1 COM4/SEG2 Function

P2FSR3 P23 Function select
- 0 I/O Port
- 1 COM3/SEG1 Function

P2FSR2 P22 Function select
- 0 I/O Port
- 1 COM2/SEG0 Function

P2FSR1 P21 Function select
- 0 I/O Port
- 1 COM1 Function

P2FSR0 P20 Function select
- 0 I/O Port
- 1 COM0 Function

NOTE)

1. The P22-P27 is automatically configured as common or segment signal according to the duty in the LCDCRL register when the pin is selected as the sub-function for common/segment.

9.6 P3 Port

9.6.1 P3 Port Description

P3 is 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO), P3 pull-up resistor selection register (P3PU),P3 open-drain selection register (P3OD), and port 3 function selection register (P3FSR)

9.6.2 Register description for P3

P3 (P3 Data Register) : 98H

7	6	5	4	3	2	1	0
P37	P36	P35	P34	P33	P32	P31	P30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P3[7:0] I/O Data

P3IO (P3 Direction Register) : A1H

7	6	5	4	3	2	1	0
P37IO	P36IO	P35IO	P34IO	P33IO	P32IO	P31IO	P30IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P3IO[7:0] P3 Data I/O Direction

0 Input

1 Output

P3PU (P3 Pull-up Resistor Selection Register) :D7H

7	6	5	4	3	2	1	0
P37PU	P36PU	P35PU	P34PU	P33PU	P32PU	P31PU	P30PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P3PU[7:0] Configure Pull-up Resistor of P3 Port

0 Disable

1 Enable

P3OD (P3 Open-drain Selection Register) :95H

7	6	5	4	3	2	1	0
P37OD	P36OD	P35OD	P34OD	P33OD	P32OD	P31OD	P30OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P3OD[7:0] Configure Open-drain of P3 Port

0 Push-pull output

1 Open-drain output

P3FSR (Port 3 Function Selection Register) :EFH

7	6	5	4	3	2	1	0
P3FSR7	P3FSR6	P3FSR5	P3FSR4	P3FSR3	P3FSR2	P3FSR1	P3FSR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value :00H

P3FSR7 P37 Function select
- 0 I/O Port
- 1 SEG13 Function

P3FSR6 P36 Function select
- 0 I/O Port
- 1 SEG12 Function

P3FSR5 P35 Function select
- 0 I/O Port
- 1 SEG11 Function

P3FSR4 P34 Function select
- 0 I/O Port
- 1 SEG10 Function

P3FSR3 P33 Function select
- 0 I/O Port
- 1 SEG9 Function

P3FSR2 P32 Function select
- 0 I/O Port
- 1 SEG8 Function

P3FSR1 P31 Function select
- 0 I/O Port
- 1 SEG7 Function

P3FSR0 P30 Function select
- 0 I/O Port
- 1 SEG6 Function

9.7 P4 Port

9.7.1 P4 Port Description

P4 is 8-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO), P4 pull-up resistor selection register (P4PU), P4 open-drain selection register (P4OD), and port 4 function selection register (P4FSR)

9.7.2 Register description for P4

P4 (P4 Data Register) :A0H

7	6	5	4	3	2	1	0
P47	P46	P45	P44	P43	P42	P41	P40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P4[7:0] I/O Data

P4IO (P4 Direction Register) : B1H

7	6	5	4	3	2	1	0
P47IO	P46IO	P45IO	P44IO	P43IO	P42IO	P41IO	P40IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P4IO[7:0] P4 Data I/O Direction

0 Input

1 Output

P4PU (P4 Pull-up Resistor Selection Register) :DAH

7	6	5	4	3	2	1	0
P47PU	P46PU	P45PU	P44PU	P43PU	P42PU	P41PU	P40PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P4PU[7:0] Configure Pull-up Resistor of P4 Port

0 Disable

1 Enable

P4OD (P4 Open-drain Selection Register) :96H

7	6	5	4	3	2	1	0
P47OD	P46OD	P45OD	P44OD	P43OD	P42OD	P41OD	P40OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P4OD[7:0] Configure Open-drain of P4 Port

0 Push-pull output

1 Open-drain output

P4FSR (Port 4 Function Selection Register) :F1H

7	6	5	4	3	2	1	0
P4FSR7	P4FSR6	P4FSR5	P4FSR4	P4FSR3	P4FSR2	P4FSR1	P4FSR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value :00H

P4FSR7 P47 Function select
- 0 I/O Port
- 1 SEG21 Function

P4FSR6 P46 Function select
- 0 I/O Port
- 1 SEG20 Function

P4FSR5 P45 Function select
- 0 I/O Port
- 1 SEG19 Function

P4FSR4 P44 Function select
- 0 I/O Port
- 1 SEG18 Function

P4FSR3 P43 Function select
- 0 I/O Port
- 1 SEG17 Function

P4FSR2 P42 Function select
- 0 I/O Port
- 1 SEG16 Function

P4FSR1 P41 Function select
- 0 I/O Port
- 1 SEG15 Function

P4FSR0 P40 Function select
- 0 I/O Port
- 1 SEG14 Function

9.8 P5 Port

9.8.1 P5 Port Description

P5 is 8-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO), P5 pull-up resistor selection register (P5PU), P5 open-drain selection register (P5OD), and port 5 function selection high/low register (P5FSRH/P5FSRL)

9.8.2 Register description for P5

P5 (P5 Data Register) :B0H

7	6	5	4	3	2	1	0
P57	P56	P55	P54	P53	P52	P51	P50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P5[7:0] I/O Data

P5IO (P5 Direction Register) : B9H

7	6	5	4	3	2	1	0
P57IO	P56IO	P55IO	P54IO	P53IO	P52IO	P51IO	P50IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P5IO[7:0] P5 Data I/O Direction

0 Input

1 Output

NOTE)

1. EC0/SI/SCK-in/RXD function possible when input.

P5PU (P5 Pull-up Resistor Selection Register) :DBH

7	6	5	4	3	2	1	0
P57PU	P56PU	P55PU	P54PU	P53PU	P52PU	P51PU	P50PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P5PU[7:0] Configure Pull-up Resistor of P5 Port

0 Disable

1 Enable

P5OD (P5 Open-drain Selection Register) :9AH

7	6	5	4	3	2	1	0
P57OD	P56OD	P55OD	P54OD	P53OD	P52OD	P51OD	P50OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P5OD[7:0] Configure Open-drain of P5 Port

0 Push-pull output

1 Open-drain output

P5FSRH (Port 5 Function Selection High Register) :F3H

7	6	5	4	3	2	1	0
–	P5FSRH6	P5FSRH5	P5FSRH4	P5FSRH3	P5FSRH2	P5FSRH1	P5FSRH0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P5FSRH[6:5] P57 Function select

P5FSRH6	P5FSRH5	Description
0	0	I/O Port (RXD function possible when input)
0	1	SO Function
1	0	SEG29 Function
1	1	Not used

P5FSRH[4:3] P56 Function select

P5FSRH4	P5FSRH3	Description
0	0	I/O Port (SCK-in function possible when input)
0	1	SCK-out Function
1	0	SEG28 Function
1	1	TXD Function

P5FSRH2 P55 Function select

0	I/O Port (SI function possible when input)
1	SEG27 Function

P5FSRH[1:0] P54 Function select

P5FSRH1	P5FSRH0	Description
0	0	I/O Port (EC0 function possible when input)
0	1	T0O Function
1	0	SEG26 Function
1	1	Not used

P5FSRL (Port 5 Function Selection Low Register) :F2H

7	6	5	4	3	2	1	0
–	–	–	–	P5FSRL3	P5FSRL2	P5FSRL1	P5FSRL0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P5FSRL3 P53 Function select
- 0 I/O Port
- 1 SEG25 Function

P5FSRL2 P52 Function select
- 0 I/O Port
- 1 SEG24 Function

P5FSRL1 P51 Function select
- 0 I/O Port
- 1 SEG23 Function

P5FSRL0 P50 Function select
- 0 I/O Port
- 1 SEG22 Function

9.9 P6 Port

9.9.1 P6 Port Description

P6 is 6-bit I/O port. P6 control registers consist of P6 data register (P6), P6 direction register (P6IO), P6 pull-up resistor selection register (P6PU), P6 open-drain selection register (P6OD),and port 6 function selection register (P6FSR)

9.9.2 Register description for P6

P6 (P6 Data Register) :C0H

7	6	5	4	3	2	1	0
–	–	–	P64	P63	P62	P61	P60
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P6[4:0] I/O Data

P6IO (P6 Direction Register) : C1H

7	6	5	4	3	2	1	0
–	–	–	P64IO	P63IO	P62IO	P61IO	P60IO
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P6IO[4:0] P6 Data I/O Direction

0 Input

1 Output

P6PU (P6 Pull-up Resistor Selection Register) :DCH

7	6	5	4	3	2	1	0
–	–	–	P64PU	P63PU	P62PU	P61PU	P60PU
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P6PU[4:0] Configure Pull-up Resistor of P6 Port

0 Disable

1 Enable

P6OD (P6 Open-drain Selection Register) :9BH

7	6	5	4	3	2	1	0
–	–	–	P64OD	P63OD	P62OD	P61OD	P60OD
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

P6OD[4:0] Configure Open-drain of P6 Port

0 Push-pull output

1 Open-drain output

P6FSR (Port 6 Function Selection Register) :F4H

7	6	5	4	3	2	1	0
–	–	–	–	P6FSR3	P6FSR2	P6FSR1	P6FSR0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

P6FSR3 P64 Function Select
- 0 I/O Port
- 1 SXOUT Function

P6FSR2 P63 Function Select
- 0 I/O Port
- 1 SXIN Function

P6FSR1 P61 Function Select
- 0 I/O Port
- 1 XIN Function

P6FSR0 P60 Function Select
- 0 I/O Port
- 1 XOUT Function

NOTE)

1. Refer to the configure option for the P62/RESETB.

10 Interrupt Controller

10.1 Overview

The MC96F6508Asupports up to 20 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

- Receive the request from 20 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher prioritylevel is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency: 3~9 machinecycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The MC96F6508A supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Table 10-1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Interrupt Group	Highest → Lowest			
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23

Highest

Lowest

Table 10-1. Interrupt Group Priority Level

10.2 External Interrupt

The external interrupt on INT1, INT2 and INT5 pins receivevarious interrupt request depending on the external interrupt polarity register (EIPOL), key interrupt polarity 0 register (KPOL0) andkey interrupt polarity 1 register (KPOL1) as shown in Figure 10.1.The external interrupt flag register (EIFLAG) and key interrupt flag register (KFLAG) provides the status of external interrupts.

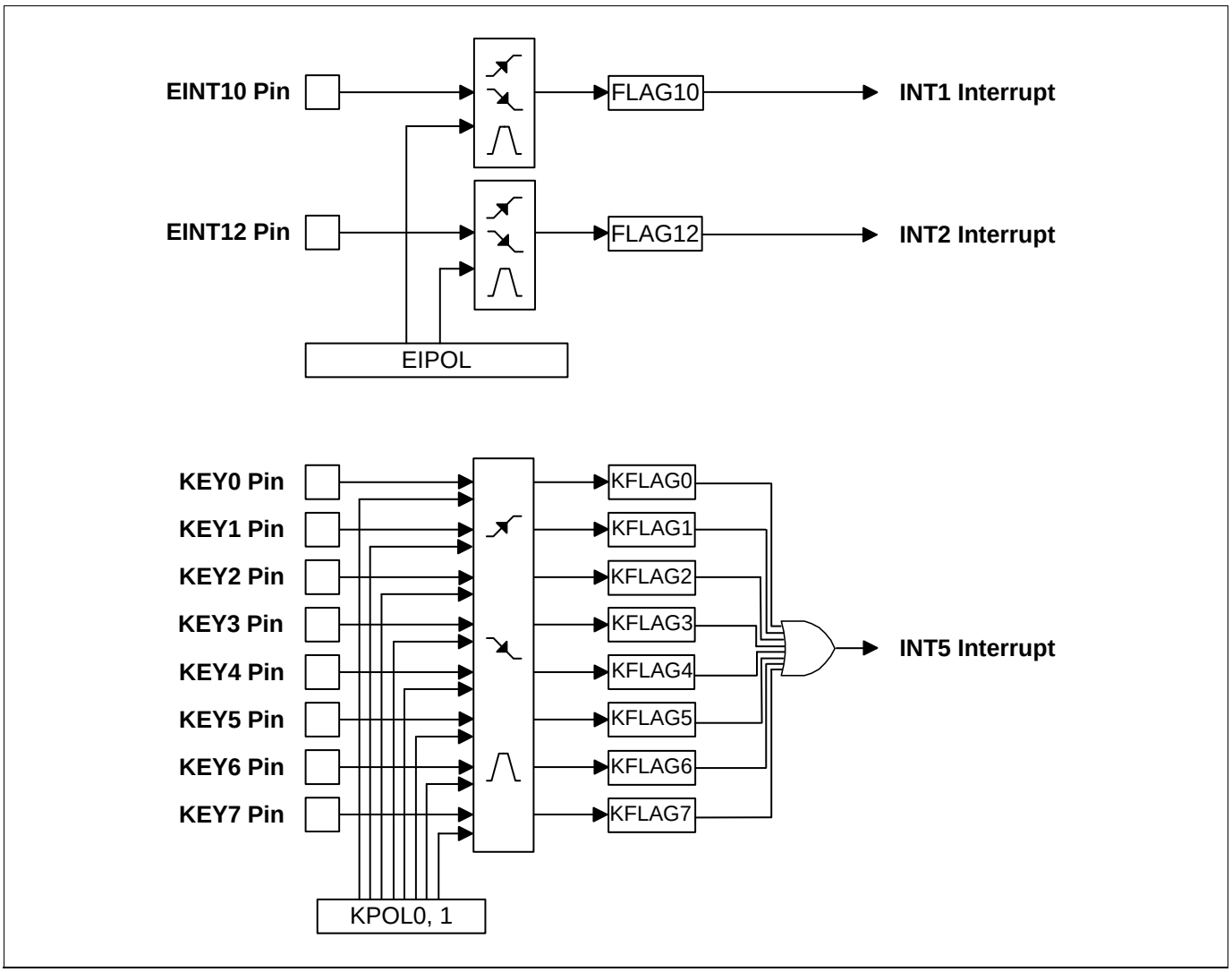


Figure 10.1 External Interrupt Description

10.3 Block Diagram

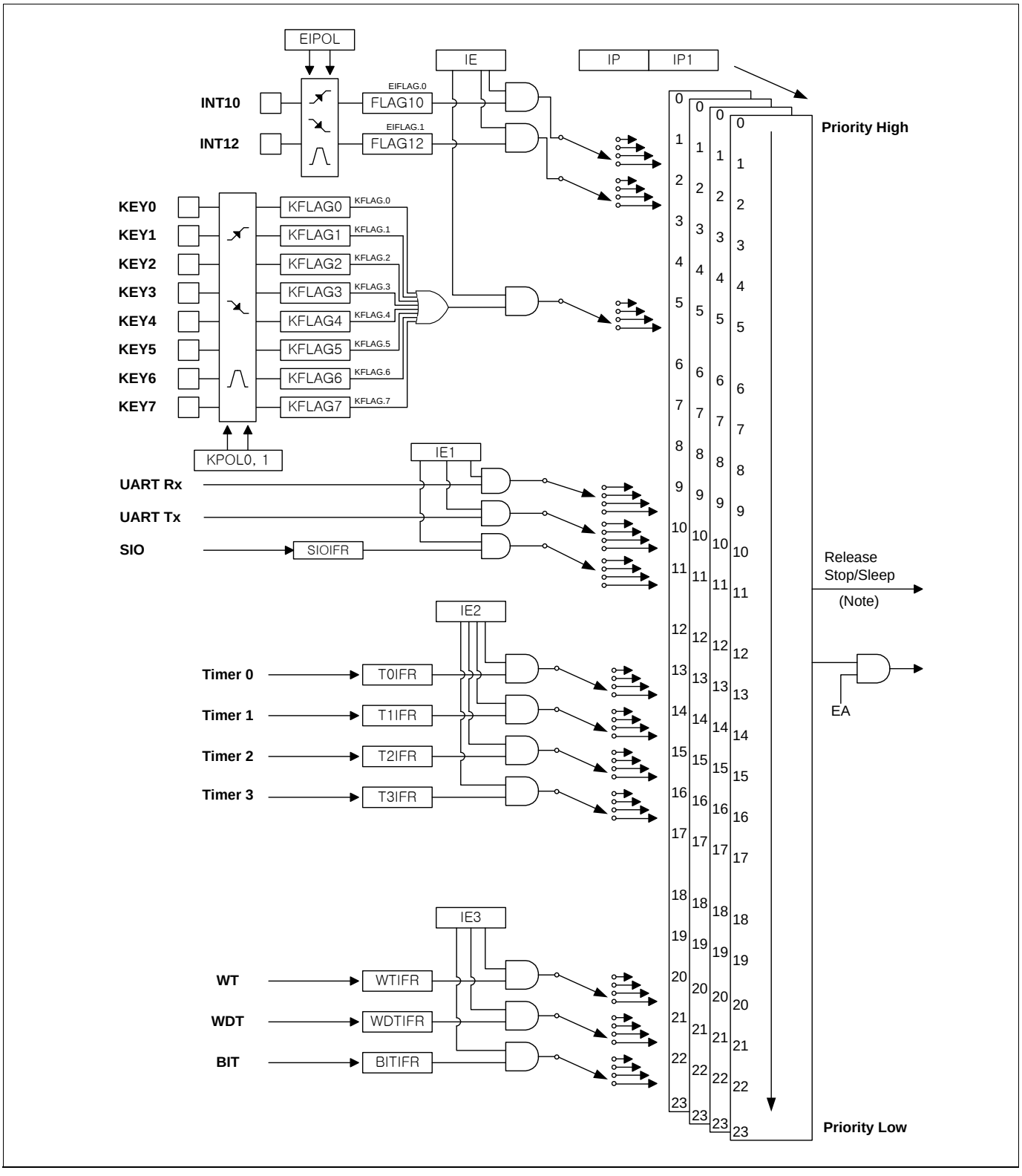


Figure 10.2 Block Diagram of Interrupt

NOTE)

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

10.4 Interrupt Vector Table

The interrupt controller supports 24 interrupt sources as shown in the Table 10-2. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	-	0	Non-Maskable	0000H
-	INT0	IE.0	1	Maskable	0003H
External Interrupt 10	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
-	INT3	IE.3	4	Maskable	001BH
-	INT4	IE.4	5	Maskable	0023H
KEY Interrupt	INT5	IE.5	6	Maskable	002BH
-	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
-	INT8	IE1.2	9	Maskable	0043H
UART Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
UART Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
SIO Interrupt	INT11	IE1.5	12	Maskable	005BH
-	INT12	IE2.0	13	Maskable	0063H
T0 Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Interrupt	INT16	IE2.4	17	Maskable	0083H
-	INT17	IE2.5	18	Maskable	008BH
-	INT18	IE3.0	19	Maskable	0093H
-	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
-	INT23	IE3.5	24	Maskable	00BBH

Table 10-2. Interrupt Vector Address Table

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to '0' by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC at stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. Since the end of the execution of current instruction, it needs 3~9 machine cycles to go to the interrupt service routine. The interrupt service task is terminated by the interrupt return instruction [RETI]. Once an interrupt request is generated, the following process is performed.

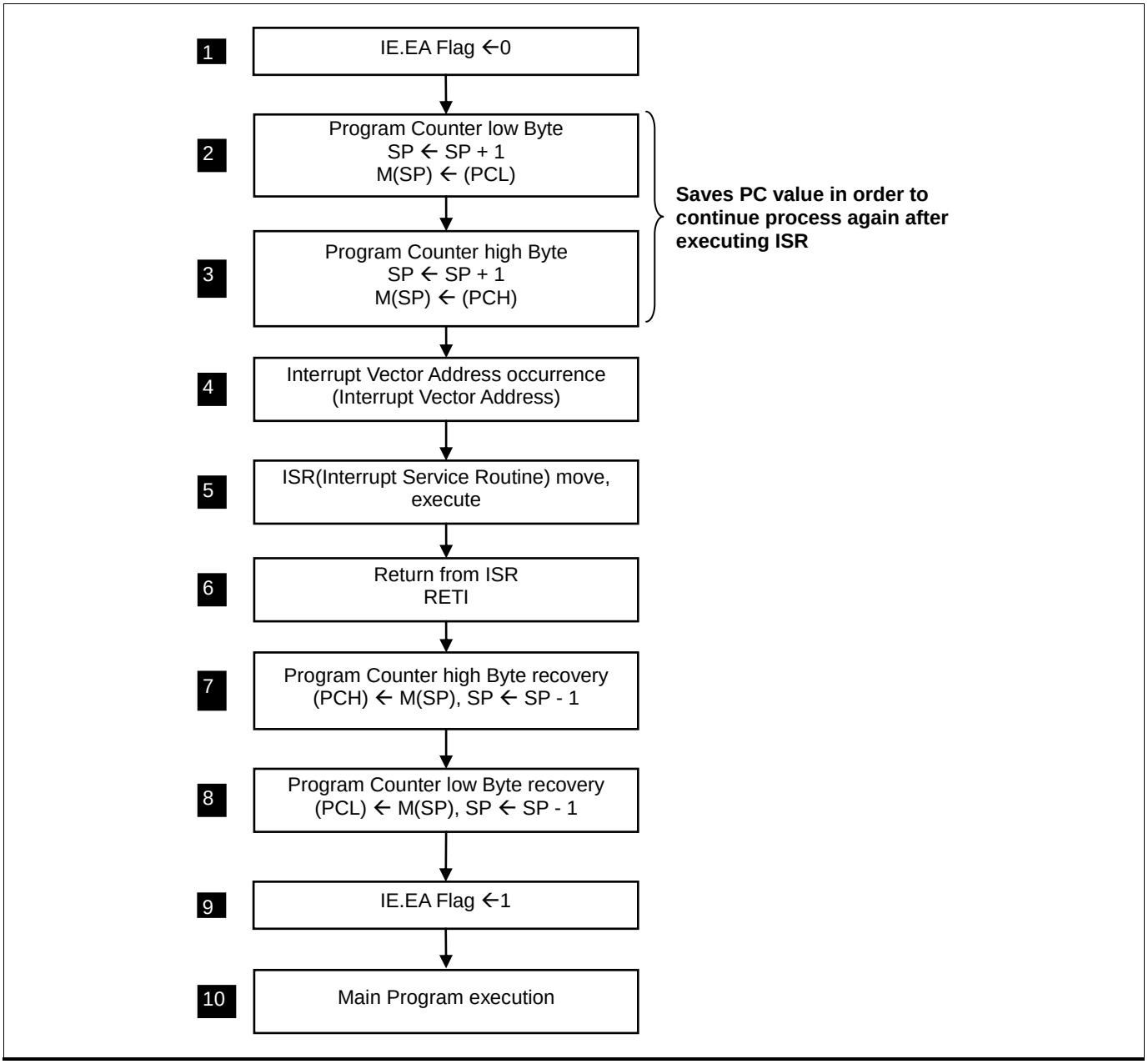


Figure 10.3 Interrupt Sequence Flow

10.6 Effective Timing after Controlling Interrupt Bit

Case a) Control Interrupt Enable Register (IE, IE1, IE2, IE3)

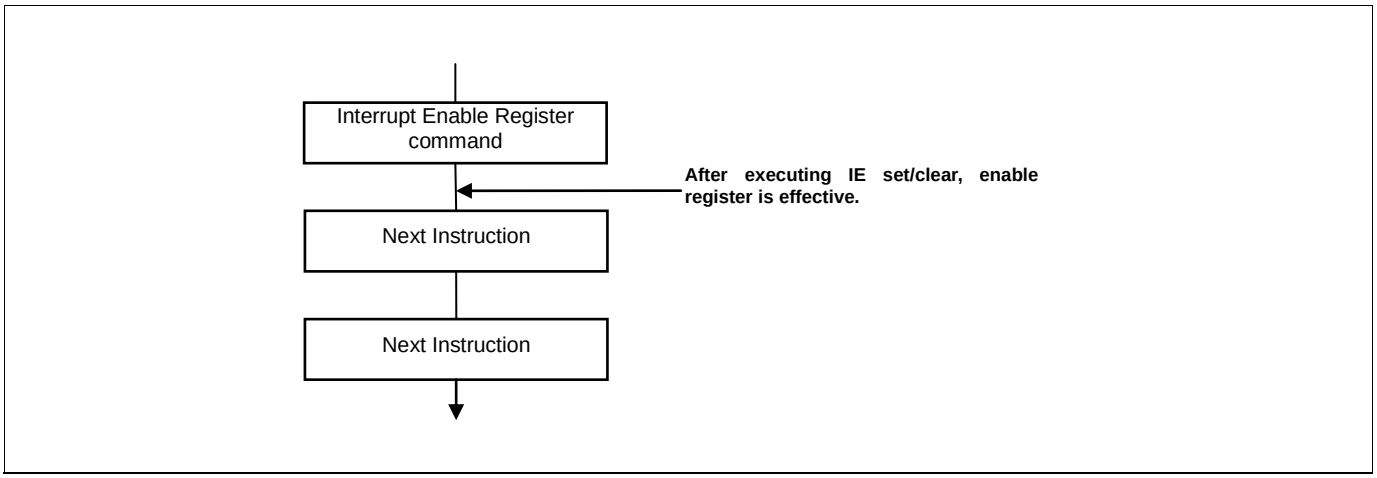


Figure 10.4 Effective Timing of Interrupt Enable Register

Case b) Interrupt flag Register

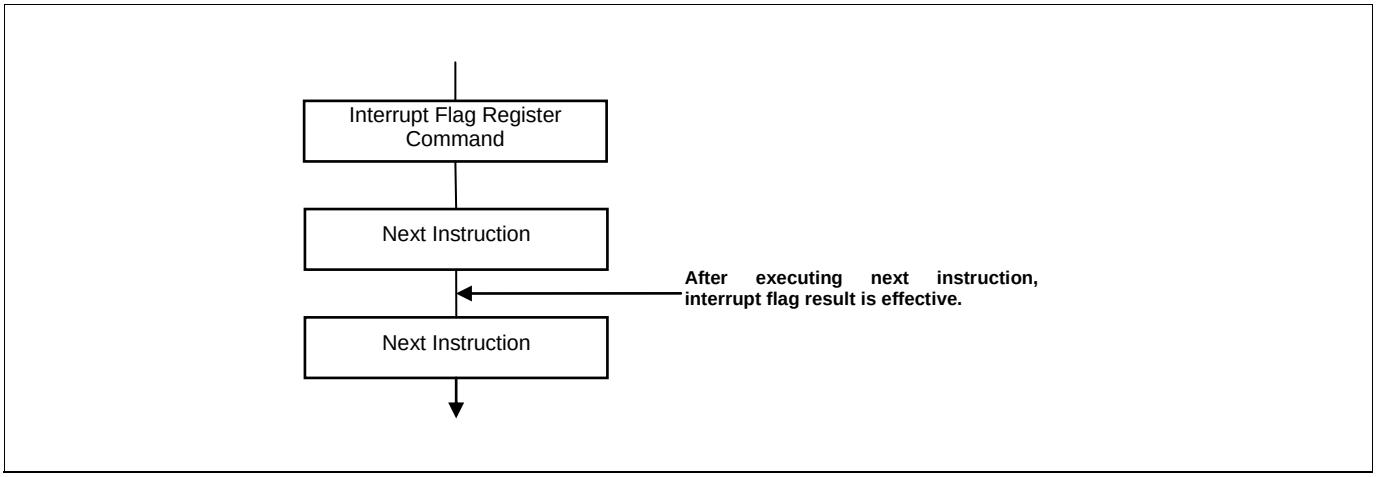


Figure 10.5 Effective Timing of Interrupt Flag Register

10.7 Multi Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is served first. If more than one interrupt request are received, the interrupt polling sequence determines which request is served first by hardware. However, for special features, multi-interrupt processing can be executed by software.

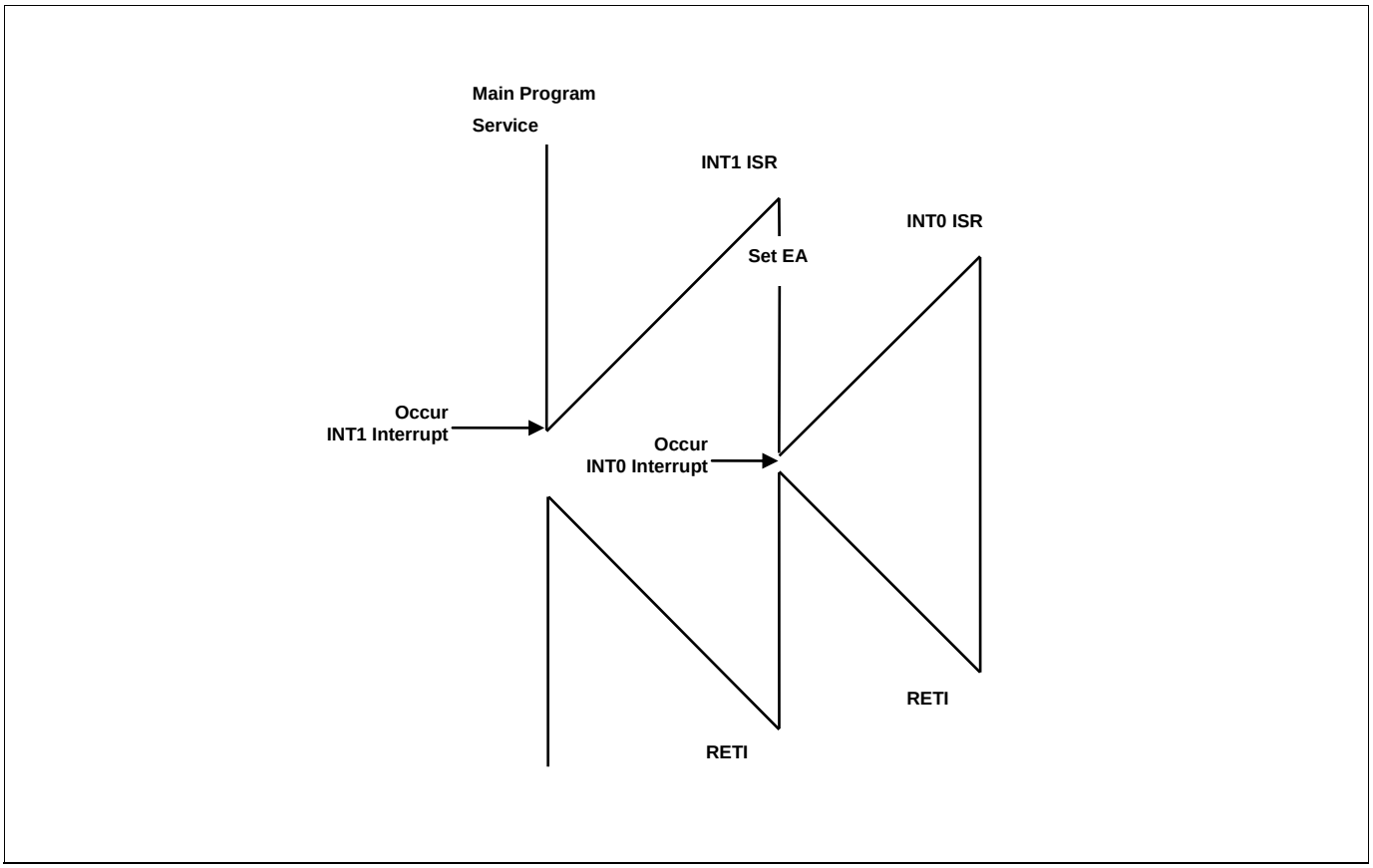


Figure 10.6 Effective Timing of Multi-Interrupt

Figure 10.6 shows an example of multi-interrupt processing. While INT1 is served, INT0 which has higher priority than INT1 is occurred. Then INT0 is served immediately and then the remain part of INT1 service routine is executed. If the priority level of INT0 is same or lower than INT1, INT0 will be served after the INT1 service has completed.

An interrupt service routine may be only interrupted by an interrupt of higher priority and, if two interrupts of different priorityoccur at the same time, the higher level interrupt will be served first. An interrupt cannot be interrupted by another interrupt ofthe same or a lower priority level. If two interrupts of the same priority level occur simultaneously, the service order for those interrupts is determined by the scan order.

10.8 Interrupt Enable Accept Timing

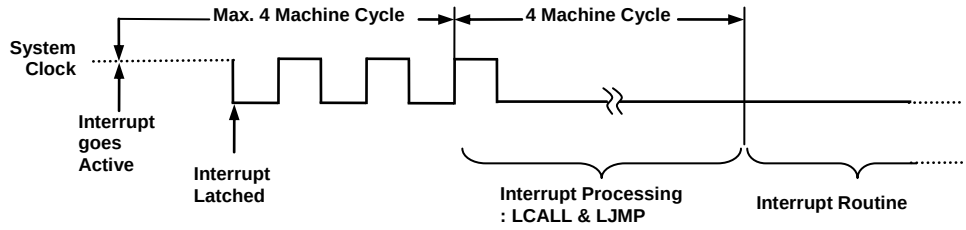


Figure 10.7 Interrupt Response Timing Diagram

10.9 Interrupt Service Routine Address

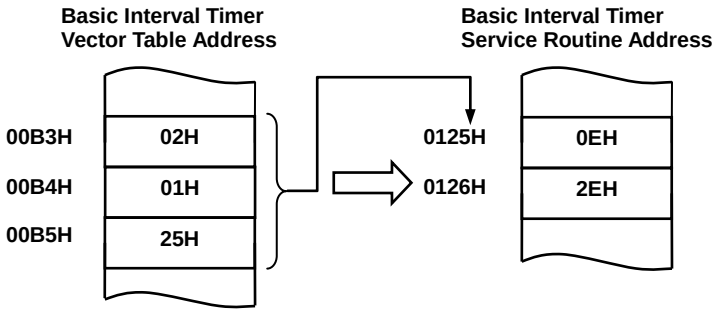


Figure 10.8 Correspondence between Vector Table Address and the Entry Address of ISR

10.10 Saving/Restore General-Purpose Registers

```
INTxx :  PUSH  PSW
         PUSH  DPL
         PUSH  DPH
         PUSH  B
         PUSH  ACC
         :


Interrupt_Processing:
         .
         .
         POP  ACC
         POP  B
         POP  DPH
         POP  DPL
         POP  PSW
         RETI
```

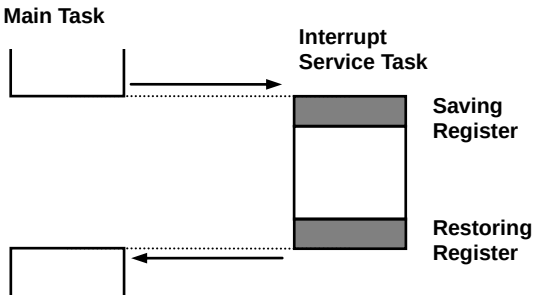


Figure 10.9 Saving/Restore Process Diagram and Sample Source

10.11 Interrupt Timing

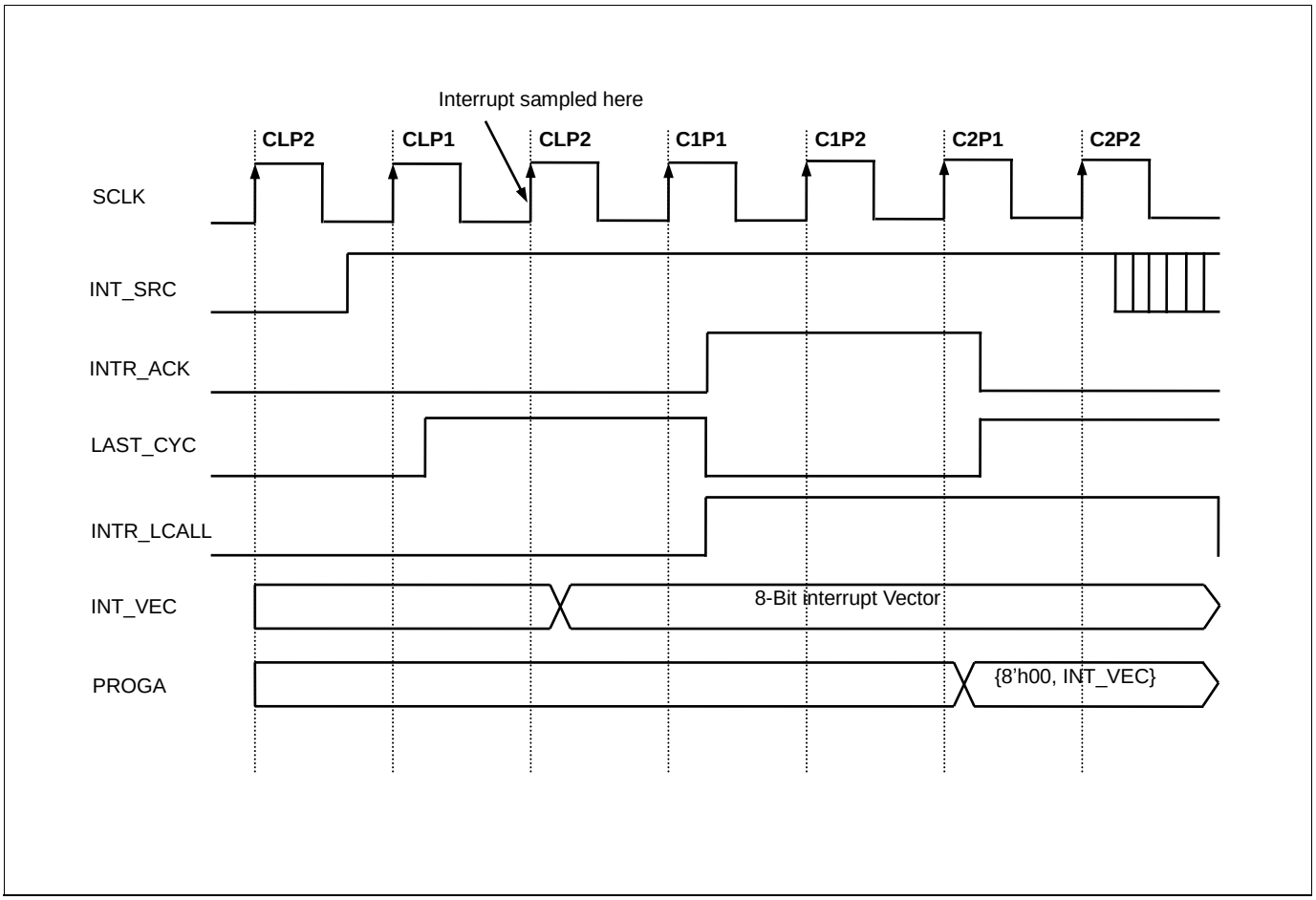


Figure 10.10 Timing Chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt sources are sampled at the last cycle of a command. If an interrupt source is detected the lower 8-bit of interrupt vector (INT_VEC) is decided. M8051W core makes interrupt acknowledge at the first cycle of a command, and executes long call to jump to interrupt service routine.

NOTE)

1. command cycle CLPx: L=Last cycle, 1=1st cycle or 1st phase, 2=2nd cycle or 2nd phase

10.12 Interrupt Register Overview

10.12.1 Interrupt Enable Register (IE, IE1, IE2, IE3)

Interrupt enable register consists of global interrupt control bit (EA) and peripheral interrupt control bits.Total 24 peripherals are able to control interrupt.

10.12.2 Interrupt Priority Register (IP, IP1)

The 24 interrupts are divided into 6 groups which haveeach 4 interrupt sources. A group can be assigned 4 levels interrupt priority using interrupt priority register. Level 3 is the highest priority, while level 0 is the lowest priority. After a reset IP and IP1 are cleared to ‘00H’. If interrupts have the same priority level, lower number interrupt is served first.

10.12.3 External Interrupt Flag Register (EIFLAG, KFLAG)

The external interrupt flag register (EIFLAG) and key interrupt flag register (KFLAG) are set to ‘1’ when the external interrupt generating condition is satisfied. The flag is cleared when the interrupt service routine is executed. Alternatively, the flag can be cleared by writing ‘0’ to it.

10.12.4 External Interrupt Edge Register (EIPOL, KPOL0, KPOL1)

The external interrupt polarityregister (EIPOL) and key interrupt polarity 0/1 register (KPOL0/KPOL1) determine the edge of interrupt (rising, falling and both edge).

10.12.5 Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIFLAG	A4H	R/W	00H	External Interrupt Flag Register
EIPOL	A5H	R/W	00H	External Interrupt Polarity Register
KFLAG	E8H	R/W	00H	Key Interrupt Flag Register
KPOL1	AFH	R/W	00H	Key Interrupt Polarity 1 Register
KPOL0	AEH	R/W	00H	Key Interrupt Polarity 0 Register

Table 10-3. Interrupt Register Map

10.12.6 Interrupt Register Description

The interrupt register is used for controlling interrupt functions. Also it has external interrupt control registers. The interrupt register consists of interrupt enable register (IE), interrupt enable register 1 (IE1), interrupt enable register 2 (IE2) and interrupt enable register 3 (IE3). For external interrupt, it consists of external interrupt flag register (EIFLAG), external interrupt polarity register (EIPOL), Keyinterrupt flag register (KFLAG), keyinterrupt polarity 0 register (KPOL0) andkey interrupt polarity 1 register (KPOL1).

10.12.7 Register Description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	–	INT5E	–	–	INT2E	INT1E	–
R/W	–	R/W	–	–	R/W	R/W	–

Initial value :00H

EA Enable or Disable All Interrupt bits
- 0 All Interrupt disable
- 1 All Interrupt enable

INT5E Enable or Disable Key Interrupt 0 ~ 7 (KEY0 ~ KEY7)
- 0 Disable
- 1 Enable

INT2E Enable or Disable External Interrupt 12 (EINT12)
- 0 Disable
- 1 Enable

INT1E Enable or Disable External Interrupt 10 (EINT10)
- 0 Disable
- 1 Enable

IE1 (Interrupt Enable Register 1): A9H

7	6	5	4	3	2	1	0
–	–	INT11E	INT10E	INT9E	–	–	–
–	–	R/W	R/W	R/W	–	–	–

Initial value: 00H

INT11E Enable or Disable SIO Interrupt
- 0 Disable
- 1 Enable

INT10E Enable or Disable UART Tx Interrupt
- 0 Disable
- 1 Enable

INT9E Enable or Disable UART Rx Interrupt
- 0 Disable
- 1 Enable

IE2 (Interrupt Enable Register 2) : AAH

7	6	5	4	3	2	1	0
–	–	–	INT16E	INT15E	INT14E	INT13E	–
–	–	–	R/W	R/W	R/W	R/W	–

Initial value :00H

INT16E Enable or Disable Timer 3 Interrupt
- 0 Disable
- 1 Enable

INT15E Enable or Disable Timer 2 Interrupt
- 0 Disable
- 1 Enable

INT14E Enable or Disable Timer 1 Interrupt
- 0 Disable
- 1 Enable

INT13E Enable or Disable Timer 0 Interrupt
- 0 Disable
- 1 Enable

IE3 (Interrupt Enable Register 3) : ABH

7	6	5	4	3	2	1	0
–	–	–	INT22E	INT21E	INT20E	–	–
–	–	–	R/W	R/W	R/W	–	–

Initial value :00H

INT22E Enable or Disable BIT Interrupt
- 0 Disable
- 1 Enable

INT21E Enable or Disable WDT Interrupt
- 0 Disable
- 1 Enable

INT20E Enable or Disable WT Interrupt
- 0 Disable
- 1 Enable

IP (Interrupt Priority Register) : B8H

7	6	5	4	3	2	1	0
–	–	IP5	IP4	IP3	IP2	IP1	IP0
–	–	RW	RW	RW	RW	RW	RW

Initial value :00H

IP1 (Interrupt Priority Register 1) : F8H

7	6	5	4	3	2	1	0
–	–	IP15	IP14	IP13	IP12	IP11	IP10
–	–	RW	RW	RW	RW	RW	RW

Initial value :00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG (External Interrupt Flag Register) : A4H

7	6	5	4	3	2	1	0
–	–	–	–	–	–	FLAG12	FLAG10
–	–	–	–	–	–	RW	RW

Initial value :00H

FLAG[1:0] When an external interrupt is occurred, the flag becomes ‘1’. The flag is cleared only by writing ‘0’ to the bit or automatically cleared by INT_ACK signal. Writing “1” has no effect.

0 External Interrupt not occurred

1 External Interrupt occurred

EIPOL (External Interrupt Polarity Register): A5H

7	6	5	4	3	2	1	0
–	–	–	–	POL12		POL10	
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

POL[3:0] External Interrupt (EINT10/EINT12) Polarity Selection

POLn[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 10, 12

KFLAG (Key Interrupt Flag Register) : E8H

7	6	5	4	3	2	1	0
KFLAG7	KFLAG6	KFLAG5	KFLAG4	KFLAG3	KFLAG2	KFLAG1	KFLAG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

KFLAG[7:0] When key interrupt is occurred, the flag becomes '1'. The flag is cleared only by writing '0' to the bit. So, the flag should be cleared by software. Writing "1" has no effect.

0 Key Interrupt 0~7 not occurred

1 Key Interrupt 0~7 occurred

KPOL1 (Key Interrupt Polarity 1 Register) : AFH

7	6	5	4	3	2	1	0
KPOL7		KPOL6		KPOL5		KPOL4	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

KPOL1[7:0] Key Interrupt (KEY4/KEY5/KEY6/KEY7) Polarity Selection

KPOLn[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 4, 5, 6, and 7

KPOL0 (Key Interrupt Polarity 0 Register) : AEH

7	6	5	4	3	2	1	0
KPOL3		KPOL2		KPOL1		KPOL0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

KPOL0[7:0] Key Interrupt (KEY0/KEY1/KEY2/KEY3) Polarity Selection

KPOLn[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 0, 1, 2, and 3

11 Peripheral Hardware

11.1 Clock Generator

11.1.1 Overview

As shown in Figure 11.1, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains main/sub-frequency clock oscillator.The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin.The default system clock is 1MHz INT-RC Oscillator and the default division rate is sixteen. In order to stabilize system internally, it is used1MHz INT-RC oscillator on POR.

- Calibrated Internal RC Oscillator (16MHz)
  - INT-RC OSC/1 (16MHz)
  - INT-RC OSC/2 (8MHz)
  - INT-RC OSC/4 (4MHz)
  - INT-RC OSC/8 (2MHz)
  - INT-RC OSC/16 (1MHz, Default system clock)
  - INT-RC OSC/32 (0.5MHz)
- Main Crystal Oscillator (0.4~12MHz)
- SubCrystal Oscillator (32.768kHz)
- Internal WDTRC Oscillator (5kHz)

11.1.2 Block Diagram

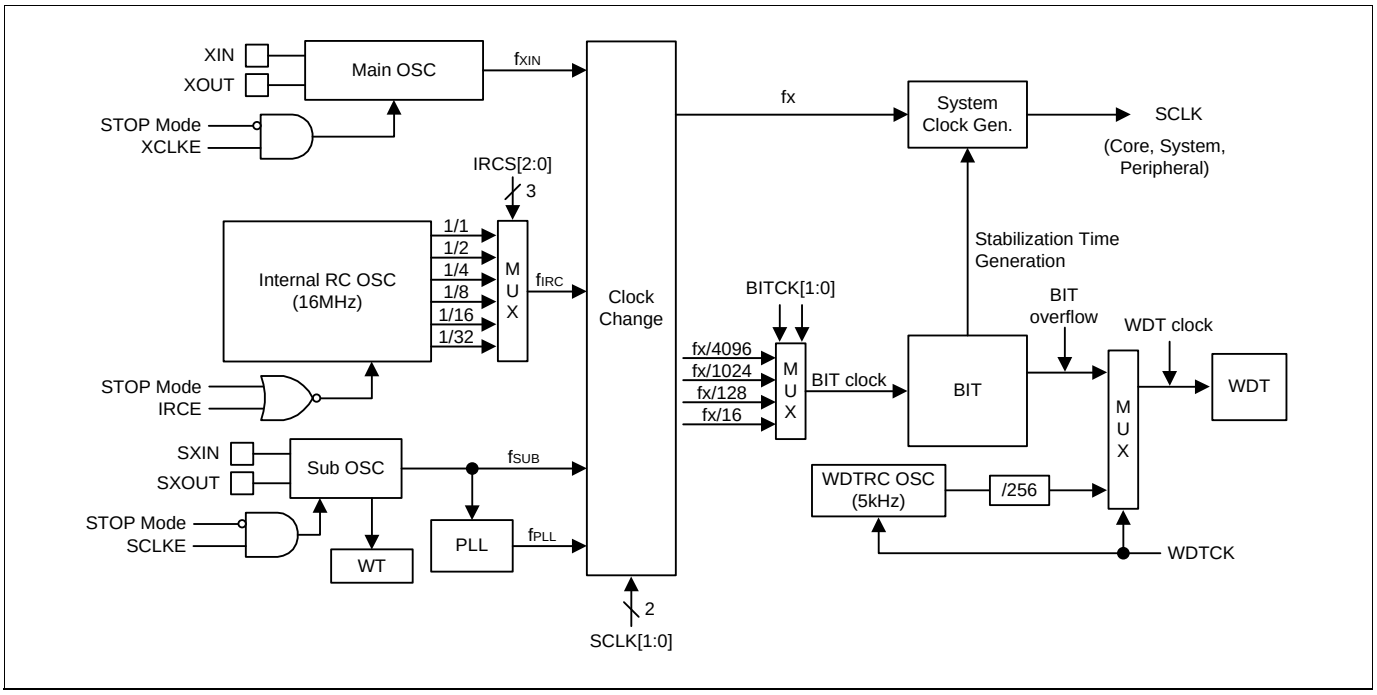


Figure 11.1 Clock Generator Block Diagram

11.1.3 PLL Circuit Diagram

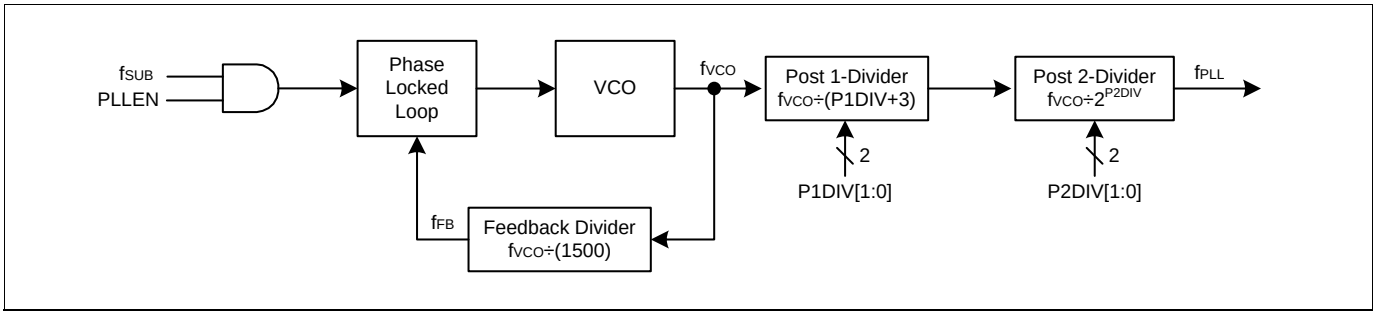


Figure 11.2 Clock Generator Block Diagram

11.1.4 Register Map

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register
OSCCR	D9H	R/W	08H	Oscillator Control Register
PLLCR	FFH	R/W	00H	Phase Locked-Loop Control Register

Table 11-1. Clock Generator Register Map

11.1.5 Clock Generator Register Description

The clock generatorregister uses clock control for system operation. The clock generation consists of system and clock control register (SCCR), oscillator control register (OSCCR) and phase locked-loop control register (PLLCR).

11.1.6 Register Description for Clock Generator

SCCR (System and Clock Control Register) : 8AH

7	6	5	4	3	2	1	0
–	–	–	–	–	–	SCLK1	SCLK0
–	–	–	–	–	–	R/W	R/W

Initial value :00H

SCLK [1:0] System Clock Selection Bit

SCLK1	SCLK0	Description
0	0	INT-RC OSC (f_{IRC}) for system clock
0	1	External Main OSC (f_{XIN}) for system clock
1	0	External Sub OSC (f_{SUB}) for system clock
1	1	Phase Locked-Loop (f_{PLL}) for system clock

OSCCR (Oscillator Control Register) : D9H

7	6	5	4	3	2	1	0
–	–	IRCS2	IRCS1	IRCS0	IRCE	XCLKE	SCLKE
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :08H

IRCS[2:0] Internal RC Oscillator Post-divider Selection

IRCS2	IRCS1	IRCS0	Description
0	0	0	f_{IRC}/32 (0.5MHz)
0	0	1	f_{IRC}/16 (1MHz)
0	1	0	f_{IRC}/8 (2MHz)
0	1	1	f_{IRC}/4 (4MHz)
1	0	0	f_{IRC}/2 (8MHz)
1	0	1	f_{IRC}/1 (16MHz)
Other values			Not used

IRCE Control the Operation of the Internal RC Oscillator

0 Enable operation of INT-RC OSC

1 Disable operation of INT-RC OSC

XCLKE Control the Operation of the External Main Oscillator

0 Disable operation of X-TAL

1 Enable operation of X-TAL

SCLKE Control the Operation of the External Sub Oscillator

0 Disable operation of SX-TAL

1 Enable operation of SX-TAL

PLLCR (Phase Locked Loop Control Register) : FFH

7	6	5	4	3	2	1	0
–	–	PLLSTA	P1DIV1	P1DIV0	P2DIV1	P2DIV0	PLLEN
–	–	R	R/W	R/W	R/W	R/W	R/W

Initial value :00H

PLLSTA PLL Locked/Unlocked Status Bit

0 PLL currently in unlocked state

1 PLL currently in locked state

P1DIV[1:0] PLL Post 1-Divider Selection Bits(49.152MHz)

P1DIV1	P1DIV0	Description
0	0	$f_{VCO}/3$ = 16.384MHz
0	1	$f_{VCO}/4$ = 12.888MHz
1	0	$f_{VCO}/5$ = 9.8304MHz
1	1	$f_{VCO}/6$ = 8.192MHz

P2DIV[1:0] PLL Post 2-Divider Data Bits

P2DIV1	P2DIV0	Description
0	0	$f_{PLL} = f_{VCO}/1$
0	1	$f_{PLL} = f_{VCO}/2$
1	0	$f_{PLL} = f_{VCO}/4$
1	1	$f_{PLL} = f_{VCO}/8$

PLLEN PLL Enable/Disable Control Bit

0 PLL Disable

1 PLL Enable

11.2 Basic Interval Timer

11.2.1 Overview

The MC96F6508A has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 11.3. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

The MC96F6508A has these basic interval timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As timer function, timer interrupt occurrence

11.2.2 Block Diagram

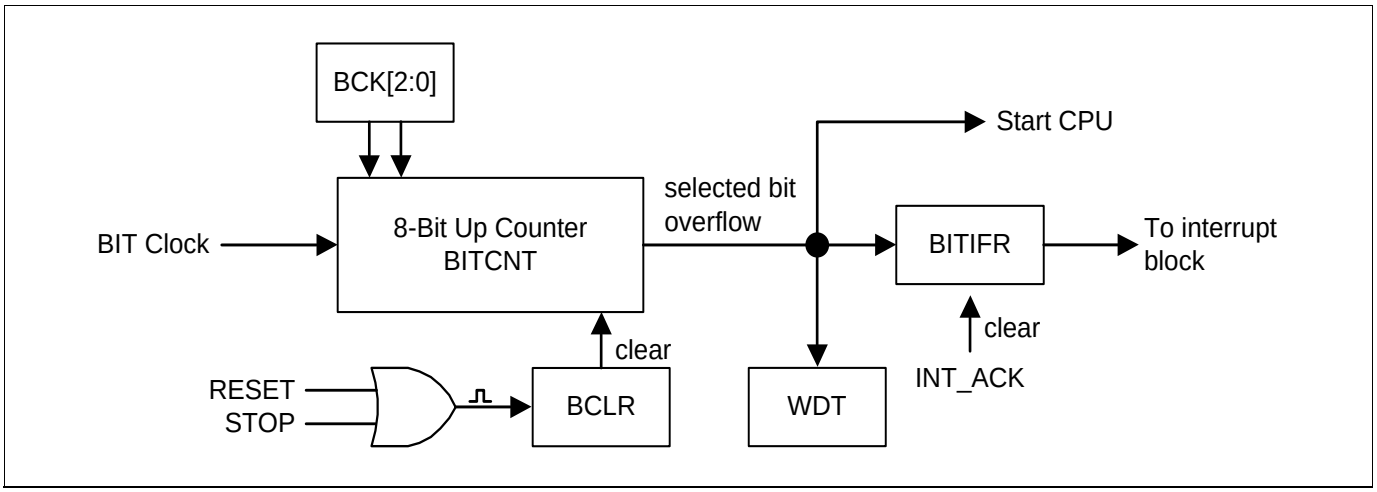


Figure 11.3 Basic Interval Timer Block Diagram

11.2.3 Register Map

Name	Address	Dir	Default	Description
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register
BITCR	8BH	R/W	01H	Basic Interval Timer Control Register

Table 11-2. Basic Interval Timer Register Map

11.2.4 Basic Interval Timer Register Description

The basicinterval timer register consists of basic interval timer counter register (BITCNT) and basic interval timer control register (BITCR). If BCLR bit is set to '1', BITCNT becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared to '0' automatically.

11.2.5 Register Description for Basic Interval Timer

BITCNT (Basic Interval Timer Counter Register) : 8CH

7	6	5	4	3	2	1	0
BITCNT7	BITCNT6	BITCNT5	BITCNT4	BITCNT3	BITCNT2	BITCNT1	BITCNT0
R	R	R	R	R	R	R	R

Initial value :00H

BITCNT[7:0] BIT Counter

BITCR (Basic Interval Timer Control Register) : 8BH

7	6	5	4	3	2	1	0
BITIFR	BITCK1	BITCK0	–	BCLR	BCK2	BCK1	BCK0
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Initial value :01H

BITIFR When BIT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 BIT interrupt no generation

1 BIT interrupt generation

BITCK[1:0] Select BIT clock source

BITCK1	BITCK0	Description
0	0	fx/4096
0	1	fx/1024
1	0	fx/128
1	1	fx/16

BCLR If this bit is written to ‘1’, BIT Counter is cleared to ‘0’

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	Description
0	0	0	Bit 0 overflow (BIT Clock * 2)
0	0	1	Bit 1 overflow (BIT Clock * 4) (default)
0	1	0	Bit 2 overflow (BIT Clock * 8)
0	1	1	Bit 3 overflow (BIT Clock * 16)
1	0	0	Bit 4 overflow (BIT Clock * 32)
1	0	1	Bit 5 overflow (BIT Clock * 64)
1	1	0	Bit 6 overflow (BIT Clock * 128)
1	1	1	Bit 7 overflow (BIT Clock * 256)

11.3 Watch Dog Timer

11.3.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPUreset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8bits of WDTCNT, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow.The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

11.3.2 WDT Interrupt Timing Waveform

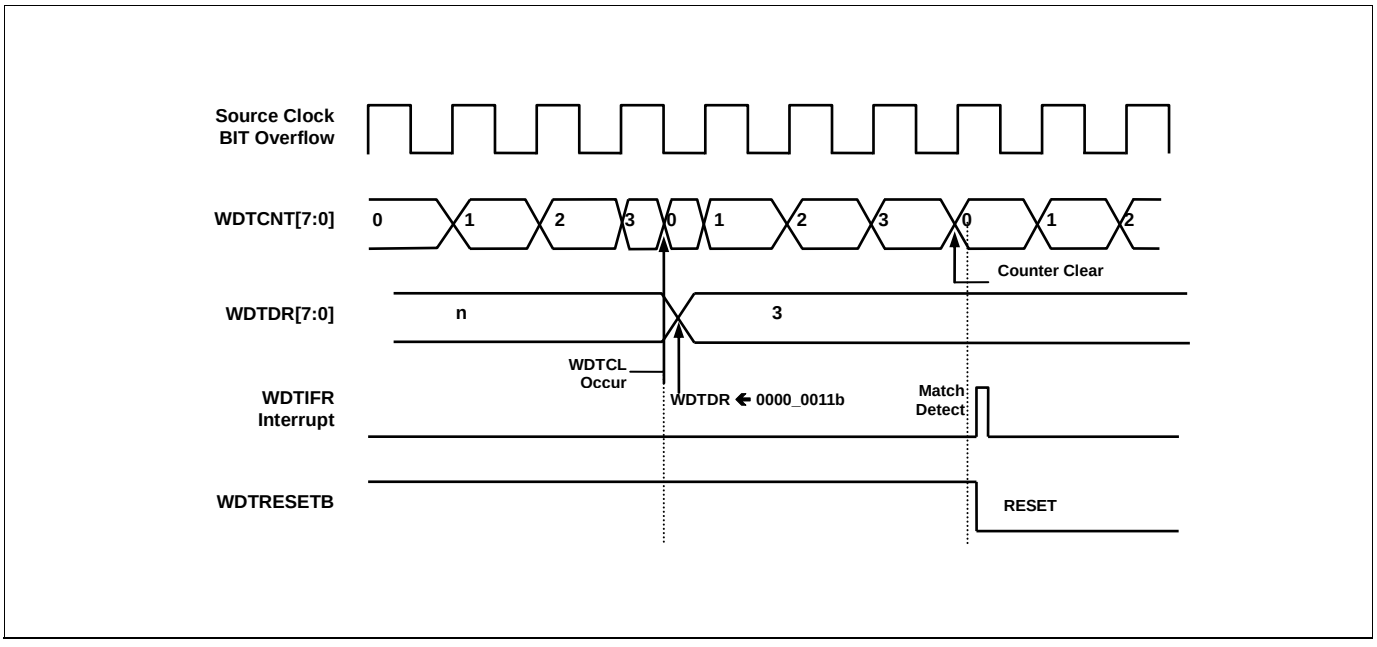


Figure 11.4 Watch Dog Timer Interrupt Timing Waveform

11.3.3 Block Diagram

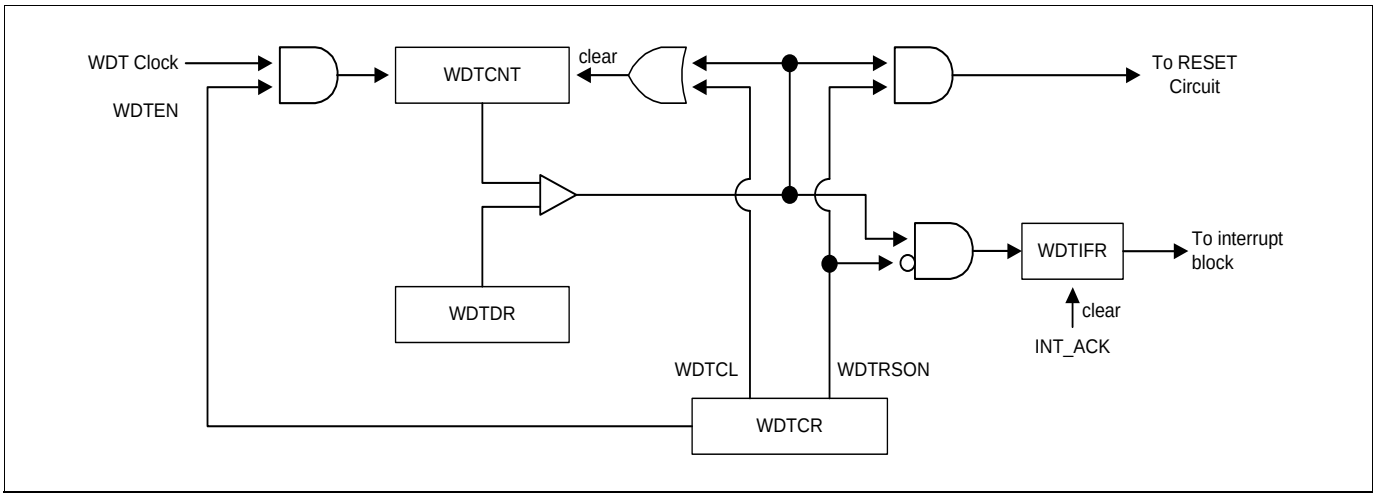


Figure 11.5 Watch Dog Timer Block Diagram

11.3.4 Register Map

Name	Address	Dir	Default	Description
WDTCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTDR	8EH	W	FFH	Watch Dog Timer Data Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

Table 11-3. Watch Dog Timer Register Map

11.3.5 Watch Dog Timer Register Description

The watch dog timer register consists of watch dog timer counter register (WDTCNT), watch dog timer dataregister (WDTDR) and watch dog timer controlregister (WDTCR).

11.3.6 Register Description for Watch Dog Timer

WDTCNT (Watch Dog Timer Counter Register: Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value :00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register: Write Case) : 8EH

7	6	5	4	3	2	1	0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value :FFH

WDTDR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTDR Value+1)
NOTE)

1. Do not write “0” in the WDTDR register.

WDTCR (Watch Dog Timer Control Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	–	–	–	WDTCK	WDTIFR
R/W	R/W	R/W	–	–	–	R/W	R/W

Initial value :00H

WDTEN Control WDT Operation
0 Disable
1 Enable

WDTRSON Control WDT RESET Operation
0 Free Running 8-bit timer
1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WDTCK Control WDT Clock Selection Bit
0 BIT overflow for WDT clock (WDTRC disable)
1 WDTRC for WDT clock (WDTRC enable)

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.
0 WDT Interrupt no generation
1 WDT Interrupt generation

11.4 Watch Timer

11.4.1 Overview

The watch timer has the function for RTC (Real Time Clock) operation.It is generally used for RTC design.The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit, and watch timer control register. To operate the watch timer, determine the input clock source, output interval, and set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock is able to be so alive that WT can continue the operation. The watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to raise resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

The watch timer supplies the clock frequency for the LCD driver (f_{LCD}). Therefore, if the watch timer is disabled, the LCD driver controller does not operate.

11.4.2 Block Diagram

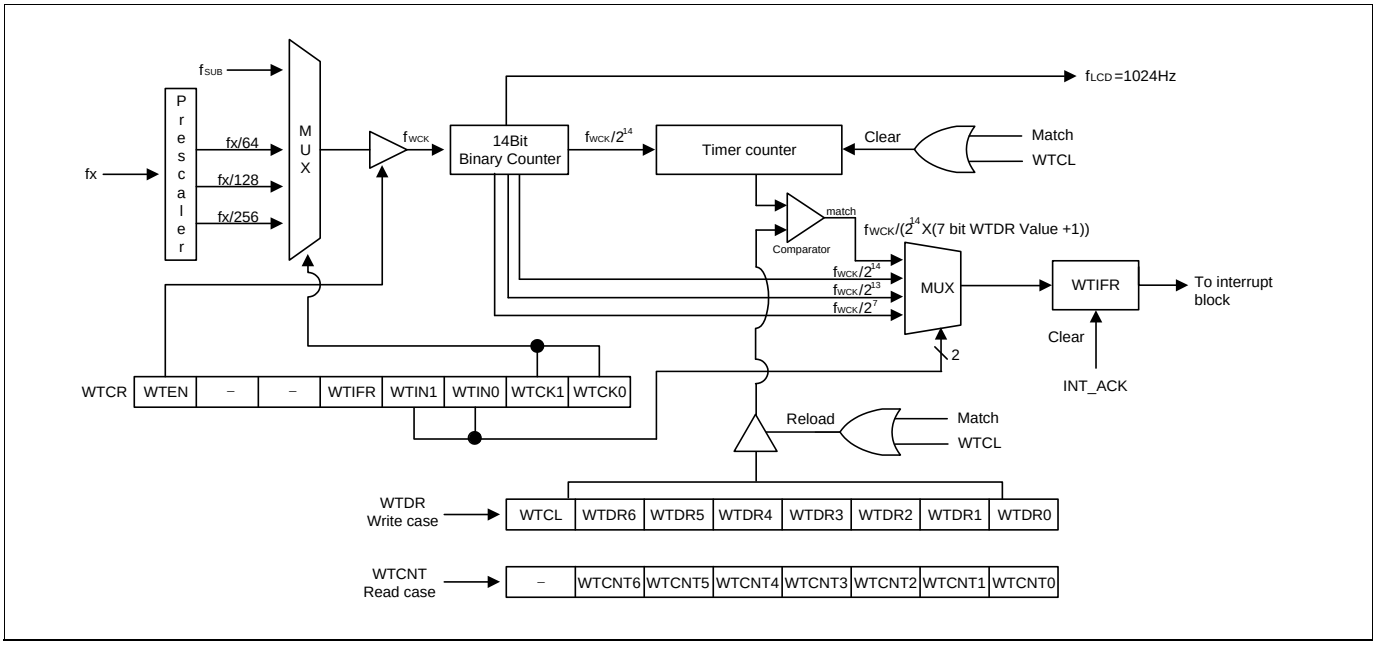


Figure 11.6 Watch Timer Block Diagram

11.4.3 Register Map

Name	Address	Dir	Default	Description
WTCNT	9FH	R	00H	Watch Timer Counter Register
WTDR	9FH	W	7FH	Watch Timer Data Register
WTCR	9EH	R/W	00H	Watch Timer Control Register

Table 11-4. Watch Timer Register Map

11.4.4 Watch Timer Register Description

The watch timer register consists of watch timer counter register (WTCNT), watch timer data register (WTDR), and watch timer controlregister (WTCR). AsWTCR is 6-bit writable/readable register, WTCR can control the clock source (WTCK[1:0]), interrupt interval (WTIN[1:0]), and function enable/disable (WTEN). Also there is WT interrupt flag bit (WTIFR).

11.4.5 Register Description for Watch Timer

WTCNT (Watch Timer Counter Register: Read Case) : 9FH

7	6	5	4	3	2	1	0
–	WTCNT6	WTCNT5	WTCNT4	WTCNT3	WTCNT2	WTCNT1	WTCNT0
–	R	R	R	R	R	R	R

Initial value :00H

WTCNT[6:0] WT Counter

WTDR (Watch Timer Data Register: Write Case) : 9FH

7	6	5	4	3	2	1	0
WTCL	WTDR6	WTDR5	WTDR4	WTDR3	WTDR2	WTDR1	WTDR0
R/W	W	W	W	W	W	W	W

Initial value :7FH

WTCL Clear WT Counter

0 Free Run

1 Clear WT Counter (auto clear after 1 Cycle)

WTDR[6:0] Set WT Period

WT Interrupt Interval=fwck/(2^14 x(7bit WTDR Value+1))

NOTE)

1. Do not write “0” in the WTDR register.

WTCR (Watch Timer Control Register) : 9EH

7	6	5	4	3	2	1	0
WTEN	–	–	WTIFR	WTIN1	WTIN0	WTCK1	WTCK0
R/W	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

WTEN Control Watch Timer

0 Disable

1 Enable

WTIFR When WT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal. Writing "1" has no effect.

0 WT Interrupt no generation

1 WT Interrupt generation

WTIN[1:0] Determine Interrupt Interval

WTIN1	WTIN0	Description
0	0	f_{WCK}/2^7
0	1	f_{WCK}/2^13
1	0	f_{WCK}/2^14
1	1	f_{WCK}/(2^14 x (7bit WTDR Value+1))

WTCK[1:0] Determine Source Clock

WTCK1	WTCK0	Description
0	0	f_{SUB}
0	1	f_X/256
1	0	f_X/128
1	1	f_X/64

NOTE)

1. f_X– System clock frequency (Where fx= 4.19MHz)
2. f_{SUB}– Sub clock oscillator frequency (32.768kHz)
3. f_{WCK}– Selected Watch timer clock
4. f_{LCD} – LCD frequency (Where f_X= 4.19MHz, WTCK[1:0]='10'; f_{LCD}= 1024Hz)

11.5 Timer 0, 1

11.5.1 Overview

Timer 0 and timer 1 can be used either two 8-bit timer counter or one 16-bit timer counter with combine them. Each 8-bit timer counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register, capture data register, carrier mode control register and timer interrupt flag register. (T0CNT, T0DR, T0CDR, T0CR, T1CNT, T1DRH, T1DRL, T1CDR, T1CR, CARCR, TIFR).

It has five operating modes:

- 8-bit timercounter mode
- 8-bit capture mode
- 16-bit timercounter mode
- 16-bit capture mode
- Carrier mode

The timercounter 0 and 1 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T0CK[2:0], T1CK[2:0]).

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048, EC0
- TIMER1 clock source: f_X/1, 2, 4, 8, 64, 256, 512, 1024

In the capture mode, by EINT10, the data is captured into input capture data register (T0CDR, T1CDR).
In 8-bit timercounter 0/1 mode, whenever counter value is equal to T0DR/T1DRH, T0O/REM port toggles. Also In 16-bit timercounter 0 mode, Timer 0 outputs the comparison result between counter and data register through T0O port.
In the carrier mode, Timer 1 can be used to generate the carrier frequency or a remote controller signal. Timer 1 can output the comparison result between T1CNT & T1DRH/L and carrier frequency through REM port.T1CNT value is cleared by hardware.

16BIT0	T0MS	T1MS	T0CK[2:0]	T1CK[2:0]	Timer 0	Timer 1
0	0	0	XXX	XXX	8 Bit TimerCounter Mode	8 Bit TimerCounter Mode
0	1	0	XXX	XXX	8 Bit Capture Mode	8 Bit TimerCounter Mode
0	0	1	XXX	XXX	8 Bit TimerCounter Mode	Carrier Mode
0	1	1	XXX	XXX	8 Bit Capture Mode	Carrier Mode
1	0	0	XXX	XXX	16 Bit TimerCounter Mode	
1	1	0	XXX	XXX	16 Bit Capture Mode	

Table 11-5. Timer 0/1Operating Modes

11.5.2 8-Bit Timer/Counter Mode

The 8-bit timer counter mode is selected by control register as shown in Figure 11.7.

The two 8-bit timers have each counter and data register. The counter register is increased by internal clock or external clock(EC0) input.Timer 0 can use the input clock with one of 2, 4, 8, 32, 128, 512, and 2048prescaler division rates (T0CK[2:0]). Timer 1 can use the input clock with one of 1, 2, 4, 8, 64, 256, 512, and 1024 prescaler division rates (T1CK[2:0]). When the value of T0CNT, T1CNT and T0DR, T1DRH are respectively identical in Timer 0, 1, the interrupt of Timer 0, 1 occurs.

The external clock (EC0) counts up the timer at the rising edge. If the EC0 is selected as a clock source by T0CK[2:0], EC0 port should be set to the input port by P54IO bit

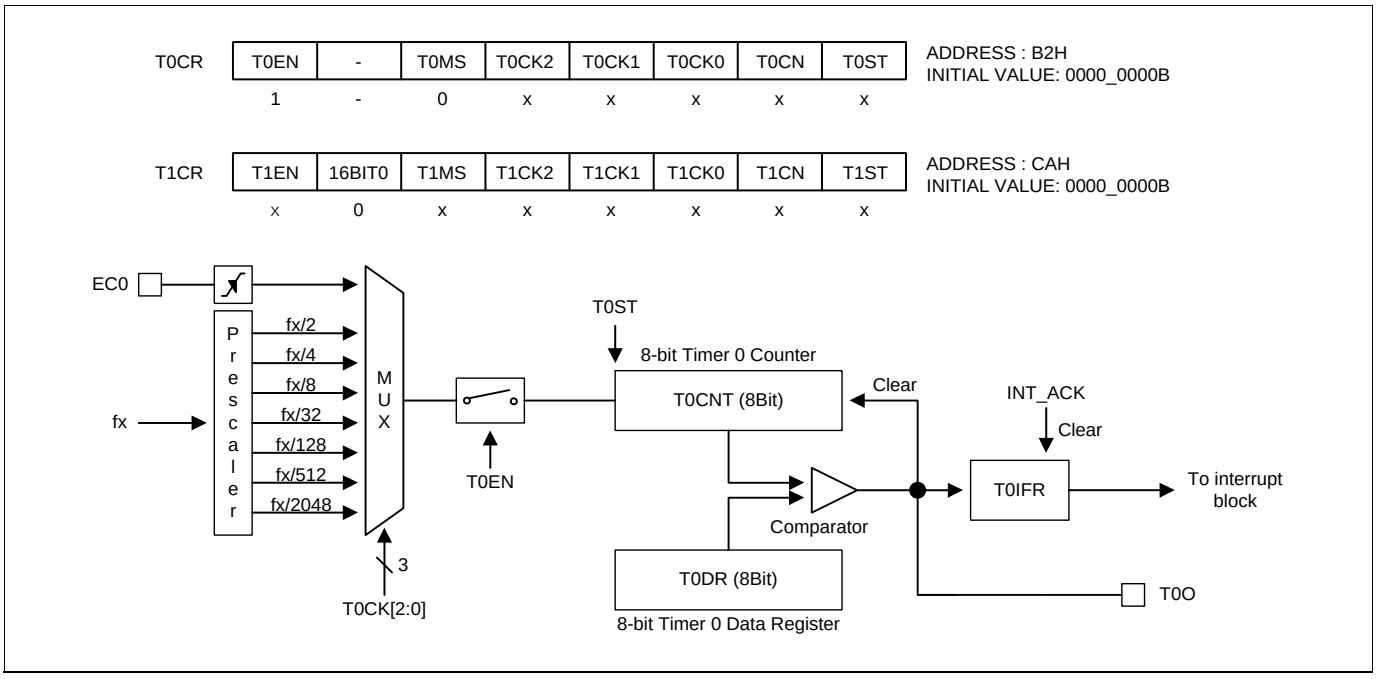


Figure 11.7 8-Bit Timer/Counter Mode for Timer 0

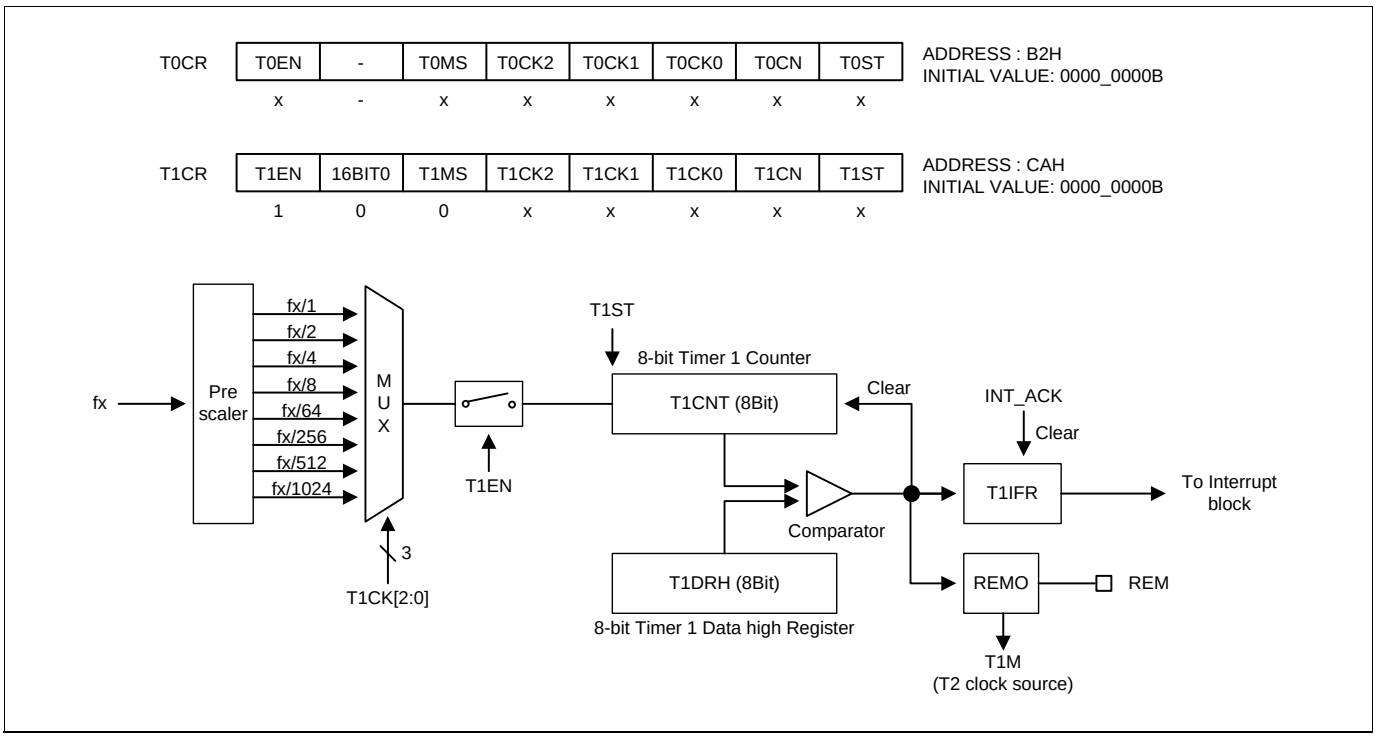


Figure 11.8 8-Bit Timer Counter Mode for Timer1

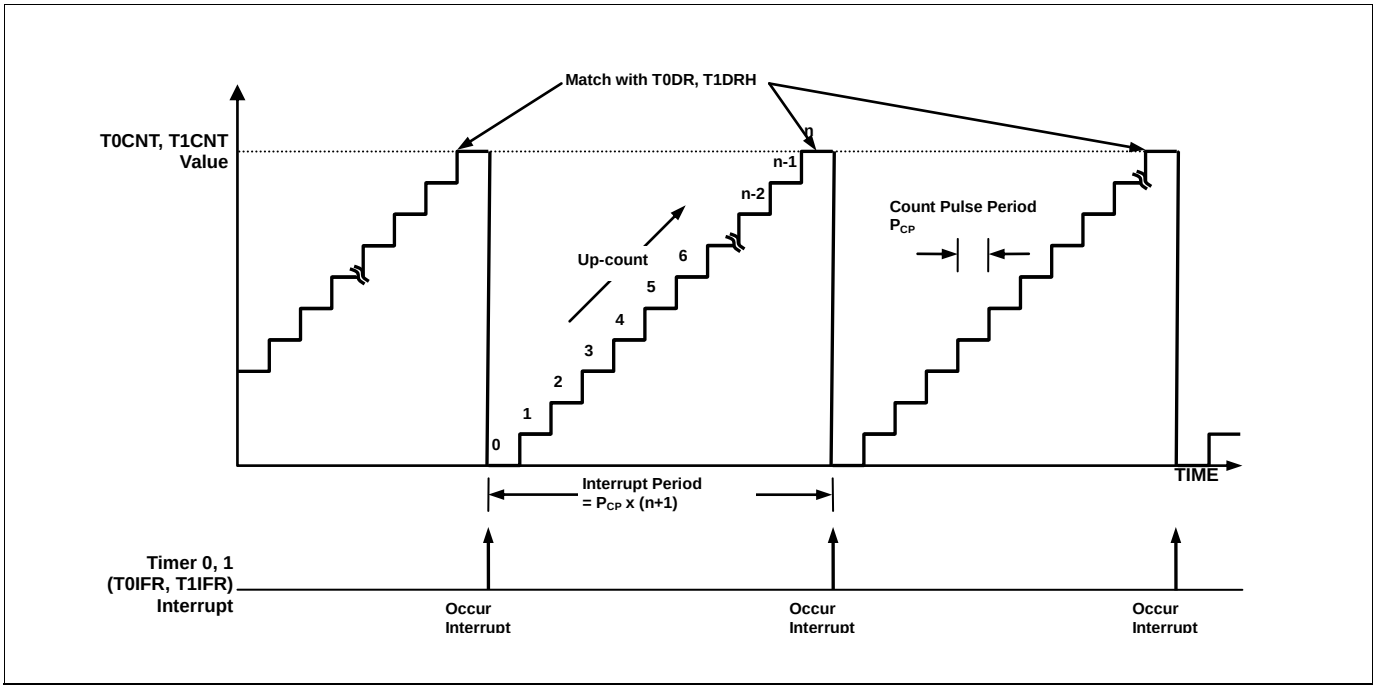


Figure 11.9 8-Bit Timer Counter 0, 1 Example

11.5.3 16-Bit Timer Counter 0 Mode

The 16-bit timercounter mode is selected by control register as shown in Figure 11.10.

The timer register is being run with all 16bits. A 16-bit timercounter register T0CNT, T1CNT are incrementd 0000H to FFFFH until it matches T0DR, T1DRH and then resets to 0000H. The match output generates the Timer 0 interrupt (No Timer 1 interrupt). The clock source is selected from T0CK[2:0] and 16BIT0 bit must be set to '1'. Timer 0 is LSB 8-bit, the timer 1 is MSB 8-bit.

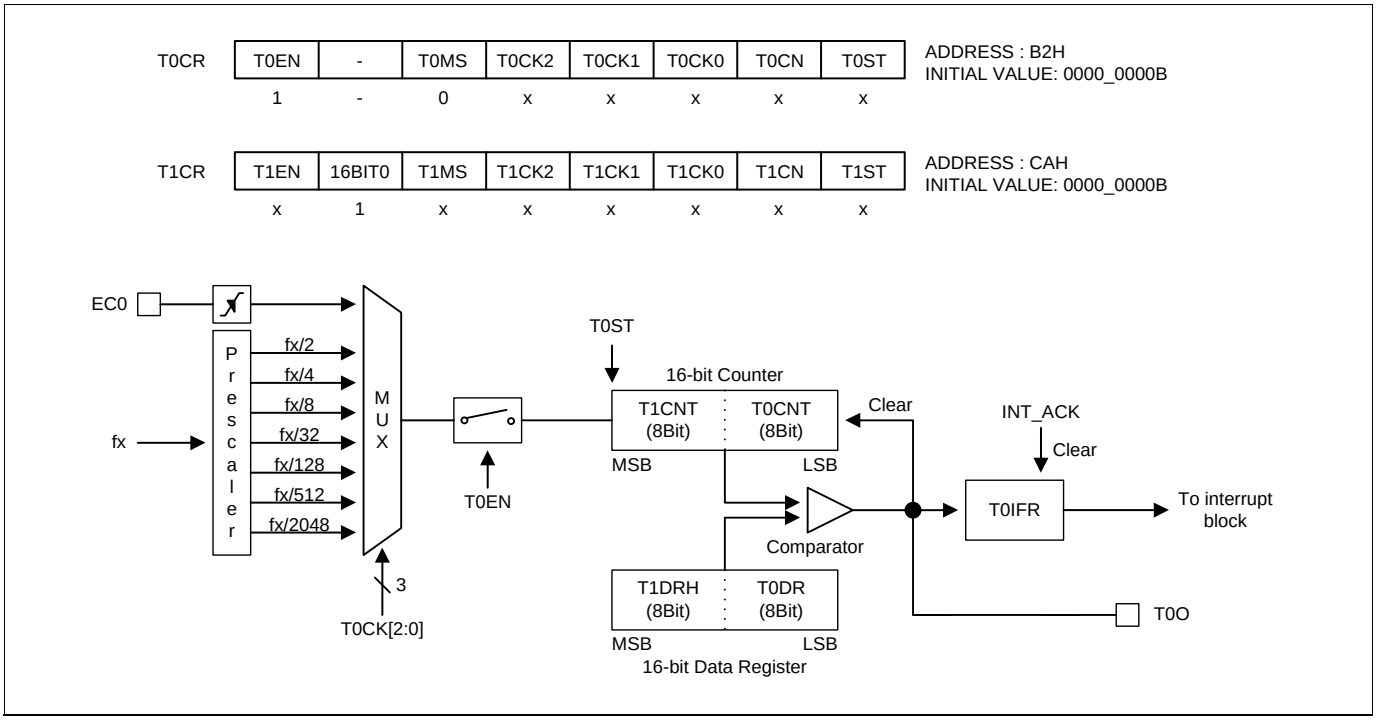


Figure 11.10 16-Bit Timer Counter Mode for Timer 0

11.5.4 8-Bit Timer 0 Capture Mode

The 8-bit Capture mode is selected by control register as shown in Figure 11.11.

The timer 0 capture mode is set by T0MS as '1'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer counter mode and the interrupt occurs when T0CNT is equal to T0DR. T0CNT value is automatically cleared by hardware and it can be also cleared by software (T0ST).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0CDR. In the timer 0 capture mode, timer 0 output (T0O) waveform is not available.

According to the EIPOL register setting, the external interrupt EINT10 function is chose. Of course, the EINT10 pin must be set to an input port.

T0CDR and T0DRare in the same address. In the capture mode, reading operation reads T0CDR, not T0DR and writing operation will update T0DR.

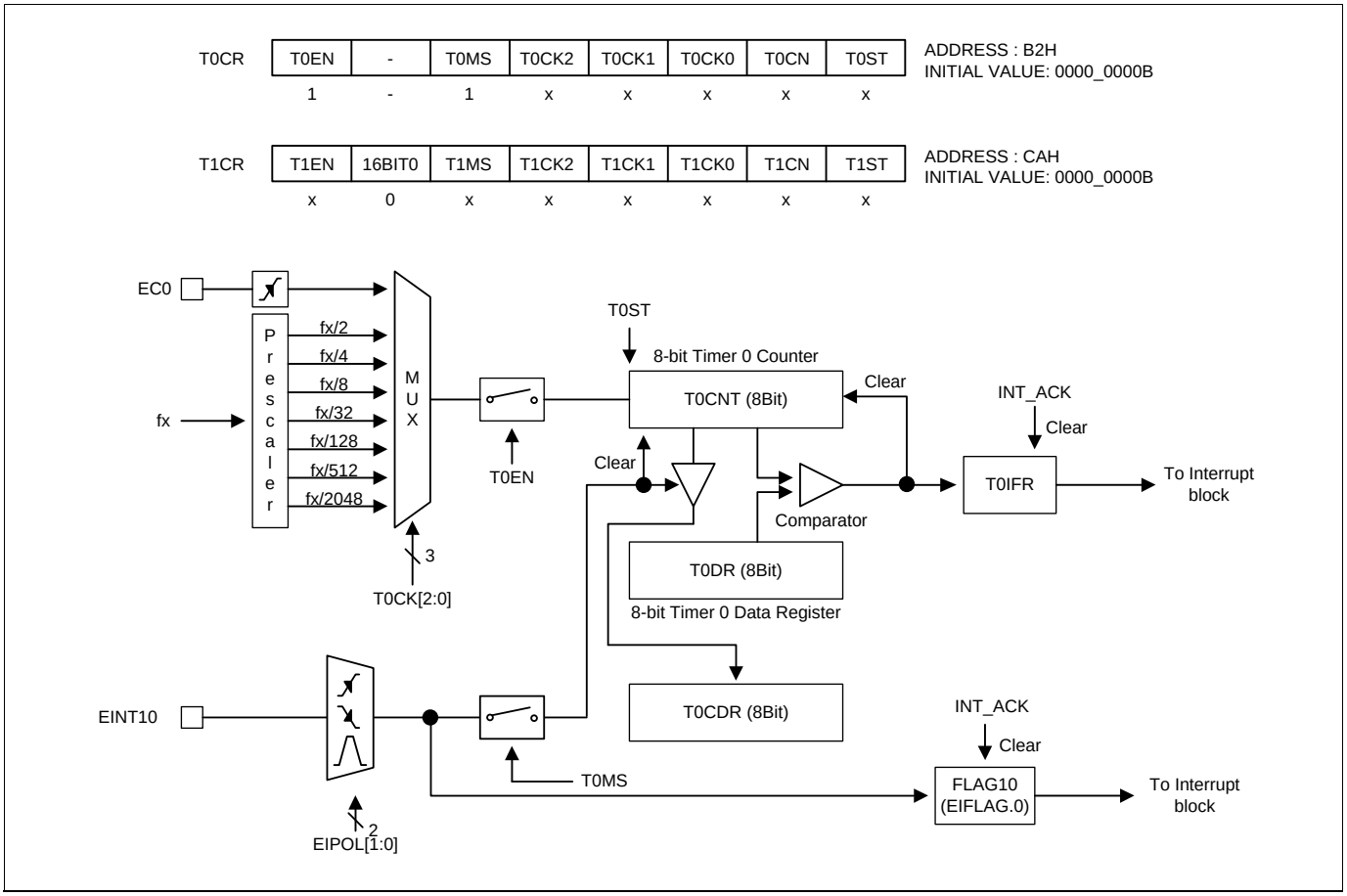


Figure 11.11 8-Bit Capture Mode for Timer 0

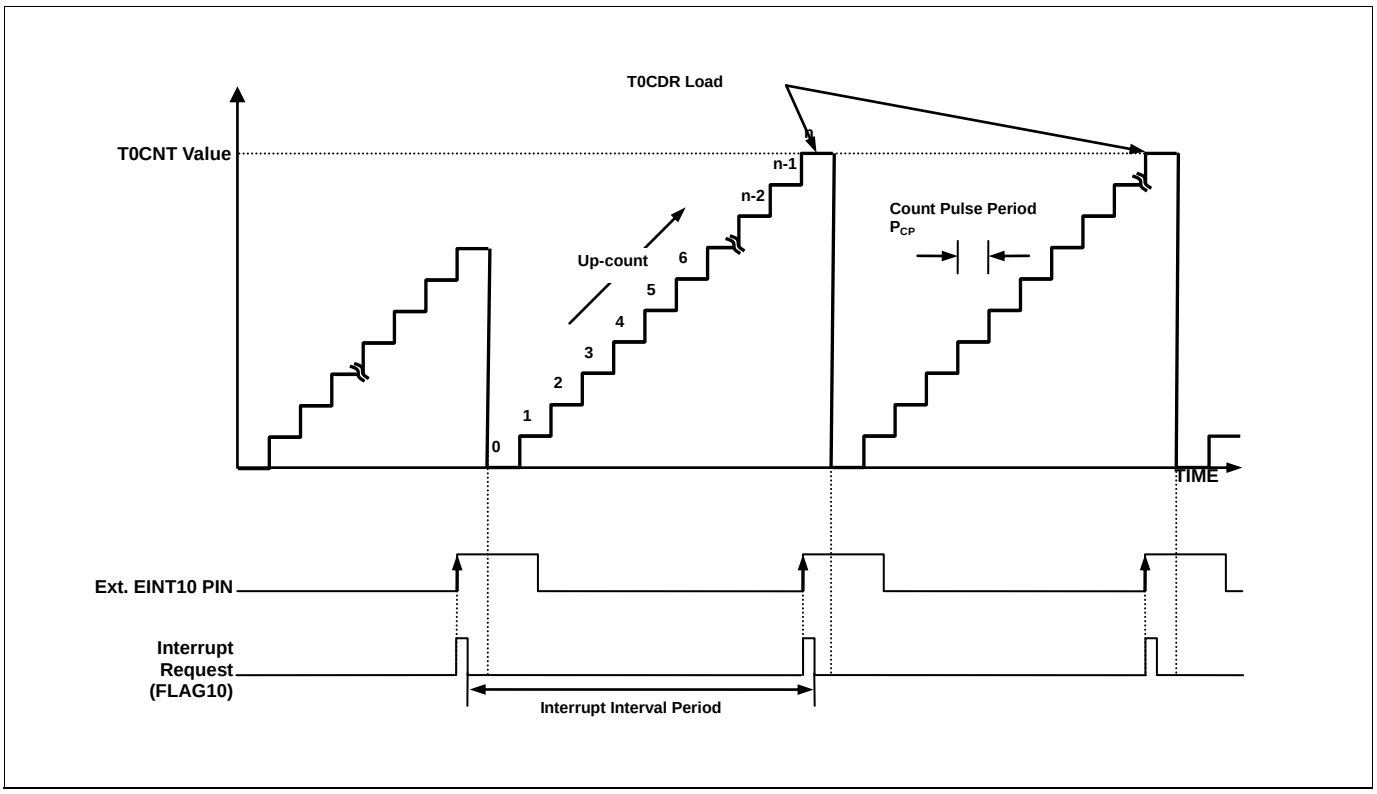


Figure 11.12 Input Capture Mode Operation for Timer 0

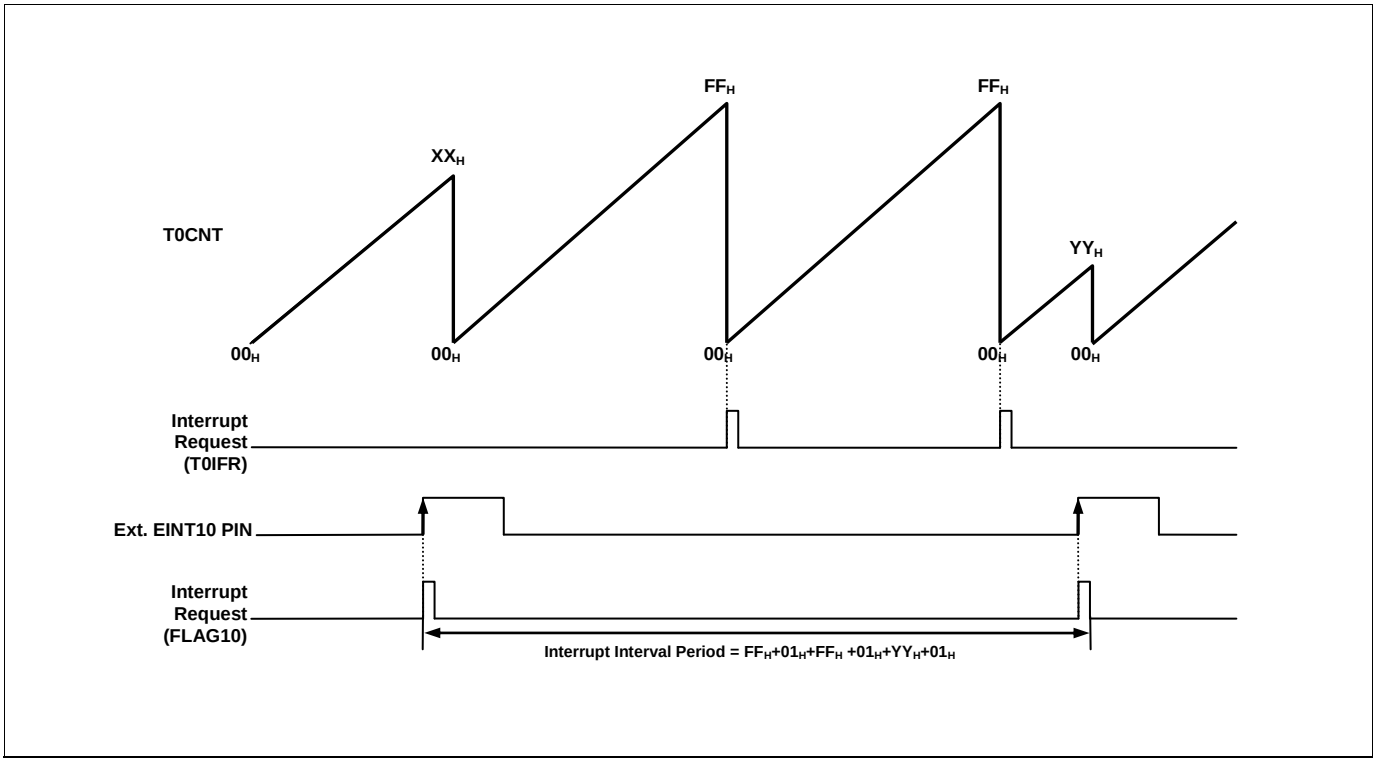


Figure 11.13 Express Timer Overflow in Capture Mode

11.5.5 16-Bit Timer 0 Capture Mode

The 16-bit capture mode is selected by control register as shown in Figure 11.14.

The 16-bit captue mode is the same oeration as 8-bit capture mode, except that the timer register uses 16 bits.The clock source is selected from T0CK[2:0] and 16BIT0 bit must be set to '1'.

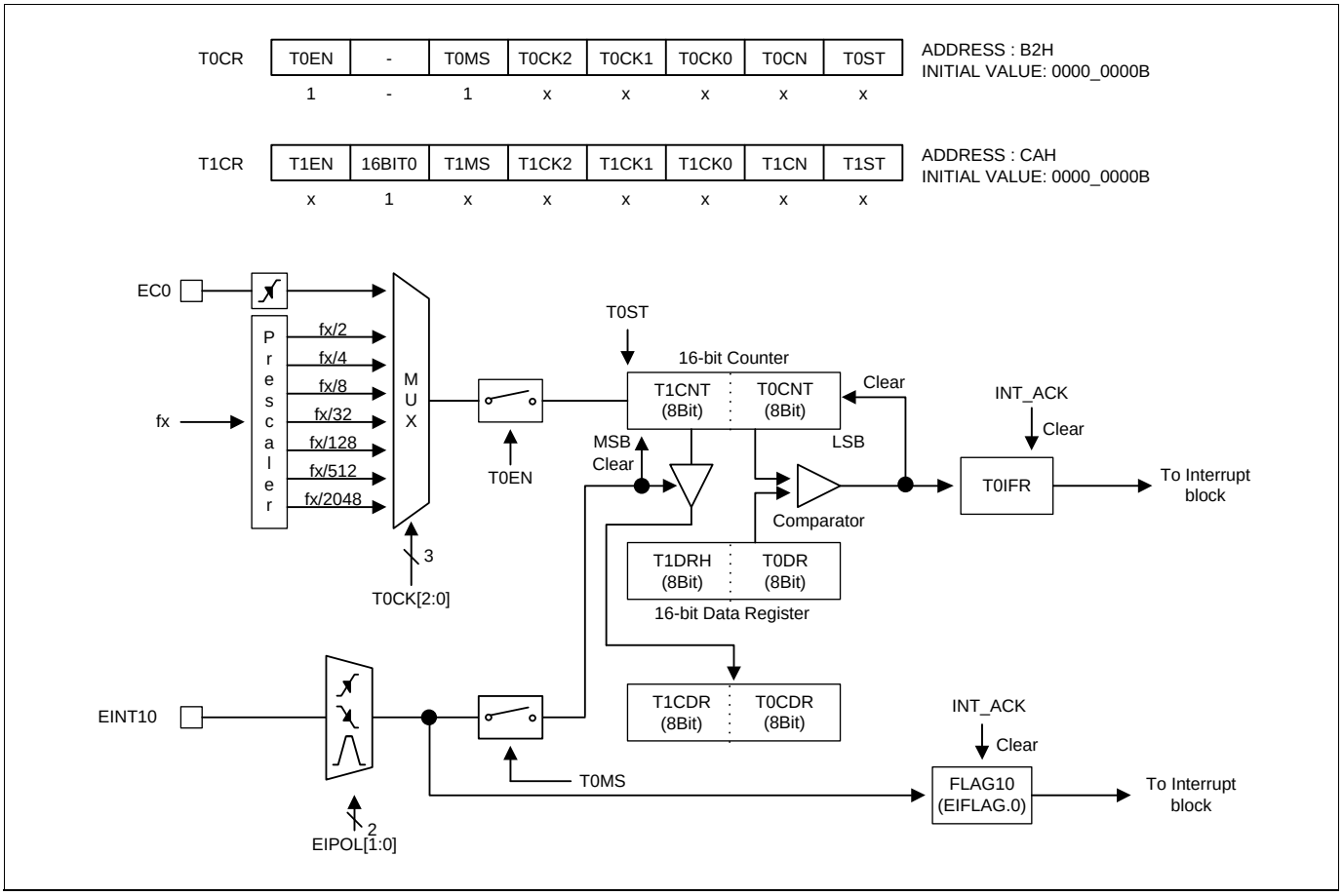


Figure 11.14 16-Bit Capture Mode for Timer 0

11.5.6 8-Bit Timer 1 Carrier Frequency Mode

The carrier frequency and the pulse of data are calculated by the formula in the following sheet. The Figure 11.15 shows the block diagram of Timer 1 for carrier frequency mode.

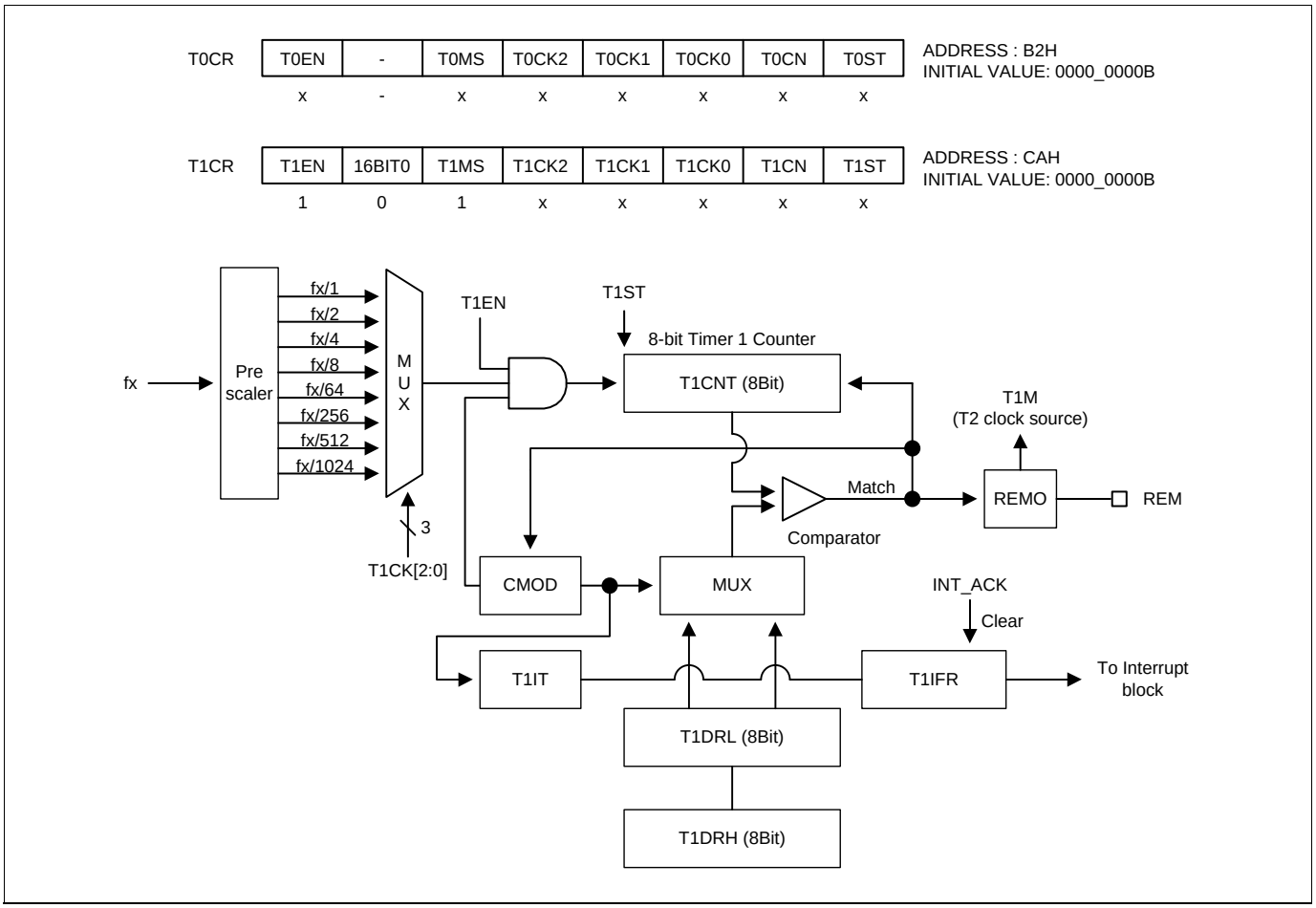
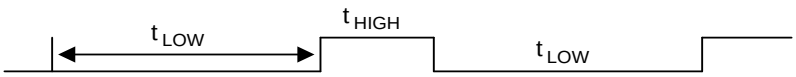


Figure 11.15 Carrier Mode for Timer 1

NOTE)

1. When one of T1DRH and T1DRL values is “00H”, the carrier frequency generator (REM) output always becomes a “High” or “Low”. At that time, Timer 1 Interrupt Flag Bit (T1IFR) is not set.

11.5.7 Carrier Output Pulse Width Calculations



To generate the above repeated waveform consisted of low period time (t_{LOW}), and high period time (t_{HIGH}).

When REMO = 0,

t_{LOW} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH< 100H, where f_{T1} = The selected clock.

When REMO = 1,

t_{LOW} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH< 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

To make t_{LOW}= 24 us and t_{HIGH} = 15 us. f_X = 4 MHz, f_{T1} = 4 MHz/4 = 1 MHz

When REMO = 0,

t_{LOW} = 24 us = (T1DRL + 1) /f_{T1} = (T1DRL + 1) x 1us, T1DRL = 22.

t_{HIGH} = 15 us = (T1DRH + 1) /f_{T1} = (T1DRH + 1) x 1us, T1DRH = 13.

When REMO = 1,

t_{LOW} = 24 us = (T1DRH + 1) / f_{T1} = (T1DRH + 1) x 1us, T1DRH = 22.

t_{HIGH} = 15 us = (T1DRL + 1) / f_{T1} = (T1DRL + 1) x 1us, T1DRL = 13.

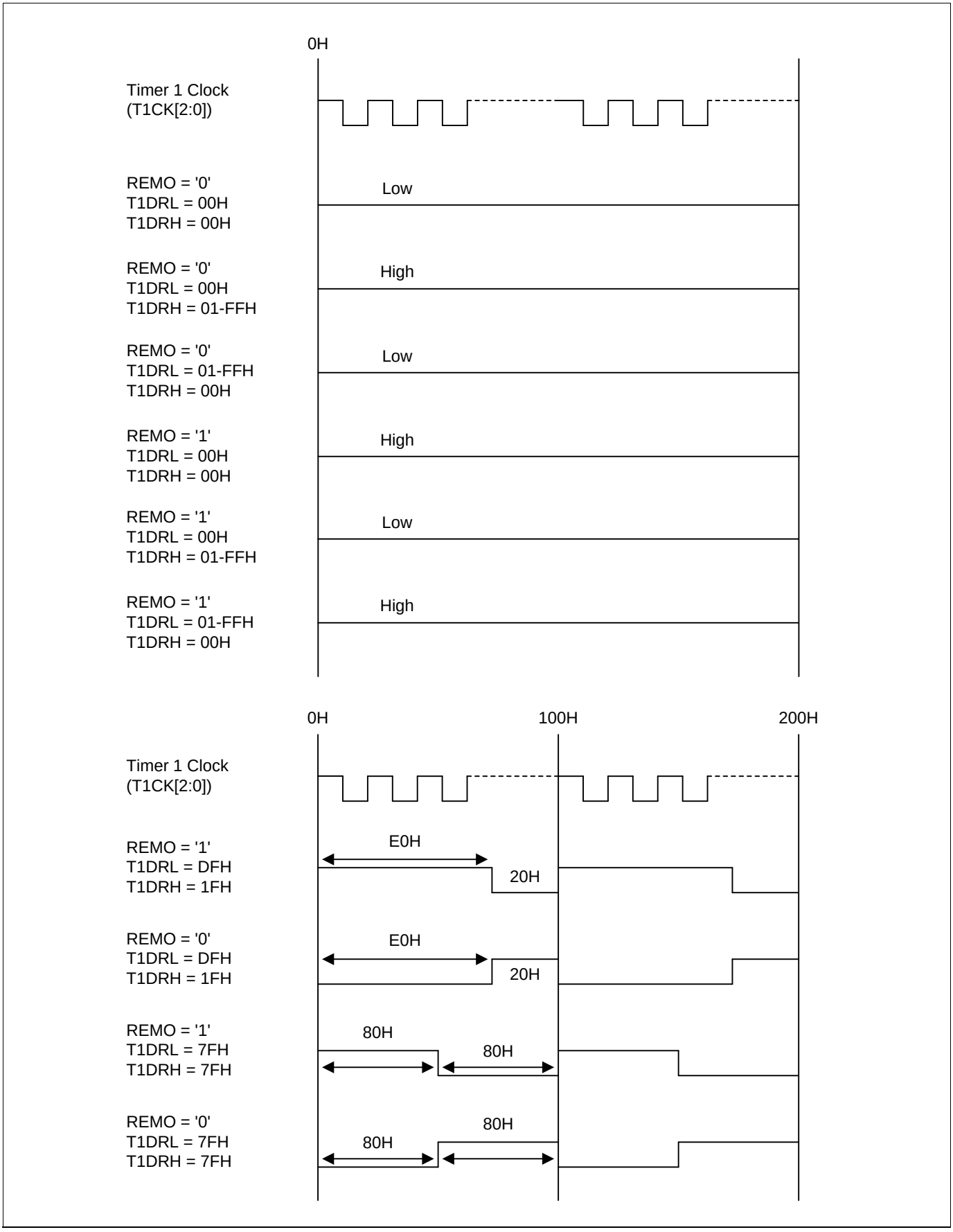


Figure 11.16 Carrier Output Waveforms in Repeat Mode for Timer 1

11.5.8 Block Diagram

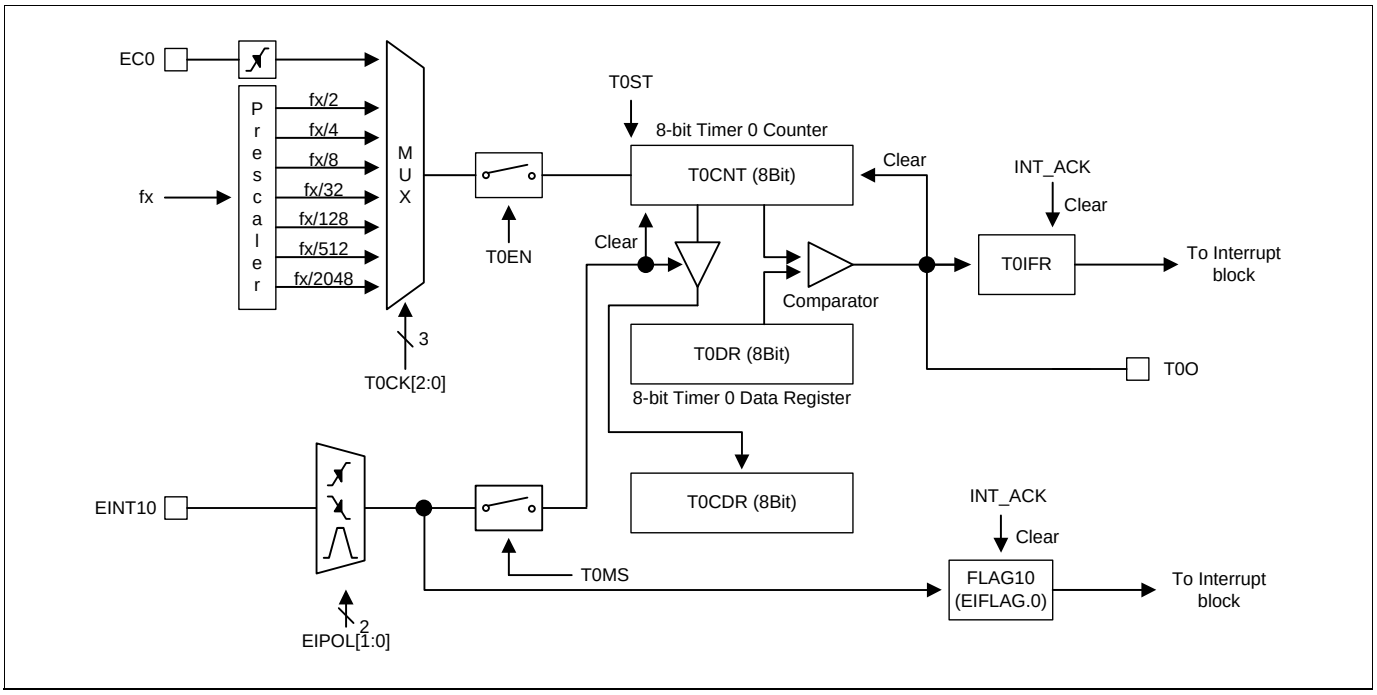


Figure 11.17 8-Bit Timer 0 Block Diagram

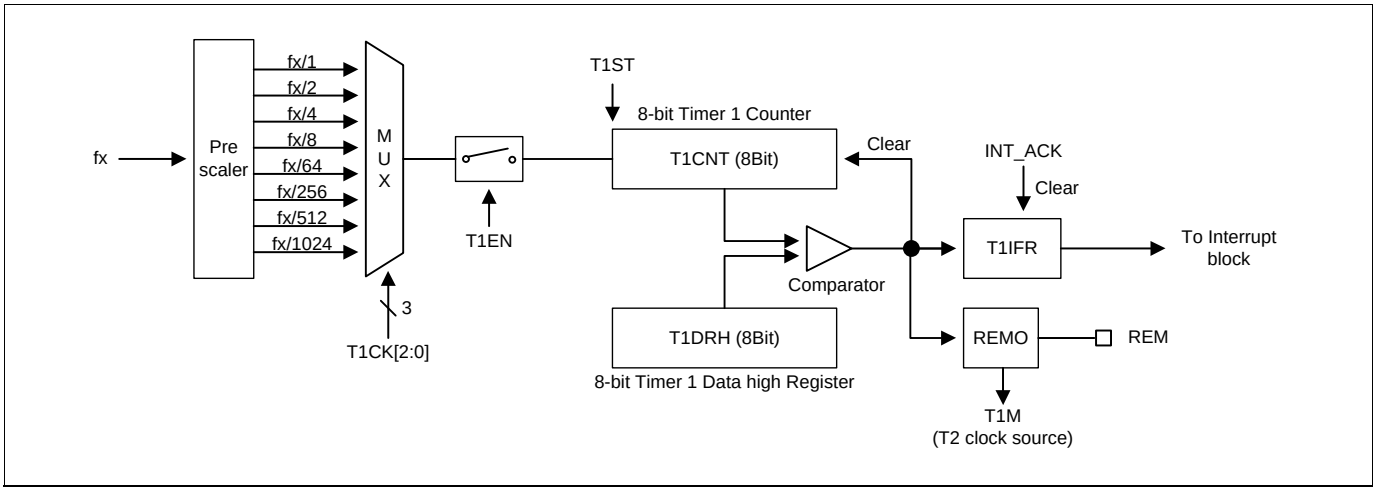


Figure 11.18 8-Bit Timer Counter 1 Block Diagram

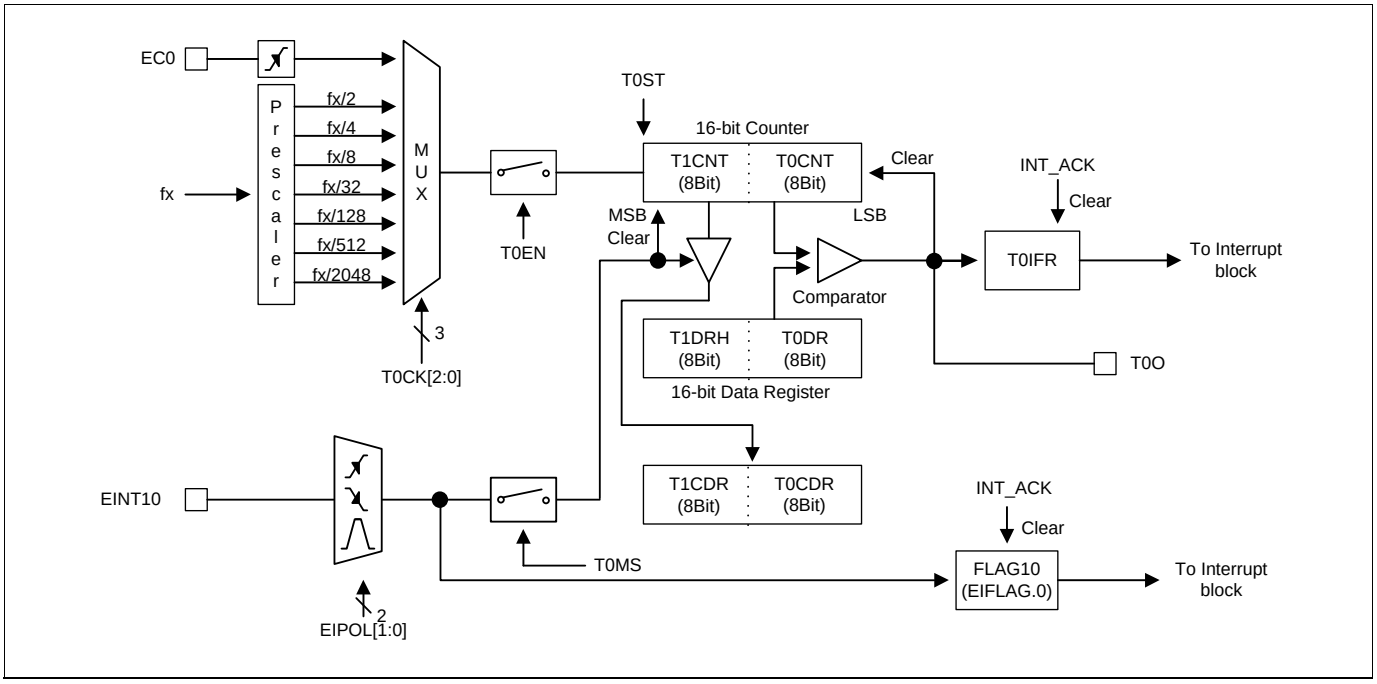


Figure 11.19 16-Bit Timer Counter 0 Block Diagram

11.5.9 Register Map

Name	Address	Dir	Default	Description
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register
T0CDR	B4H	R	00H	Timer 0 Capture Data Register
T0CR	B2H	R/W	00H	Timer 0 Control Register
T1CNT	CBH	R	00H	Timer 1 Counter Register
T1DRH	CDH	R/W	FFH	Timer 1 Data High Register
T1DRL	CCH	R/W	FFH	Timer 1 Data Low Register
T1CDR	CDH	R	00H	Timer 1 Capture Data Register
T1CR	CAH	R/W	00H	Timer 1 Control Register
CARCR	CEH	R/W	00H	Carrier Mode Control Register
TIFR	C3H	R/W	00H	Timer Interrupt Flag Register

Table 11-6. Timer 0, 1 Register Map

11.5.10 Timer Counter 0, 1 Register Description

The timer counter 0, 1 register consists of timer 0 counterregister (T0CNT), timer 0 data register (T0DR), timer 0 capture dataregister (T0CDR), timer 0 controlregister (T0CR), timer 1counterregister (T1CNT), timer 1data high/low register (T1DRH/L), timer 1capture dataregister (T1CDR), timer 1 controlregister (T1CR) and carrier mode control register(CARCR). T0IFR and T1IFR bits are in the timer interrupt flag register (TIFR).

11.5.11 Register Description for Timer Counter 0, 1

T0CNT (Timer 0 Counter Register) : B3H

7	6	5	4	3	2	1	0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value :00H

T0CNT[7:0] T0 Counter

T0DR (Timer 0 Data Register) : B4H

7	6	5	4	3	2	1	0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

T0DR[7:0] T0 Data

T0CDR (Timer 0 Capture Data Register: Read Case, Capture mode only) : B4H

7	6	5	4	3	2	1	0
T0CDR7	T0CDR6	T0CDR5	T0CDR4	T0CDR3	T0CDR2	T0CDR1	T0CDR0
R	R	R	R	R	R	R	R

Initial value :00H

T0CDR[7:0] T0 Capture

T0CR (Timer 0 Control Register) : B2H

7	6	5	4	3	2	1	0
T0EN	–	T0MS	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

T0EN Control Timer 0
- 0 Timer 0 disable
- 1 Timer 0 enable

T0MS Control Timer 0 Operation Mode
- 0 Timer Counter mode
- 1 Capture mode

T0CK[2:0] Select Timer 0 clock source. fx is a system clock frequency

T0CK2	T0CK1	T0CK0	Description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/32
1	0	0	fx/128
1	0	1	fx/512
1	1	0	fx/2048
1	1	1	External Clock (EC0)

T0CN Clear Timer 0 Counter Pause/Continue
- 0 Temporary count stop
- 1 Continue count

T0ST Control Timer 0 Start/Stop
- 0 Counter stop
- 1 Clear counter and start

NOTE)

1. Match Interrupt is generated in Capture mode.

T1CNT (Timer 1Counter Register) : CBH

7	6	5	4	3	2	1	0
T1CNT7	T1CNT6	T1CNT5	T1CNT4	T1CNT3	T1CNT2	T1CNT1	T1CNT0
R	R	R	R	R	R	R	R

Initial value :00H

T1CNT[7:0] T1 Counter

T1DRH (Timer 1 Data High Register) : CDH

7	6	5	4	3	2	1	0
T1DRH7	T1DRH6	T1DRH5	T1DRH4	T1DRH3	T1DRH2	T1DRH1	T1DRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

T1DRH[7:0] T1 Data High

T1DRL (Timer 1 Data Low Register: Carrier mode only) : CCH

7	6	5	4	3	2	1	0
T1DRL7	T1DRL6	T1DRL5	T1DRL4	T1DRL3	T1DRL2	T1DRL1	T1DRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

T1DRL[7:0] T1 Data Low

T1CDR (Timer 1Capture Data Register: Read Case, 16bit Capture mode only) : CDH

7	6	5	4	3	2	1	0
T1CDR7	T1CDR6	T1CDR5	T1CDR4	T1CDR3	T1CDR2	T1CDR1	T1CDR0
R	R	R	R	R	R/	R	R

Initial value :00H

T1CDR[7:0] 16bit T0 Capture

T1CR (Timer 1 Control Register) : CAH

7	6	5	4	3	2	1	0
T1EN	16BIT0	T1MS	T1CK2	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

T1EN Control Timer 1

0 Timer 1 disable

1 Timer 1 enable

16BIT0 Select Timer 0 8/16Bit

0 8 Bit

1 16 Bit

T1MS Control Timer 1 Operation Mode

0 Timer counter mode

1 Carrier mode

T1CK[2:0] Select Timer 1 clock source. fx is main system clock frequency

T1CK2	T1CK1	T1CK0	Description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/4
0	1	1	fx/8
1	0	0	fx/64
1	0	1	fx/256
1	1	0	fx/512
1	1	1	fx/1024

T1CN Control Timer 1 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T1ST Control Timer 1 Start/Stop

0 Counter stop

1 Clear counter and start

CARCR (Carrier Control Register: Carrier mode only) : CEH

7	6	5	4	3	2	1	0
–	–	T1IT1	T1IT0	–	–	CMOD	REMO
–	–	R/W	R/W	–	–	R/W	R/W

Initial value :00H

T1IT[1:0] T1 Interrupt Time Select

T1IT1	T1IT0	Description
0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data value
1	1	Not available

CMOD Carrier Frequency Mode Select

0 One-shot mode

1 Repeating mode

REMO REM Output Control

0 T1DRL→ Low width, T1DRH→ High width

1 T1DRL→ High width, T1DRH→ Low width

TIFR (Timer Interrupt Flag Register) : C3H

7	6	5	4	3	2	1	0
SIOIFR	–	–	–	T3IFR	T2IFR	T1IFR	T0IFR
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

SIOIFR When SIO interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 SIO Interrupt no generation

1 SIO Interrupt generation

T3IFR When T3 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T3 Interrupt no generation

1 T3 Interrupt generation

T2IFR When T2 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T2 Interrupt no generation

1 T2 Interrupt generation

T1IFR When T1 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T1 Interrupt no generation

1 T1 Interrupt generation

T0IFR When T0 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T0 Interrupt no generation

1 T0 Interrupt generation

11.6 Timer 2, 3

11.6.1 Overview

Timer 2 and timer 3 can be used either two 8-bit timer counter or one 16-bit timer counter with combine them. Each 8-bit timer counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register, capture data register and timer interrupt flag register. (T2CNT, T2DR, T2CDR, T2CR, T3CNT, T3DR, T3CDR, T3CR, TIFR).

It has four operating modes:

- 8-bit timercounter mode
- 8-bit capture mode
- 16-bit timercounter mode
- 16-bit capture mode

The timercounter 2 and 3 can be clocked by an internal or an external clock source (EC2).The clock source is selected by clock selection logic which is controlled by the clock selection bits (T2CK[2:0], T3CK[2:0]).

- TIMER2 clock source: f_X/4, 16, 64, 256, 1024, 4096,T1M, EC2
- TIMER3 clock source: f_X/1, 2, 32, 128, 256, 512, 1024, 2048

In the capture mode, by EINT12, the data is captured into input capture data register (T2CDR, T3CDR).
In 8-bit timercounter 2 mode, whenever counter value is equal to T2DR, T2O port toggles. Also In 16-bit timercounter 2 mode, Timer 2 outputs the comparison result between counter and data register through T2O port.

16BIT2	T2MS	T2CK[2:0]	T3CK[2:0]	Timer 2	Timer 3
0	0	XXX	XXX	8 Bit TimerCounter Mode	8 Bit TimerCounter Mode
0	1	XXX	XXX	8 Bit Capture Mode	8 Bit TimerCounter Mode
1	0	XXX	XXX	16 Bit TimerCounter Mode	
1	1	XXX	XXX	16 Bit Capture Mode	

Table 11-7. Timer 2/3Operating Modes

11.6.2 8-Bit Timer Counter 2, 3 Mode

The 8-bit timer counter mode is selected by control register as shown in Figure 11.20.

The two 8-bit timers have each counter and data register. The counter register is increased by internal clock, external clock(EC2) input or T1M. Timer 2 can use the input clock with one of 4, 16, 64, 256, 1024, and 4096 prescaler division rates (T2CK[2:0]). Timer 3 can use the input clock with one of 1, 2, 32, 128, 256, 512, 1024, and 2048 prescaler division rates (T3CK[2:0]). When the value of T2CNT, T3CNT and T2DR, T3DR are respectively identical in Timer 2, 3, the interrupt of Timer 2, 3 occurs.

The external clock (EC2) counts up the timer at the rising edge. If the EC2 is selected as a clock source by T2CK[2:0], EC2port should be set to the input port by P01IO bit.

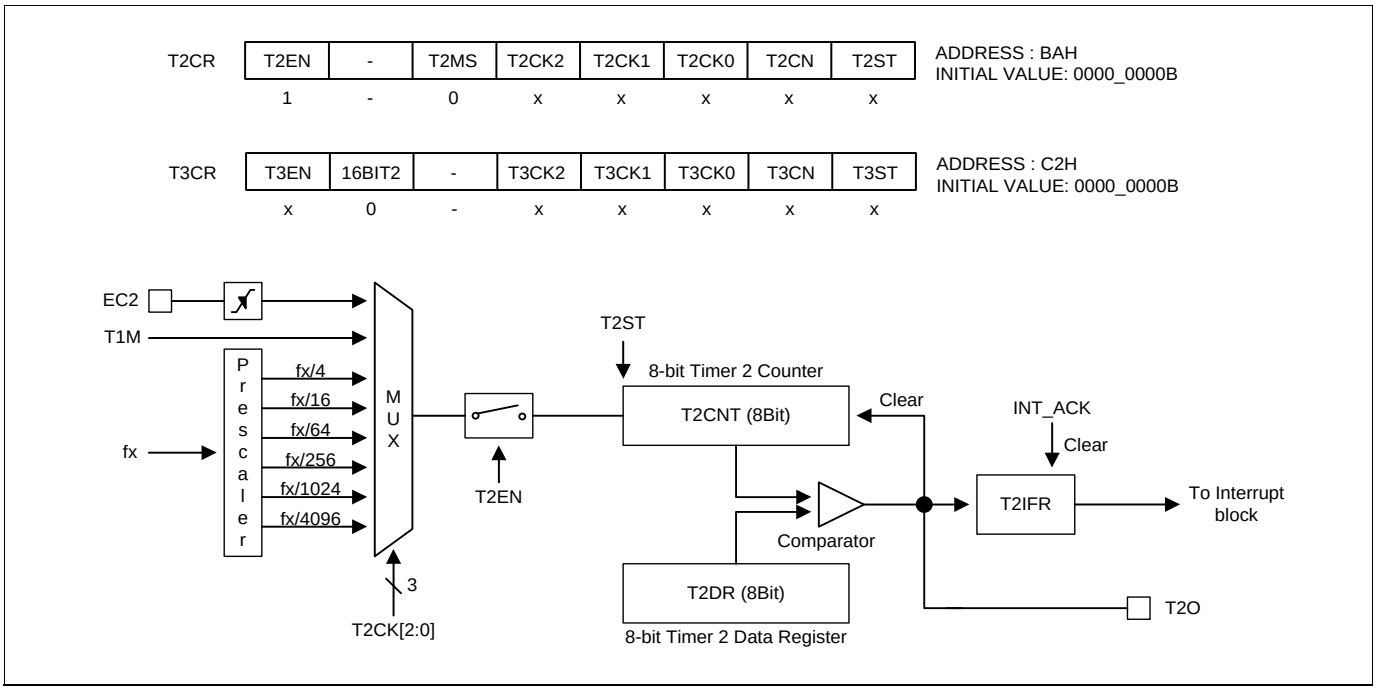


Figure 11.20 8-Bit Timer Counter Mode for Timer 2

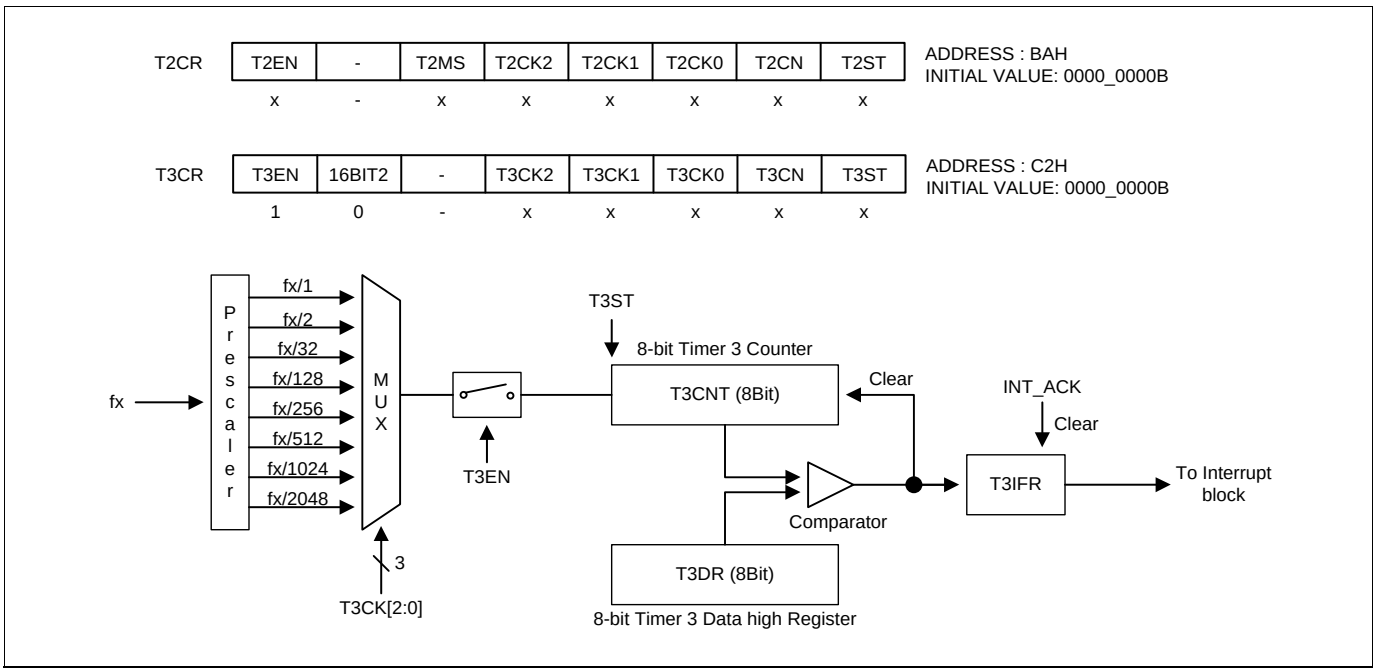


Figure 11.21 8-Bit Timer Counter Mode for Timer 3

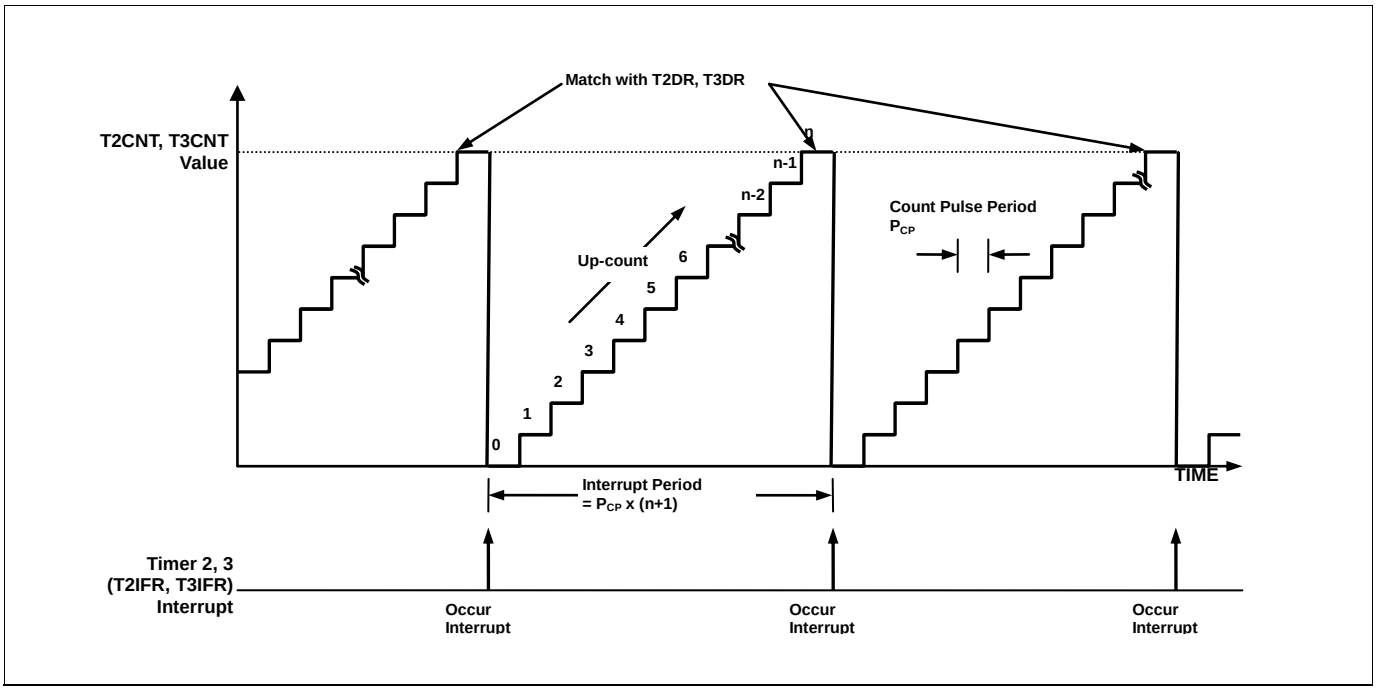


Figure 11.22 8-Bit Timer Counter 2, 3 Example

11.6.3 16-Bit Timer Counter 2 Mode

The 16-bit timercounter mode is selected by control register as shown in Figure 11.23.

The timer register is being run with all 16 bits. A 16-bit timercounter register T2CNT, T3CNT are incrementd 0000H to FFFFH until it matches T2DR, T3DR and then resets to 0000H. The match output generates the Timer 2 interrupt (No Timer 3 interrupt). The clock source is selected from T2CK[2:0] and 16BIT2 bit must be set to '1'. Timer2 is LSB 8-bit, the timer 3 is MSB 8-bit.

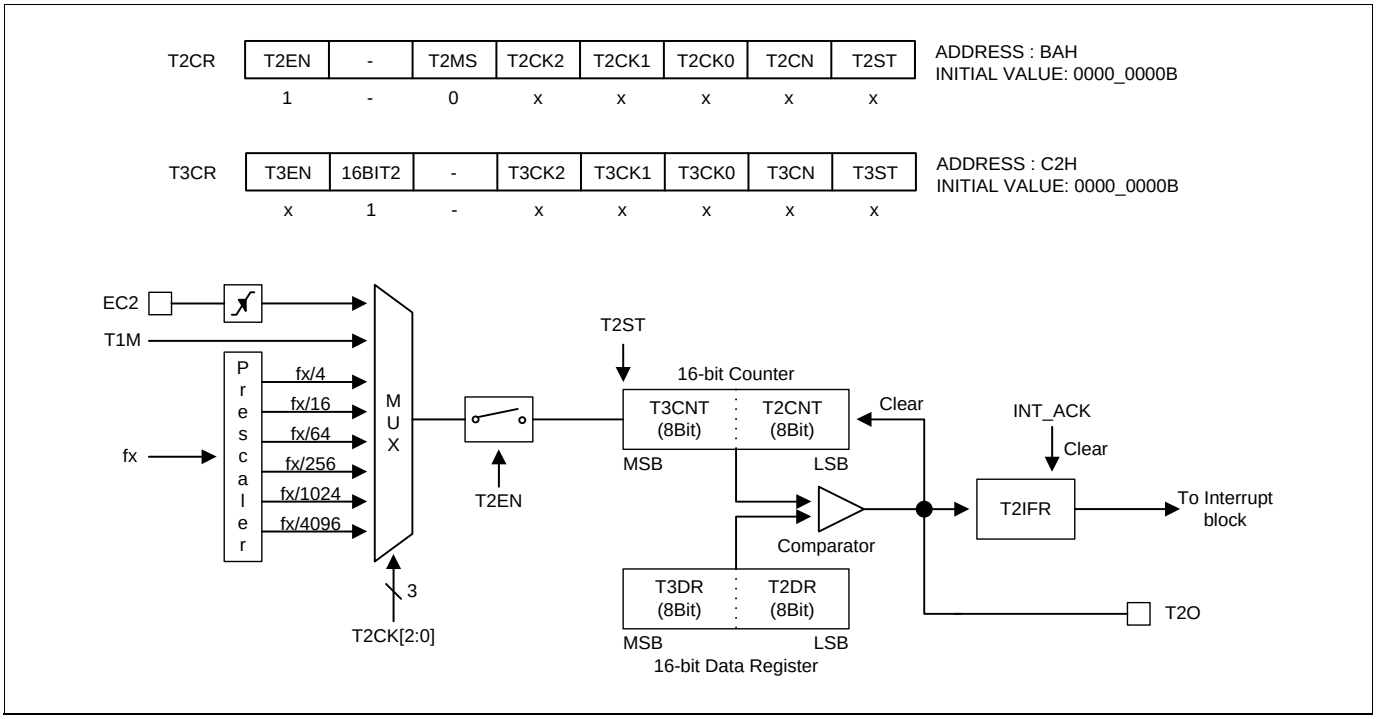


Figure 11.23 16-Bit Timer Counter Mode for Timer 2

11.6.4 8-Bit Timer 2 Capture Mode

The 8-bit Capture mode is selected by control register as shown in Figure 11.24.

The timer 2 capture mode is set by T2MS as '1'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer counter mode and the interrupt occurs when T2CNT is equal to T2DR. T2CNT value is automatically cleared by hardware and it can be also cleared by software (T2ST).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T2CDR. In the timer 2 capture mode, timer 2 output (T2O) waveform is not available.

According to the EIPOL register setting, the external interrupt EINT12 function is chose. Of course, the EINT12 pin must be set to an input port.

T2CDR and T2DRare in the same address. In the capture mode, reading operation reads T2CDR, not T2DR and writing operation will update T2DR.

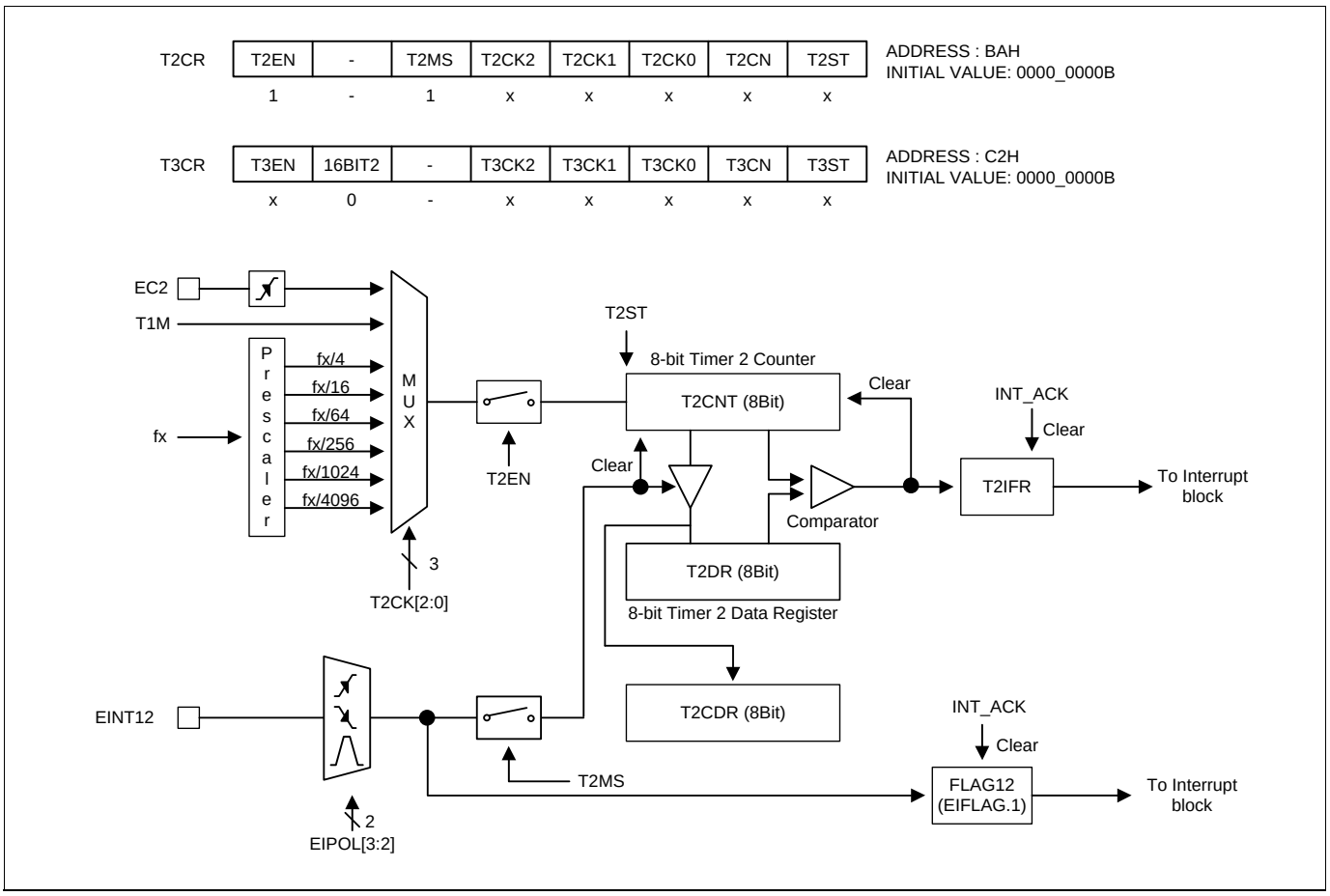


Figure 11.24 8-Bit Capture Mode for Timer 2

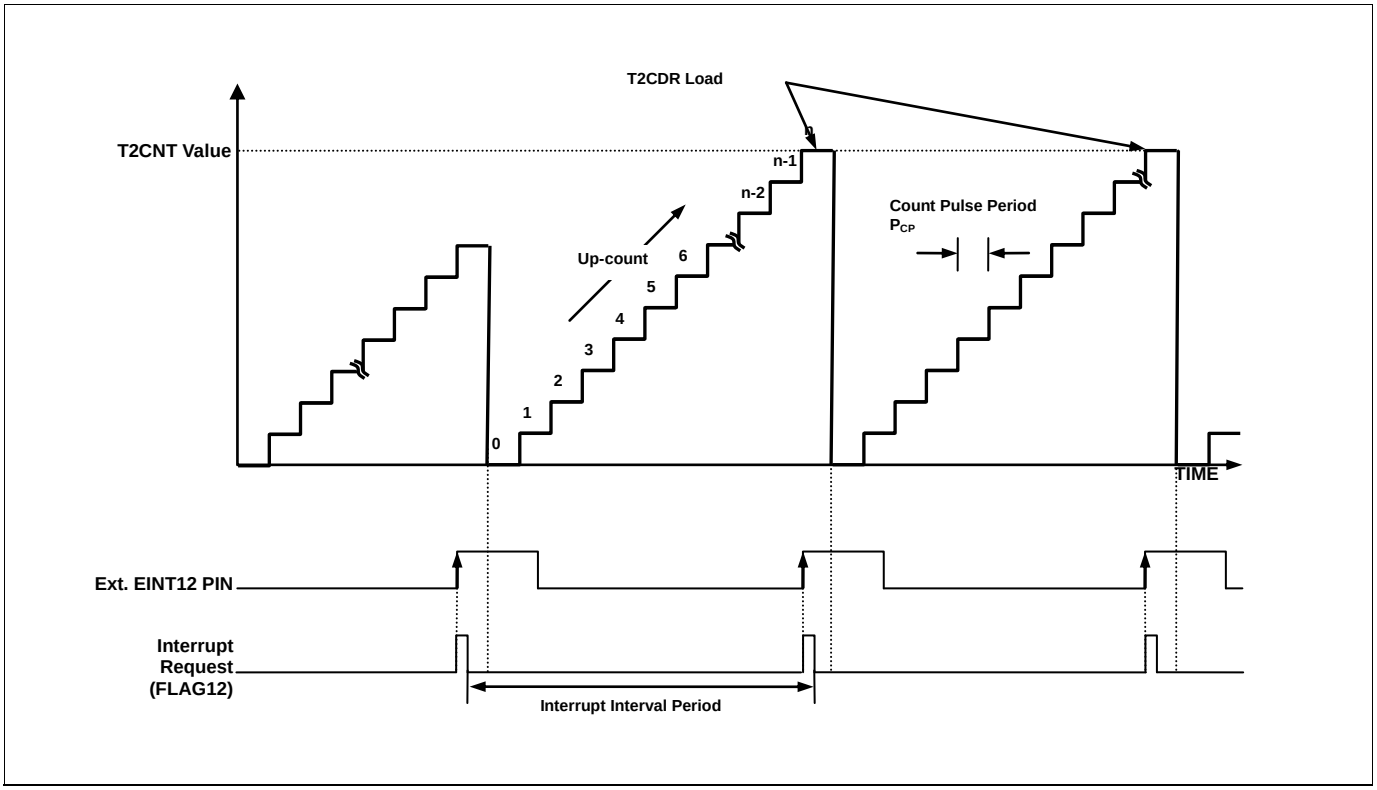


Figure 11.25 Input Capture Mode Operation for Timer 2

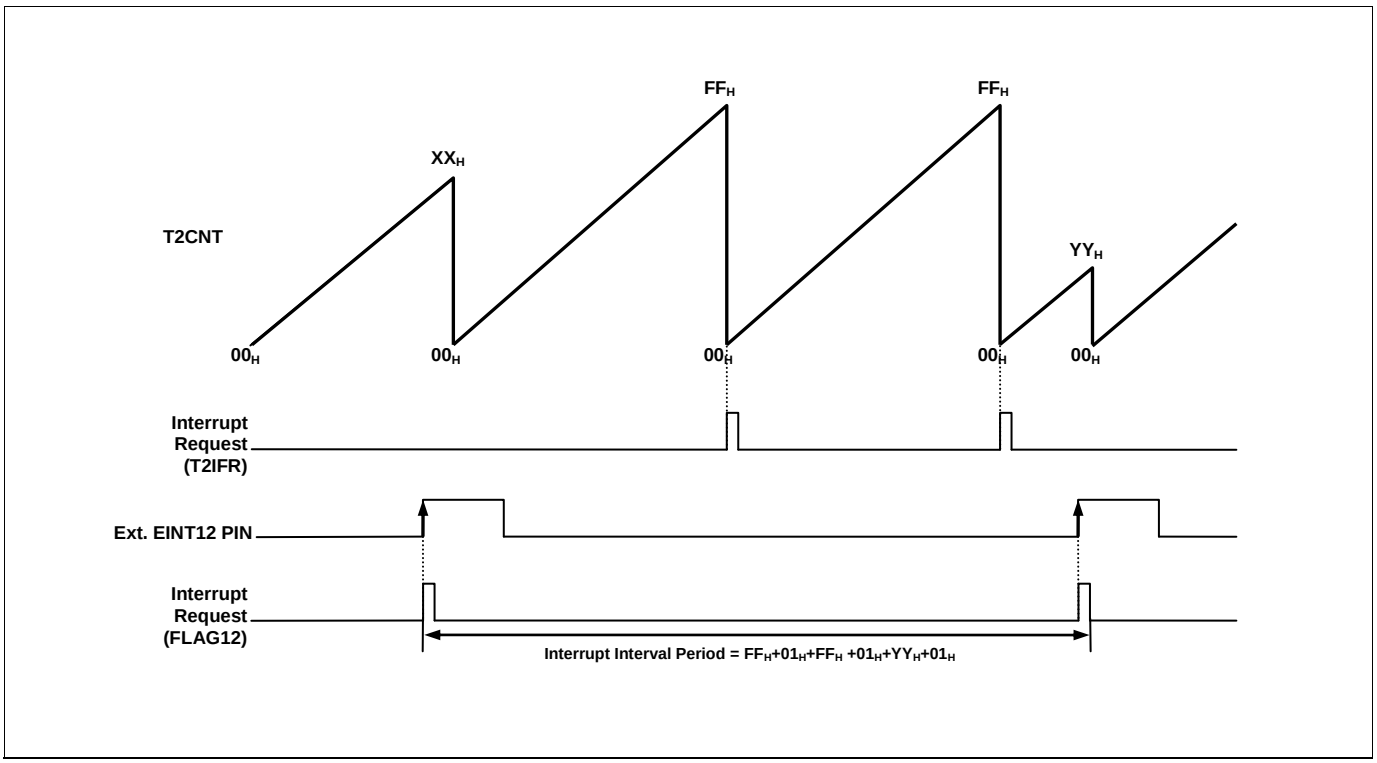


Figure 11.26 Express Timer Overflow in Capture Mode

11.6.5 16-Bit Timer 2 Capture Mode

The 16-bit capture mode is selected by control register as shown in Figure 11.27.

The 16-bit captue mode is the same oeration as 8-bit capture mode, except that the timer register uses 16 bits.The clock source is selected from T2CK[2:0] and 16BIT2 bit must be set to '1'.

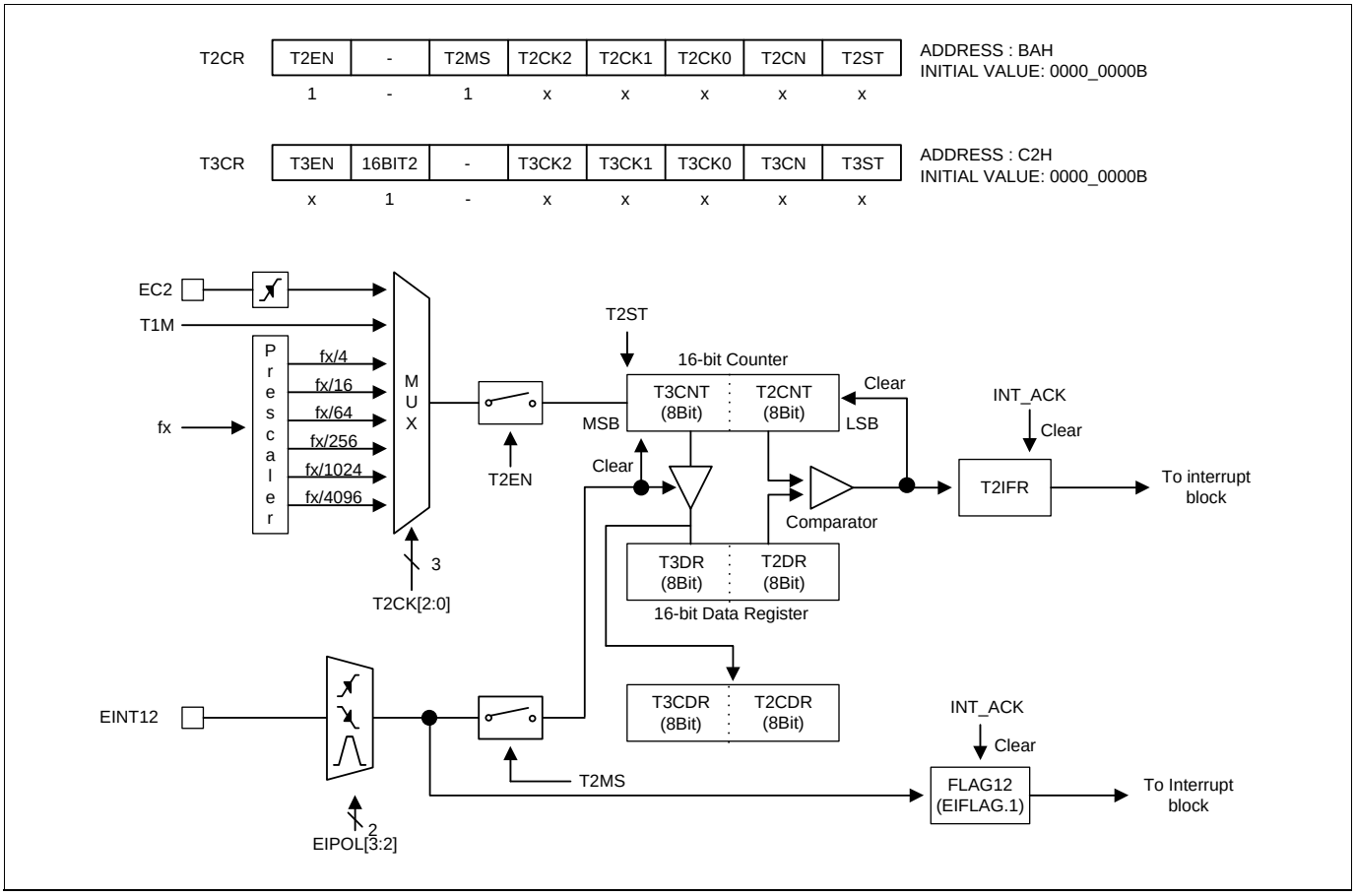


Figure 11.27 16-Bit Capture Mode for Timer 2

11.6.6 Block Diagram

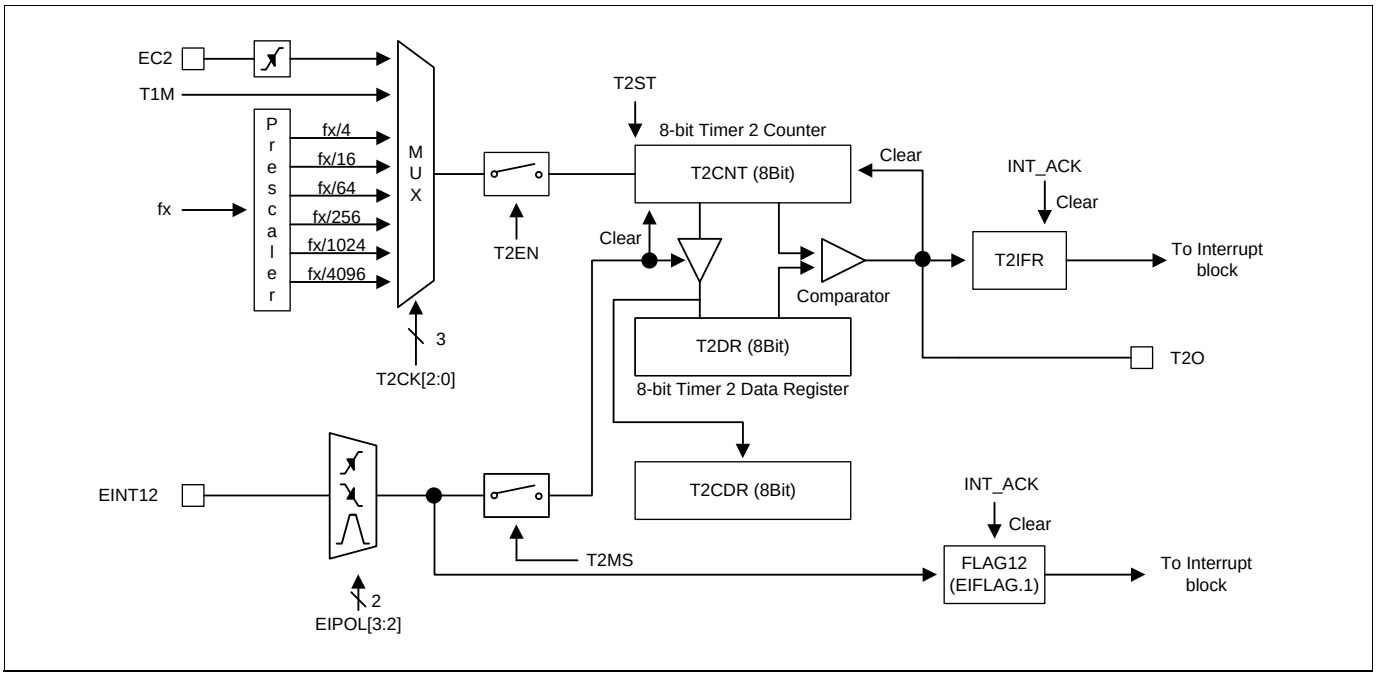


Figure 11.28 8-Bit Timer 2 Block Diagram

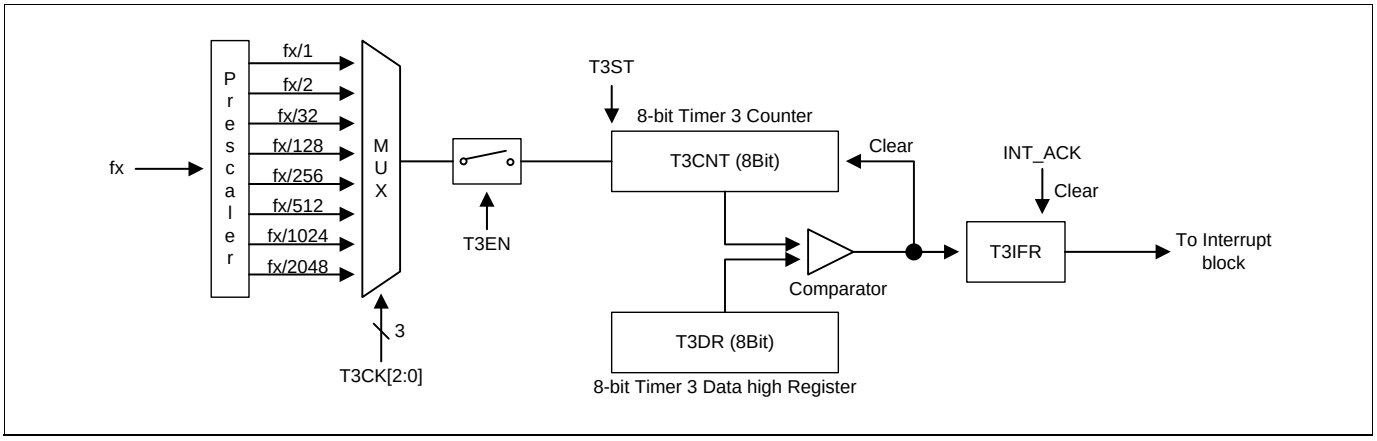


Figure 11.29 8-Bit Timer Counter 3 Block Diagram

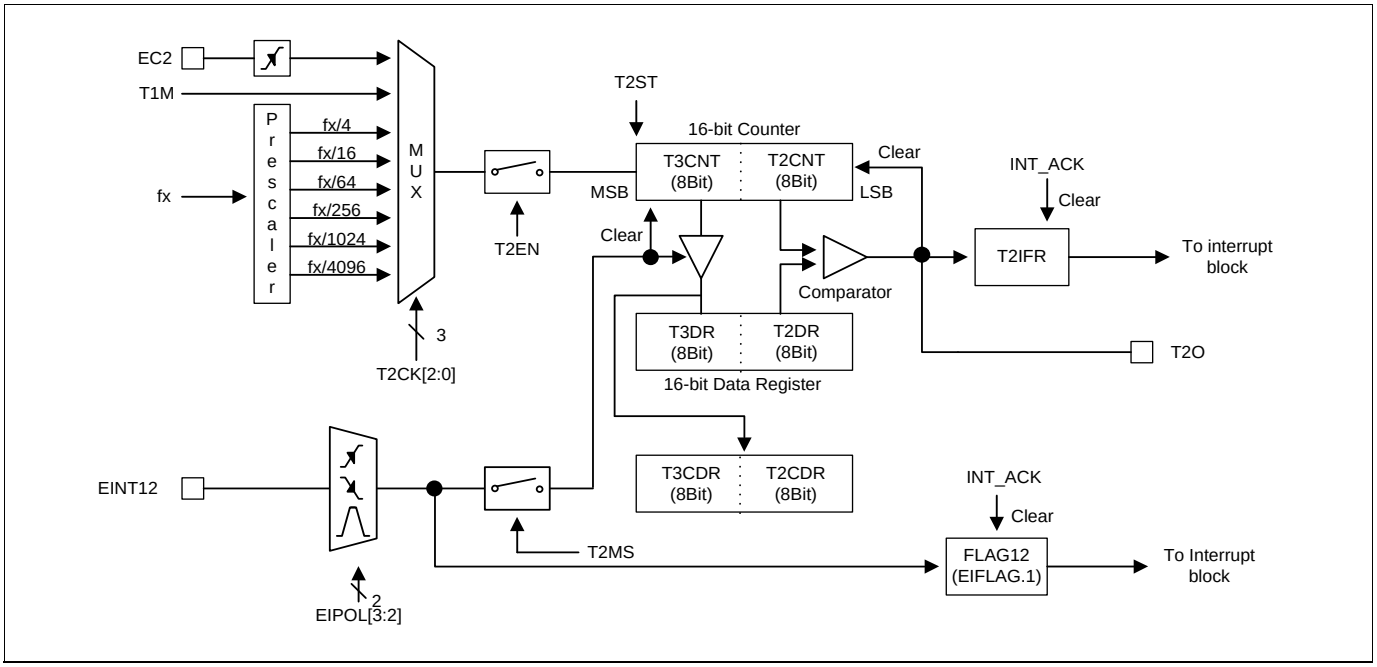


Figure 11.30 16-Bit Timer Counter 2 Block Diagram

11.6.7 Register Map

Name	Address	Dir	Default	Description
T2CNT	BCH	R	00H	Timer 2 Counter Register
T2DR	BEH	R/W	FFH	Timer 2 Data Register
T2CDR	BEH	R	00H	Timer 2 Capture Data Register
T2CR	BAH	R/W	00H	Timer 2 Control Register
T3CNT	C4H	R	00H	Timer 3 Counter Register
T3DR	C6H	R/W	FFH	Timer 3 Data Register
T3CDR	C6H	R	00H	Timer 3 Capture Data Register
T3CR	C2H	R/W	00H	Timer 3 Control Register
TIFR	C3H	R/W	00H	Timer Interrupt Flag Register

Table 11-8. Timer 2, 3 Register Map

11.6.8 Timer Counter 2, 3 Register Description

The timer counter 2, 3 register consists of timer 2counterregister (T2CNT), timer 2data register (T2DR), timer 2capture dataregister (T2CDR), timer 2 controlregister (T2CR), timer 3counterregister (T3CNT), timer 3data register (T3DR), timer 3capture dataregister (T3CDR), timer 3 controlregister (T3CR). T2IFR and T3IFR bits are in the timer interrupt flag register (TIFR).

11.6.9 Register Description for Timer Counter 2, 3

T2CNT (Timer 2Counter Register) : BCH

7	6	5	4	3	2	1	0
T2CNT7	T2CNT6	T2CNT5	T2CNT4	T2CNT3	T2CNT2	T2CNT1	T2CNT0
R	R	R	R	R	R	R	R

Initial value :00H

T2CNT[7:0] T2 Counter

T2DR (Timer 2 Data Register) : BEH

7	6	5	4	3	2	1	0
T2DR7	T2DR6	T2DR5	T2DR4	T2DR3	T2DR2	T2DR1	T2DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

T2DR[7:0] T2 Data

T2CDR (Timer 2 Capture Data Register: Read Case, Capture mode only) : BEH

7	6	5	4	3	2	1	0
T2CDR7	T2CDR6	T2CDR5	T2CDR4	T2CDR3	T2CDR2	T2CDR1	T2CDR0
R	R	R	R	R	R	R	R

Initial value :00H

T2CDR[7:0] T2 Capture

T2CR (Timer 2 Control Register) : BAH

7	6	5	4	3	2	1	0
T2EN	–	T2MS	T2CK2	T2CK1	T2CK0	T2CN	T2ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

T2EN Control Timer 2
- 0 Timer 2 disable
- 1 Timer 2 enable

T2MS Control Timer 2 Operation Mode
- 0 Timer Counter mode
- 1 Capture mode

T2CK[2:0] Select Timer 2 clock source. fx is main system clock frequency

T2CK2	T2CK1	T2CK0	Description
0	0	0	T1M
0	0	1	fx/4
0	1	0	fx/16
0	1	1	fx/64
1	0	0	fx/256
1	0	1	fx/1024
1	1	0	fx/4096
1	1	1	External Clock (EC2)

T2CN Clear Timer 2 Counter Pause/Continue
- 0 Temporary count stop
- 1 Continue count

T2ST Control Timer 2 Start/Stop
- 0 Counter stop
- 1 Clear counter and start

NOTE)

1. Match Interrupt is generated in Capture mode.

T3CNT (Timer 3Counter Register) : C4H

7	6	5	4	3	2	1	0
T3CNT7	T3CNT6	T3CNT5	T3CNT4	T3CNT3	T3CNT2	T3CNT1	T3CNT0
R	R	R	R	R	R	R	R

Initial value :00H

T3CNT[7:0] T3 Counter

T3DR (Timer 3 Data Register) : C6H

7	6	5	4	3	2	1	0
T3DR7	T3DR6	T3DR5	T3DR4	T3DR3	T3DR2	T3DR1	T3DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

T3DR[7:0] T3 Data

T3CDR (Timer 3Capture Data Register: Read Case, 16bit Capture mode only) : C6H

7	6	5	4	3	2	1	0
T3CDR7	T3CDR6	T3CDR5	T3CDR4	T3CDR3	T3CDR2	T3CDR1	T3CDR0
R	R	R	R	R	R/	R	R

Initial value :00H

T3CDR[7:0] 16bit T2 Capture

T3CR (Timer 3Control Register) : C2H

7	6	5	4	3	2	1	0
T3EN	16BIT2	–	T3CK2	T3CK1	T3CK0	T3CN	T3ST
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

T3EN Control Timer 3

0 Timer 3 disable

1 Timer 3 enable

16BIT2 Select Timer 2 8/16Bit

0 8 Bit

1 16 Bit

T3CK[2:0] Select Timer 3 clock source. fx is main system clock frequency

T3CK1	T3CK0	T3CK2	Description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/32
0	1	1	fx/128
1	0	0	fx/256
1	0	1	fx/512
1	1	0	fx/1024
1	1	1	fx/2048

T3CN Control Timer 3 Counter Pause/Continue

0 Temporary count stop

1 Continue count

T3ST Control Timer 3 Start/Stop

0 Counter stop

1 Clear counter and start

TIFR (Timer Interrupt Flag Register) : C3H

7	6	5	4	3	2	1	0
SIOIFR	–	–	–	T3IFR	T2IFR	T1IFR	T0IFR
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

SIOIFR When SIO interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 SIO Interrupt no generation

1 SIO Interrupt generation

T3IFR When T3 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T3 Interrupt no generation

1 T3 Interrupt generation

T2IFR When T2 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T2 Interrupt no generation

1 T2 Interrupt generation

T1IFR When T1 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T1 Interrupt no generation

1 T1 Interrupt generation

T0IFR When T0 interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T0 Interrupt no generation

1 T0 Interrupt generation

11.7 Buzzer Driver

11.7.1 Overview

The Buzzer consists of 8-bit counter,buzzer data register (BUZDR), and buzzer control register (BUZCR). The Square Wave (61.035Hz~125.0kHz @8MHz)is outputted through P02/BUZOpin. The buzzer dataregister (BUZDR) controls the bsuzzer frequency (look at the following expression). In buzzer control register(BUZCR), BUCK[1:0] selects source clock divided by prescaler.

$$f_{BUZ}(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125kHz	62.5kHz	31.25kHz	15.625kHz
0000_0001	62.5kHz	31.25kHz	15.625kHz	7.812kHz
…	…	…	…	…
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

Table 11-9. Buzzer Frequency at 8 MHz

11.7.2 Block Diagram

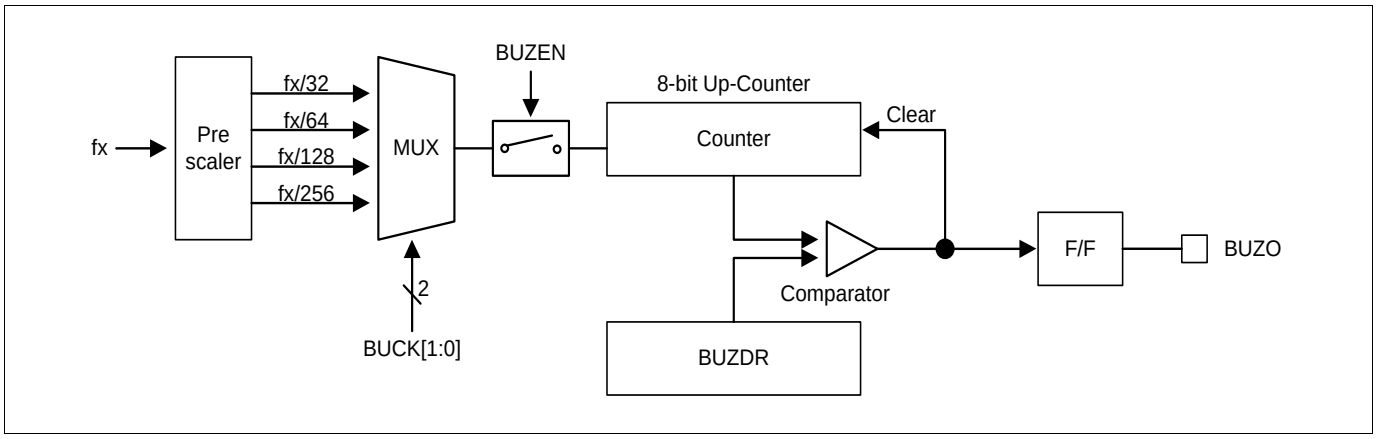


Figure 11.31 Buzzer Driver Block Diagram

11.7.3 Register Map

Name	Address	Dir	Default	Description
BUZDR	8FH	R/W	FFH	Buzzer Data Register
BUZCR	97H	R/W	00H	Buzzer Control Register

Table 11-10. Buzzer Driver Register Map

11.7.4 Buzzer Driver Register Description

Buzzer driver consists of buzzer dataregister (BUZDR) and buzzer control register (BUZCR).

11.7.5 Register Description for Buzzer Driver

BUZDR (Buzzer Data Register) : 8FH

7	6	5	4	3	2	1	0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

BUZDR[7:0] This bits control the Buzzer frequency
Its resolution is 00H ~ FFH

BUZCR (Buzzer Control Register) :97H

7	6	5	4	3	2	1	0
–	–	–	–	–	BUCK1	BUCK0	BUZEN
–	–	–	–	–	R/W	R/W	R/W

Initial value :00H

BUCK[1:0] Buzzer Driver Source Clock Selection

BUCK1	BUCK0	Description
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

BUZEN Buzzer Driver Operation Control

0	Buzzer Driver disable
1	Buzzer Driver enable

NOTE)

1. fx: System clock oscillation frequency.

11.8 SIO

11.8.1 Overview

Theserial input/output is used to transmit/receive 8-bit data serially. The serial input/output(SIO) module is a useful serial interface to communicate with other peripheral of microcontroller devices. This SIO is 8-bit clock synchronous type and consists of SIO pre-scaler register, SIO data register, SIO control register, and control circuit as illustrated in Figure 11.32. The SO pin is designed to input and output. So SIO can operate with two pins minimally. Pin P57/SO, P56/SCK and P55/SI pins are controlled by the SIO control register (SIOCR) and port function selection control registers(P5FSRH and P5IO).The SI pin must be set to input port.

The contents of the SIO data register can be written into or read out by software. The data in the SIO data register can be shifted synchronously with the transfer clock signal. SIO data register (SIODR) is an 8 bit shift register. MSB-first and LSB-first transfers are possible.

11.8.2 Block Diagram

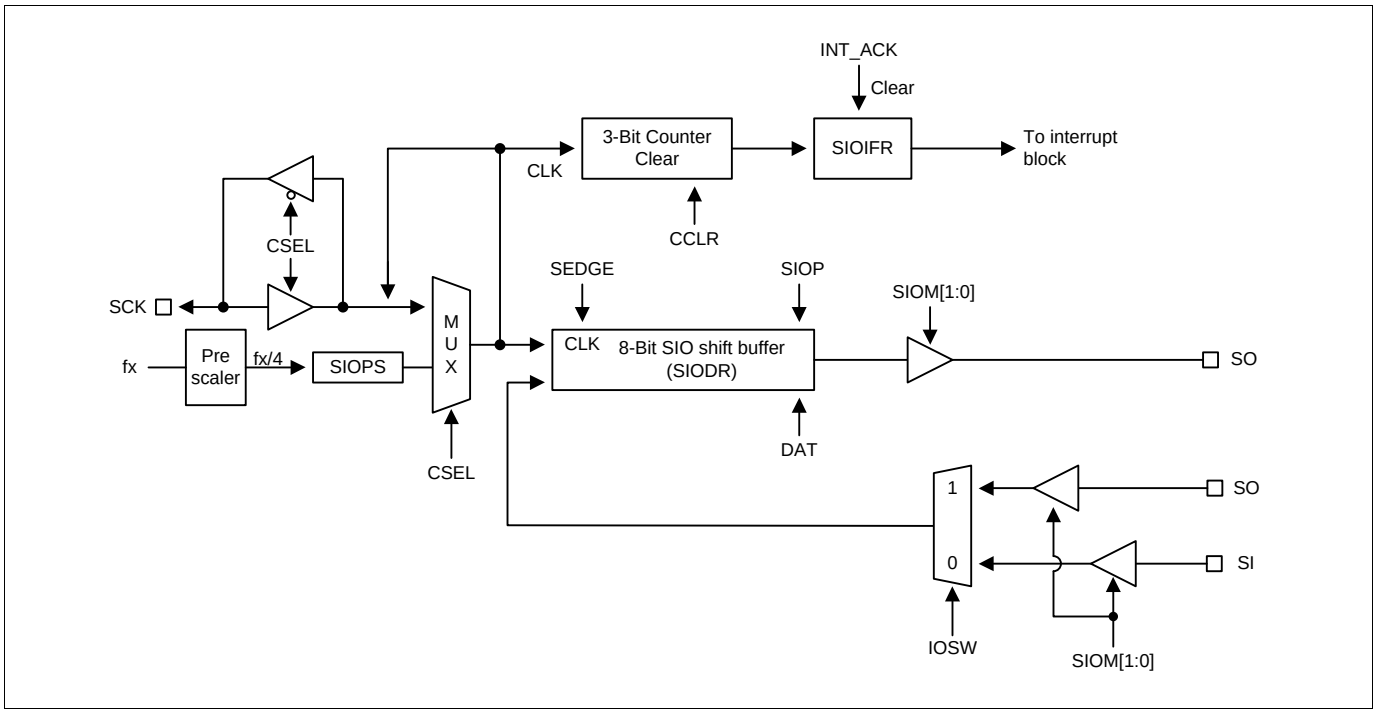


Figure 11.32 SIO Block Diagram

NOTE)

1. The system clock should be greater than the SIO input clock. So, take care of using the external clock.

11.8.3 SIO Pre-Scale Register (SIOPS)

SIOPS contains the SIO pre-scaler value. The SIO clock rate (baud rate) is calculated by the following formula.

Baud rate = Input clock (fx/4)/(Pre-scaler value + 1)

orSCK input clock, where the input clock is fx/4

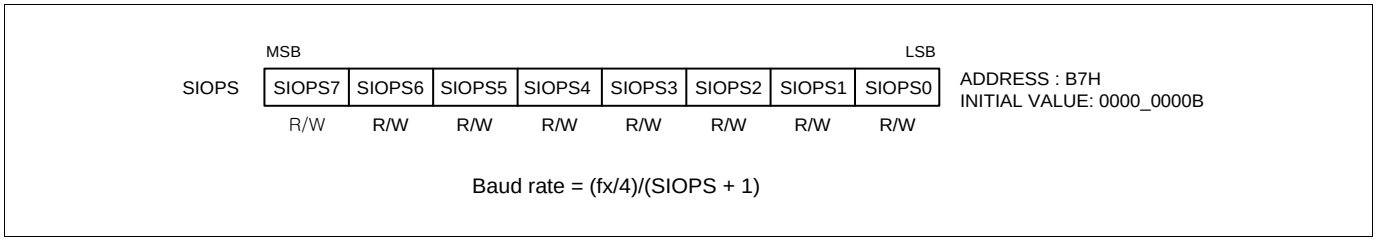


Figure 11.33 SIO Pre-Scale Register (SIOPS)

11.8.4 The usage of SIO

1. Select transmitter/receiver mode.
2. In transmitter mode, write data to be sent to SIODR.
3. Set CCLR to “1” to clear SIO counter and start shifting.
4. If Tx or Rx is completed, the SIO interrupt is generated and SIOIFR is set to “1”.
5. In receiver mode, the received data can be acquired by reading SIODR.

11.8.5 SIO Timing Diagram

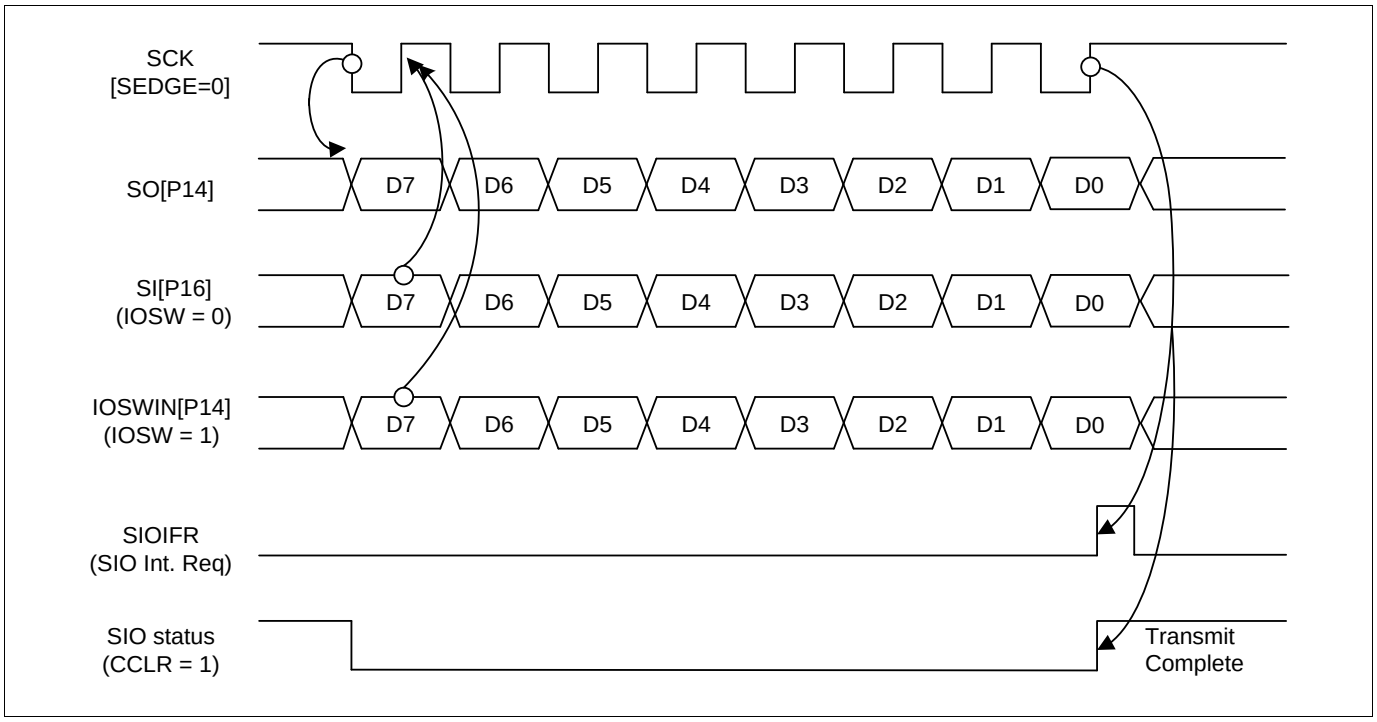


Figure 11.34 SIO Timing Diagram at SEDGE=0

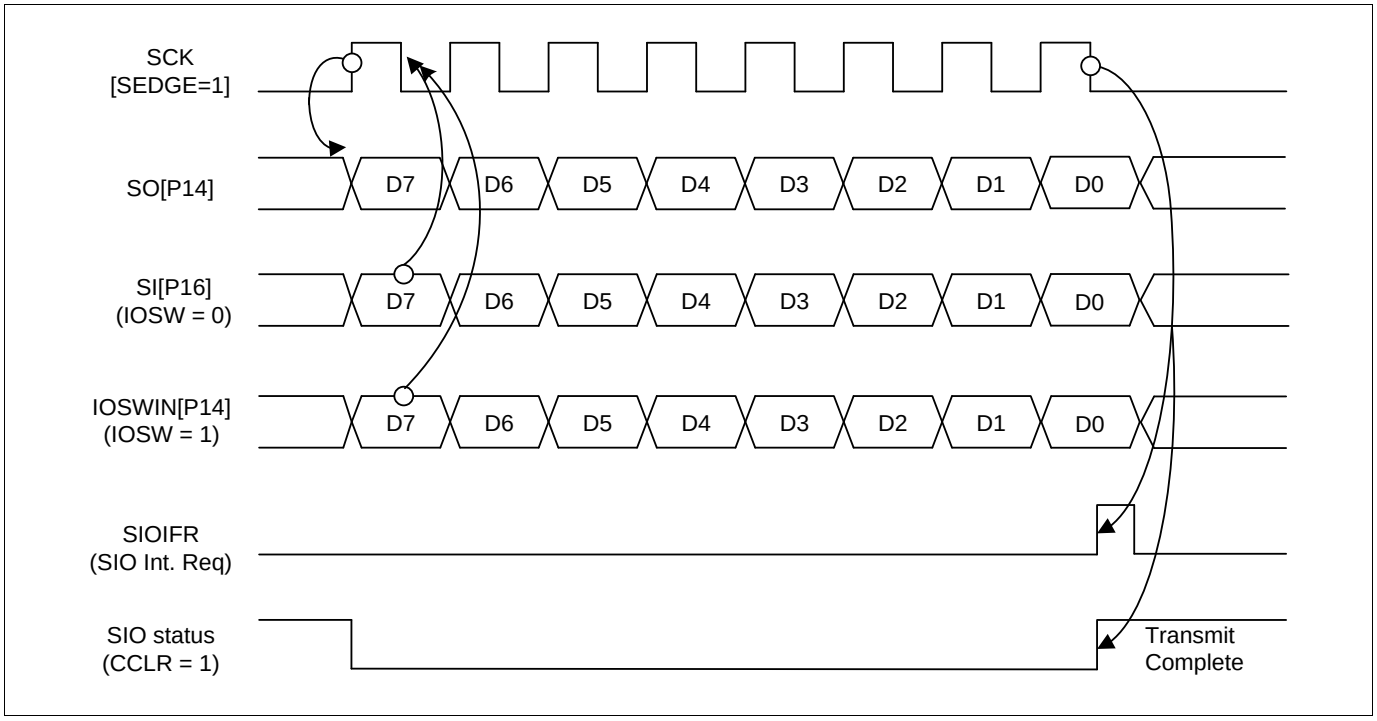


Figure 11.35 SIO Timing Diagram at SEDGE=1

11.8.6 Register Map

Name	Address	Dir	Default	Description
SIOPS	B7H	R/W	00H	SIO Pre-scale Register
SIODR	B6H	R/W	00H	SPI Data Register
SIOCR	B5H	R/W	00H	SIO Control Register

Table 11-11. SIO Register Map

11.8.7 SIO Register Description

The SIOregister consists of SIOpre-scaler register (SIOPS), SIOData Register (SIODR), and SIO control register (SIOCR).The SIOIFR bit is in the timer interrupt flag register (TIFR).

11.8.8 Register Description for SIO

SIOPS (SIO Pre-scaler Register) :B7H

7	6	5	4	3	2	1	0
SIOPS7	SIOPS6	SIOPS5	SIOPS4	SIOPS3	SIOPS2	SIOPS1	SIOPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

SIOPS [7:0] SIO Pre-scale
Baud Rate = (fx/4)/(SIOPS+1)

SIODR (SIO Data Register) :B6H

7	6	5	4	3	2	1	0
SIODR7	SIODR6	SIODR5	SIODR4	SIODR3	SIODR2	SIODR1	SIODR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

SIODR [7:0] SIO Data

SIOCR (SIO Control Register) :B5H

7	6	5	4	3	2	1	0
CSEL	DAT	SIOP	IOSW	SIOM1	SIOM0	CCLR	SEDGE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

CSEL SIO Shift Clock Selection

0 Internal clock (P.S clock)

1 External clock (SCK)

DAT Data Direction Control

0 MSB first mode

1 LSB first mode

SIOP SIO Shift Operation Enable

0 Disable shifter and clock counter

1 Enable shifter and clock counter

IOSW Serial Input Pin Selection Bit

0 SI pin selection

1 SO pin selection

NOTE)

1. If SO pin is selected for a serial data input, SO pin should be set to an input and port. So, the SIOM, P5FSRH[6:5] and P57IO bits should be set to '01b', '00b' and '0b' respectively. Refer to the P5IO and P5FSRH register for setting

SIOM[1:0] SIO Mode Selection

SIOM1	SIOM0	Description
0	0	Transmit mode
0	1	Receive mode
1	x	Transmit/Receive mode

CCLR SIO Counter Clear and Shift Start

0 No action

1 Clear 3-bit counter and start shifting

SEDGE SIO Clock Edge Selection

0 Tx at falling edges, Rx at rising edges

1 Tx at rising edge, Rx at falling edges

NOTE)

1. The serial I/O interrupt flag (SIOIFR bit) is in the timer interrupt flag register (TIFR register).

11.9 UART

11.9.1 Overview

The universal asynchronous serial receiver and transmitter (UART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete

UART has baud rategenerator, transmitter and receiver. The baud rate generator for asynchronous operation.The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats.The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (UARTDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

11.9.2 Block Diagram

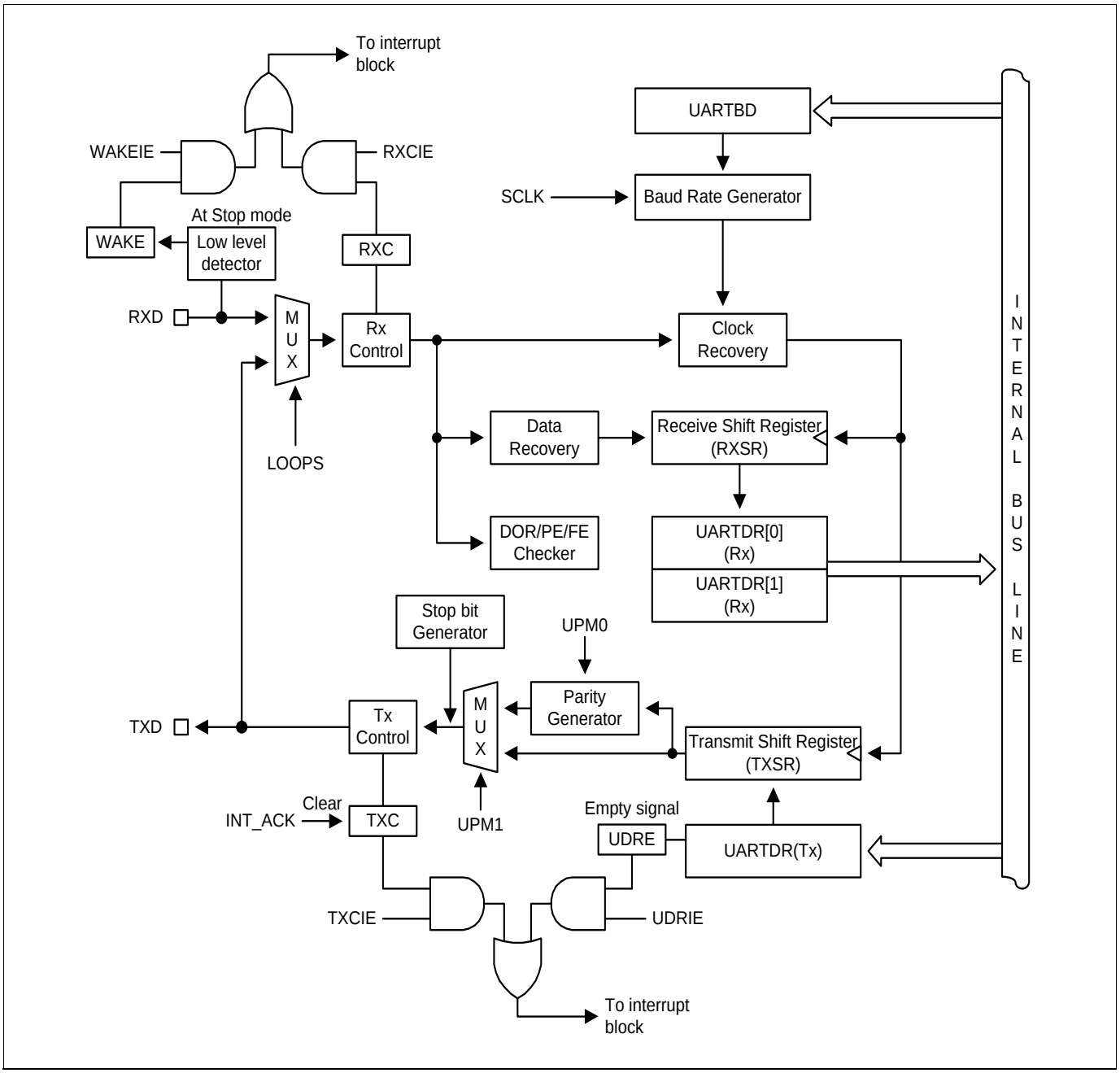


Figure 11.36 UART Block Diagram

11.9.3 Clock Generation

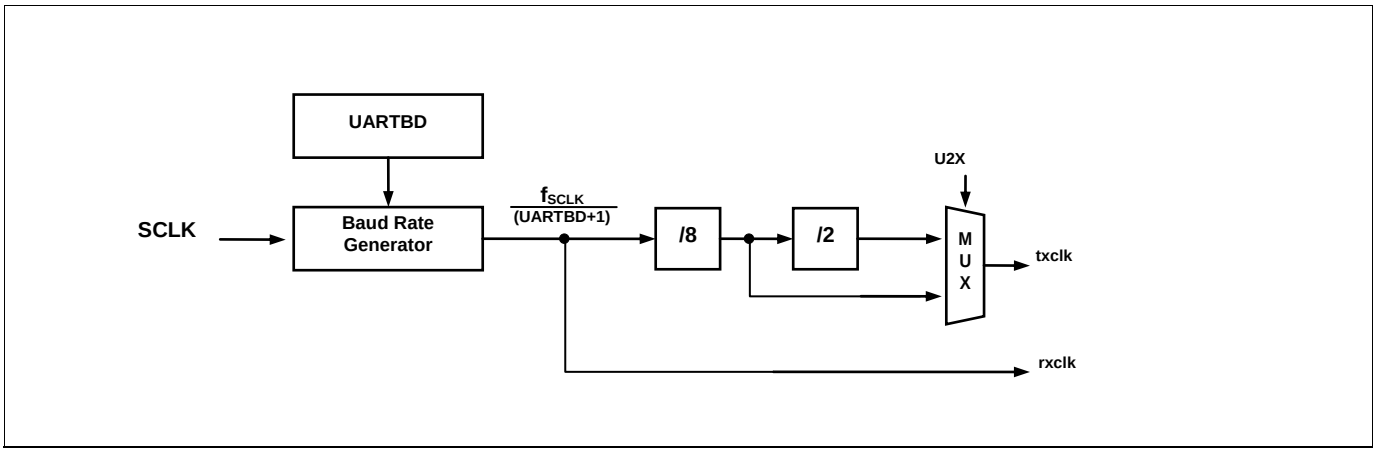


Figure 11.37 Clock Generation Block Diagram

The clock generation logic generates the base clock for the transmitter and receiver.

Following table shows equations for calculating the baud rate (in bps).

Operating Mode	Equation for Calculating Baud Rate
Normal Mode(U2X=0)	$\text{Baud Rate} = \frac{\text{fx}}{16(\text{UARTBD}+1)}$
Double Speed Mode(U2X=1)	$\text{Baud Rate} = \frac{\text{fx}}{8(\text{UARTBD}+1)}$

Table 11-12. Equations for Calculating Baud Rate Register Setting

11.9.4 Data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error detection.

The UART supports all 30 combinations of the following as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- no, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by the least significant data bit (LSB). Then the next data bits, up to nine, are succeeding, ending with the most significant bit (MSB). If parity function is enabled, the parity bit is inserted between the last data bit and the stop bit. A high-to-low transition on data pin is considered as start bit.When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle state. The idle means high state of data pin. The following figure shows the possible combinations of the frame formats. Bits inside brackets are optional.

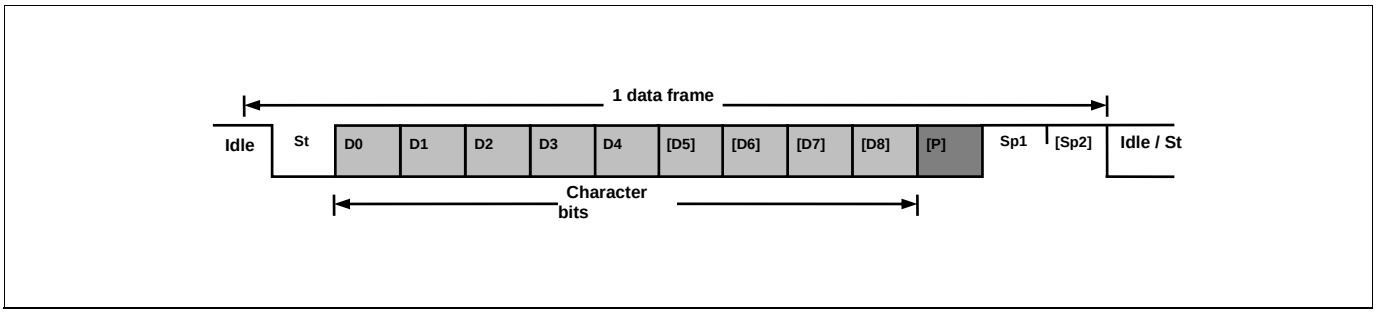


Figure 11.38 Frame Format

1 data frame consists of the following bits

- Idle No communication on communication line (TxD/RxD)
- St Start bit (Low)
- Dn Data bits (0~8)
- Parity bit ---------- Even parity, Odd parity, No parity
- Stop bit(s) ---------- 1 bit or 2 bits

The frame format used by the UART is set by the USIZE[2:0], UPM[1:0] and USBS bits in UARTCR1 and UARTCR3register. The Transmitter and Receiver use the same setting.

11.9.5 Parity bit

The parity bit is calculated by doing an exclusive-OR of all the data bits. If odd parity is used, the result of the exclusive-or is inverted. The parity bit is located between the MSB and first stop bit of a serial frame.

$P_{even} = D_{n-1} \wedge \ldots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 0$

$P_{odd} = D_{n-1} \wedge \ldots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 1$

P_{even} : Parity bit using even parity

P_{odd} : Parity bit using odd parity

D_n : Data bit n of the character

11.9.6 UART Transmitter

The UART transmitter is enabled by setting the TXE bit in UARTCR2register.When the Transmitter is enabled, the TXD pin should be set to TXD function for the serial output pin of UART by the P5FSRH[4:3].The baud-rate, operation mode and frame format must be setup once before doing any transmission.

11.9.6.1 Sending Tx data

A data transmission is initiated by loading the transmit buffer (UARTDRregister I/O location) with the data to be transmitted.The data written in transmit buffer is moved to the shift register when the shift register is ready to send a new frame.The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded with new data, it will transfer one complete frame according to the settings of control registers.If the 9-bit characters are used, the ninth bit must be written to the TX8 bit in UARTCR3 register before it is loaded to the transmit buffer (UARTDR register).

11.9.6.2 Transmitter flag and interrupt

The UART transmitter has 2 flags which indicate its state.One is UART data register empty flag (UDRE) and the other is transmit complete flag (TXC). Both flags can be interrupt sources.

UDRE flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains data to be transmitted but has not yet been moved into the shift register. And also this flag can be cleared by writing ‘0’ to this bit position. Writing ‘1’ to this bit position is prevented.

When the data register empty interrupt enable (UDRIE) bit in UARTCR2 register is set and the global interrupt isenabled, UART data register empty interrupt is generated while UDRE flag is set.

The transmit complete (TXC) flag bit is set when the entire frame in the transmit shift register has been shifted out and there is no more data in the transmit buffer. The TXC flag is automatically cleared when the transmit complete interrupt service routine is executed, or it can be cleared by writing ‘0’ to TXC bit in UARTST register.

When the transmit complete interrupt enable (TXCIE) bit in UARTCR2 register is set and the global interrupt is enabled,UART transmit complete interrupt is generated while TXC flag is set.

11.9.6.3 Parity Generator

The parity generator calculates the parity bit for the serial frame data to be sent. When parity bit is enabled (UPM[1]=1), the transmitter control logic inserts the parity bit between the MSB and the first stop bit of the frame to be sent.

11.9.6.4 Disabling Transmitter

Disabling the transmitter by clearing the TXE bit will not become effective until ongoing transmission is completed. When the Transmitter is disabled, the TXD pin can be used as a normal general purpose I/O (GPIO).

11.9.7 UART Receiver

The UART receiver is enabled by setting the RXE bit in the UARTCR2register. When the receiver is enabled, the RXD pin should be set to the input port for the serial input pin of UARTby P57IO bit.The baud-rate, mode of operation and frame format must be set before serial reception.

11.9.7.1 Receiving Rx data

The receiver starts data reception when it detects a valid start bit (LOW) on RXD pin. Each bit after start bit is sampled at pre-defined baud-rate (asynchronous) and shifted into the receive shift register until the first stop bit of a frame is received. Even if there's 2^{nd} stop bit in the frame, the 2^{nd} stop bit is ignored by the receiver.That is, receiving the first stop bit means that a complete serial frame is present in the receiver shift register and contents of the shift register are to be moved into the receive buffer. The receive buffer is read by reading the UARTDR register.

If 9-bit characters are used (USIZE[2:0] = "111"), the ninth bit is stored in the RX8 bit position in the UARTCR3 register. The 9^{th} bit must be read from the RX8 bit before reading the low 8 bits from the UARTDR register.Likewise, the error flags FE, DOR, PE must be read before reading the data from UARTDR register. It's because the error flags are stored in the same FIFO position of the receive buffer.

11.9.7.2 Receiver Flag and Interrupt

The UARTreceiver has one flag that indicates the receiver state.

The receive complete (RXC) flag indicates whether there are unread data in the receive buffer. This flag is set when there are unread data in the receive buffer and cleared when the receive buffer is empty.If the receiver is disabled (RXE=0), the receiver buffer is flushed and the RXC flag is cleared.

When the receive complete interrupt enable (RXCIE) bit in the UARTCR2 register is set and global interrupt is enabled, the UART receiver complete interrupt is generated while RXC flag is set.

The UART receiver has three error flags which are frame error (FE), data overrun (DOR) and parity error (PE). These error flags can be read from the UARTST register. As received data are stored in the 2-level receive buffer, these error flags are also stored in the same position of receive buffer. So, before reading received data from UARTDR register, read the UARTST register first which contains error flags.

The frame error (FE) flag indicates the state of the first stop bit. The FE flag is '0' when the stop bit was correctly detected as '1', and the FE flag is '1' when the stop bit was incorrect, i.e. detected as '0'. This flag can be used for detecting out-of-sync conditions between data frames.

The data overrun (DOR) flag indicates data loss due to a receive buffer full condition. DOR occurs when the receive buffer is full, and another new data is present in the receive shift register which are to be stored into the receive buffer. After the DOR flag is set, all the incoming data are lost. To prevent data loss or clear this flag, read the receive buffer.

The parity error (PE) flag indicates that the frame in the receive buffer had a parity error when received. If parity check function is not enabled (UPM[1]=0), the PE bit is always read '0'.

11.9.7.3 Parity Checker

If parity bit is enabled (UPM[1]=1), the Parity Checker calculates the parity of the data bits in incoming frame and compares the result with the parity bit from the received serial frame.

11.9.7.4 Disabling Receiver

In contrast to transmitter, disabling the Receiver by clearing RXE bit makes the Receiver inactive immediately. When the receiver is disabled, the receiver flushes the receive buffer, the remaining data in the buffer is all reset, andthe RXD pin can be used as a normal general purpose I/O (GPIO).

11.9.7.5 Asynchronous Data Reception

To receive asynchronous data frame, the UART includes a clock and data recovery unit. Theclock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXD pin.

The data recovery logic samples and low pass filters the incoming bits, and this removes the noise of RXD pin.

The next figure illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times the baud-rate for normal mode (U2X=0) and 8 times the baud-rate for double speed mode (U2X=1). The horizontal arrows show the synchronization variation due to the asynchronous sampling process. Note that larger time variation is shown when using the double speed mode.

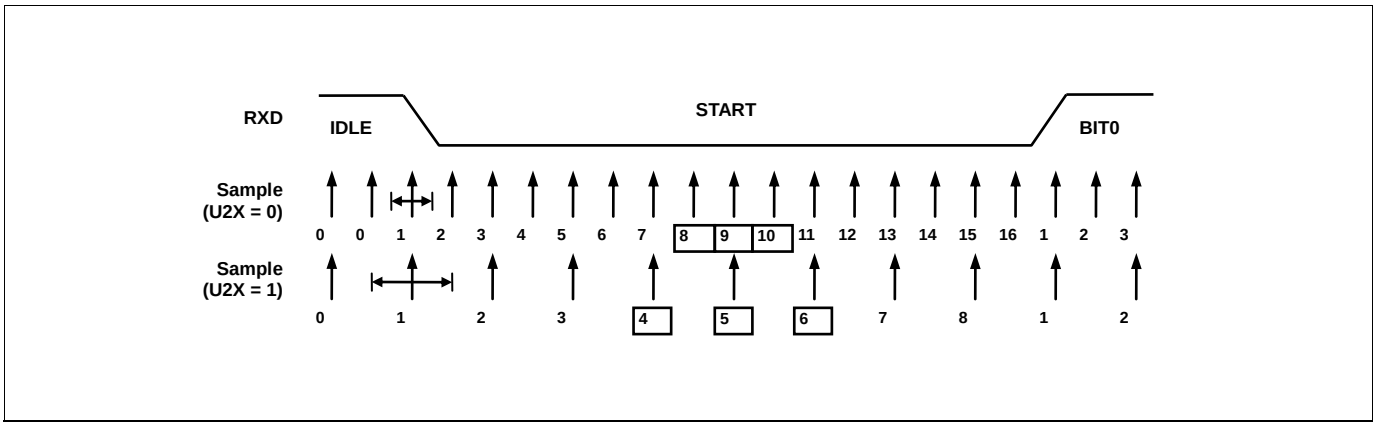


Figure 11.39 Start Bit Sampling

When the receiver is enabled (RXE=1), the clock recovery logic tries to find a high-to-low transition on the RXD line, the start bit condition. After detecting high to low transition on RXD line, the clock recovery logic uses samples 8,9, and 10 for normal mode, and samples 4, 5, and 6 for double speed mode to decide if a valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. And the data recovery can begin. The synchronization process is repeated for each start bit.

As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost similar to the clock recovery process. The data recovery logic samples 16 times for each incoming bits for normal mode and 8 times for double speed mode.And uses sample 8, 9, and 10 to decide data value for normal mode, and samples 4, 5, and 6 for double speed mode.If more than 2 samples have low levels, the received bit is considered to a logic ‘0’ and if more than 2 samples have high levels, the received bit is considered to a logic ‘1’. The data recovery process is then repeated until a complete frame is received including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the Receiver is in idle state and waiting to find start bit.

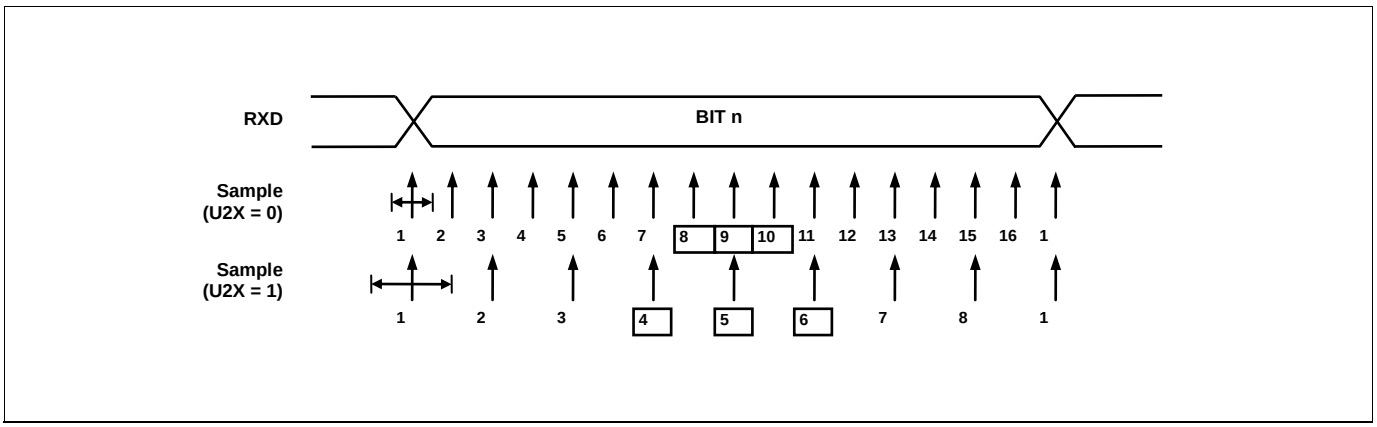


Figure 11.40 Sampling of Data and Parity Bit

The process for detecting stop bit is like clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, else a frame error (FE) flag is set. After deciding whether the first stop bit is valid or not, the Receiver goes to idle state and monitors the RXD line to check a valid high to low transition is detected (start bit detection).

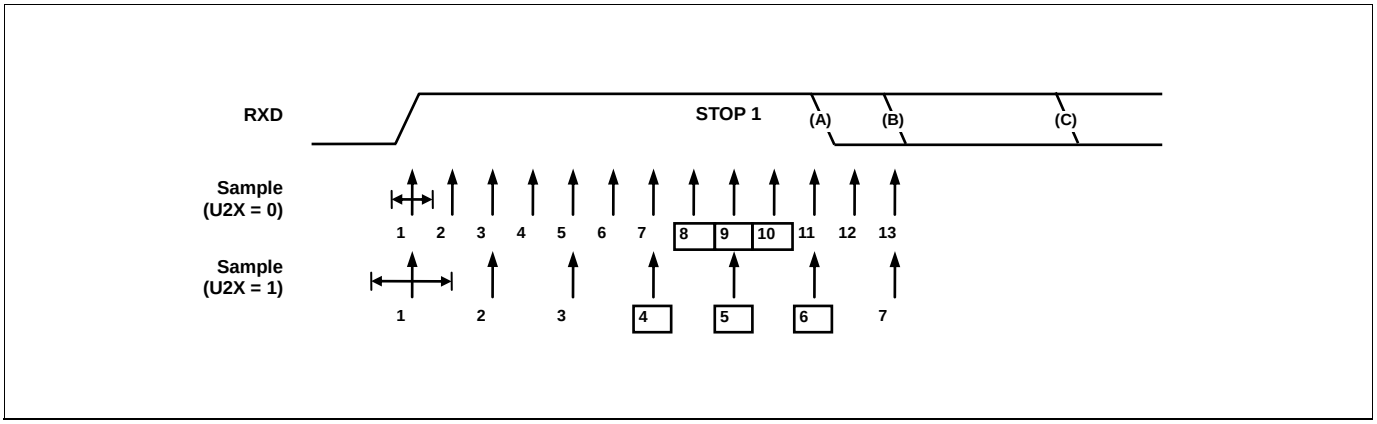


Figure 11.41 Stop Bit Sampling and Next Start Bit Sampling

11.9.8 Register Map

Name	Address	Dir	Default	Description
UARTBD	E6H	R/W	FFH	UART Baud Rate Generation Register
UARTDR	EFH	R/W	00H	UART Data Register
UARTCR1	E2H	R/W	00H	UART Control Register 1
UARTCR2	E3H	R/W	00H	UART Control Register 2
UARTCR3	E4H	R/W	00H	UART Control Register 3
UARTST	E5H	R/W	80H	UART Status Register

Table 11-13. UART Register Map

11.9.9 UART Register Description

UART module consists of UART baud rate generation register (UARTBD), UART data register (UARTDR),UART control register 1 (UARTCR1),UART control register 2 (UARTCR2) ,UART control register 3 (UARTCR3), and UART status register (UARTST).

11.9.10 Register Description for UART

UARTBD (UART BaudRate Generation Register) : E6H

7	6	5	4	3	2	1	0
UARTBD7	UARTBD6	UARTBD5	UARTBD4	UARTBD3	UARTBD2	UARTBD1	UARTBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :FFH

UARTBD [7:0] The value in this register is used to generate internal baud rate. To prevent malfunction, do not write ‘0’.

UARTDR (UART Data Register) : E7H

7	6	5	4	3	2	1	0
UARTDR7	UARTDR6	UARTDR5	UARTDR4	UARTDR3	UARTDR2	UARTDR1	UARTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

UARTDR [7:0] The UART Transmit Buffer and Receive Buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the UARTDR register. Reading the UARTDR register returns the contents of the Receive Buffer.

Write this register only when the UDRE flag is set.

UARTCR1 (UART Control Register 1) : E2H

7	6	5	4	3	2	1	0
-	-	UPM1	UPM0	USIZE2	USIZE1	USIZE0	-
-	-	R/W	R/W	R/W	R/W	R/W	-

Initial value : 00H

UPM[1:0] Selects Parity Generation and Check methods

UPM1	UPM0	Parity
0	0	No Parity
0	1	Reserved
1	0	Even Parity
1	1	Odd Parity

USIZE[2:0] Selects the Length of Data Bits in Frame

USIZE2	USIZE1	USIZE0	Data Length
0	0	0	5 bit
0	0	1	6 bit
0	1	0	7 bit
0	1	1	8 bit
1	1	1	9 bit
Other values			Reserved

UARTCR2 (UART Control Register 2) : E3H

7	6	5	4	3	2	1	0
UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	UARTEN	U2X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

UDRIE Interrupt enable bit for UART Data Register Empty

0 Interrupt from UDRE is inhibited (use polling)

1 When UDRE is set, request an interrupt

TXCIE Interrupt enable bit for Transmit Complete

0 Interrupt from TXC is inhibited (use polling)

1 When TXC is set, request an interrupt

RXCIE Interrupt enable bit for Receive Complete

0 Interrupt from RXC is inhibited (use polling)

1 When RXC is set, request an interrupt

WAKEIE Interrupt enable bit for Wake in STOP mode. When device is in stop mode, if RXD goes to LOW level, an interrupt can be requested to wake-up system. At that time the UDRIE bit and UARTST register value should be set to ‘0b’ and “00H”, respectively.

0 Interrupt from Wake is inhibited

1 When WAKE is set, request an interrupt

TXE Enables the transmitter unit

0 Transmitter is disabled

1 Transmitter is enabled

RXE Enables the receiver unit

0 Receiver is disabled

1 Receiver is enabled

UARTEN Activate UART module by supplying clock. When one of TXE and RXE values is “1”, the UARTEN bit always set to “1”.

0 UART is disabled (clock is halted)

1 UART is enabled

U2X This bit selects receiver sampling rate.

0 Normal operation

1 Double Speed operation

UARTCR3 (UART Control Register 3) : E4H

7	6	5	4	3	2	1	0
-	LOOPS	-	-	-	USBS	TX8	RX8
-	R/W	-	-	-	R/W	R/W	R

Initial value : 00H

LOOPS Controls the Loop Back Mode of UART, for test mode

0 Normal operation

1 Loop Back mode

USBS Selects the length of stop bit.

0 1 Stop Bit

1 2 Stop Bit

TX8 The ninth bit of data frame in UART. Write this bit first before loading the UARTDR register

0 MSB (9^{th} bit) to be transmitted is '0'

1 MSB (9^{th} bit) to be transmitted is '1'

RX8 The ninth bit of data frame in UART. Read this bit first before reading the receive buffer

0 MSB (9^{th} bit) received is '0'

1 MSB (9^{th} bit) received is '1'

UARTST (UART Status Register) : E5H

7	6	5	4	3	2	1	0
UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE
R/W	R/W	R	R/W	R/W	R	R/W	R/W

Initial value :80H

UDRE The UDRE flag indicates if the transmit buffer (UARTDR) is ready to receive new data. If UDRE is '1', the buffer is empty and ready to be written. This flag can generate a UDRE interrupt.

0 Transmit buffer is not empty.

1 Transmit buffer is empty.

TXC This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer. This flag is automatically cleared when the interrupt service routine of a TXC interrupt is executed. This flag can generate a TXC interrupt. This bit is automatically cleared.

0 Transmission is ongoing.

1 Transmit buffer is empty and the data in transmit shift register are shifted out completely.

RXC This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read. The RXC flag can be used to generate a RXC interrupt.

0 There is no data unread in the receive buffer

1 There are more than 1 data in the receive buffer

WAKE This flag is set when the RXD pin is detected low while the CPU is in stop mode. This flag can be used to generate a WAKE interrupt. This bit should be cleared by program software.

0 No WAKE interrupt is generated.

1 WAKE interrupt is generated

SOFTRST This is an internal reset and only has effect on UART. Writing '1' to this bit initializes the internal logic of UART and this bit is automatically cleared.

0 No operation

1 Reset UART

DOR This bit is set if a Data Overrun occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.

0 No Data Overrun

1 Data Overrun detected

FE This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read.

0 No Frame Error

1 Frame Error detected

PE This bit is set if the next character in the receive buffer has a Parity Error to be received while Parity Checking is enabled. This bit is valid until the receive buffer is read.

0 No Parity Error

1 Parity Error detected

11.9.11 Baud Rate setting (example)

Baud Rate	fx=1.00MHz		fx=1.8432MHz		fx=2.00MHz	
	UARTBD	ERROR	UARTBD	ERROR	UARTBD	ERROR
2400	25	0.2%	47	0.0%	51	0.2%
4800	12	0.2%	23	0.0%	25	0.2%
9600	6	-7.0%	11	0.0%	12	0.2%
14.4k	3	8.5%	7	0.0%	8	-3.5%
19.2k	2	8.5%	5	0.0%	6	-7.0%
28.8k	1	8.5%	3	0.0%	3	8.5%
38.4k	1	-18.6%	2	0.0%	2	8.5%
57.6k	-	-	1	-25.0%	1	8.5%
76.8k	-	-	1	0.0%	1	-18.6%
115.2k	-	-	-	-	-	-
230.4k	-	-	-	-	-	-

(continued)

Baud Rate	fx=3.6864MHz		fx=4.00MHz		fx=7.3728MHz	
	UARTBD	ERROR	UARTBD	ERROR	UARTBD	ERROR
2400	95	0.0%	103	0.2%	191	0.0%
4800	47	0.0%	51	0.2%	95	0.0%
9600	23	0.0%	25	0.2%	47	0.0%
14.4k	15	0.0%	16	2.1%	31	0.0%
19.2k	11	0.0%	12	0.2%	23	0.0%
28.8k	7	0.0%	8	-3.5%	15	0.0%
38.4k	5	0.0%	6	-7.0%	11	0.0%
57.6k	3	0.0%	3	8.5%	7	0.0%
76.8k	2	0.0%	2	8.5%	5	0.0%
115.2k	1	0.0%	1	8.5%	3	0.0%
230.4k	-	-	-	-	1	0.0%
250k	-	-	-	-	1	-7.8%
0.5M	-	-	-	-	-	-

(continued)

Baud Rate	fx=8.00MHz		fx=11.0592MHz	
	UARTBD	ERROR	UARTBD	ERROR
2400	207	0.2%	-	-
4800	103	0.2%	143	0.0%
9600	51	0.2%	71	0.0%
14.4k	34	-0.8%	47	0.0%
19.2k	25	0.2%	35	0.0%
28.8k	16	2.1%	23	0.0%
38.4k	12	0.2%	17	0.0%
57.6k	8	-3.5%	11	0.0%
76.8k	6	-7.0%	8	0.0%
115.2k	3	8.5%	5	0.0%
230.4k	1	8.5%	2	0.0%
250k	1	0.0%	2	-7.8%
0.5M	-	-	-	-

Table 11-14. Examples of UARTBD Settings for Commonly Used Oscillator Frequencies

11.10 LCD Driver

11.10.1 Overview

The LCD driver is controlled by the LCD Control Register (LCDCRH/L)and LCD driver contrast control register (LCDCCR). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCDCRH, LCDCRL and LCDCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes if a sub-frequency clock is used as LCD clock source.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don't rewrite LCDCRH frequently.

11.10.2 LCD Display RAM Organization

Display data are stored to the display data area in the internal data memory.

The display data which stored to the display internal data area (address E2H-FFH) are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with a program.

Figure 11-36 shows the correspondence between the display external data area and the COM/SEG pins. The LCD is turned on when the display data is “1” and turned off when “0”.

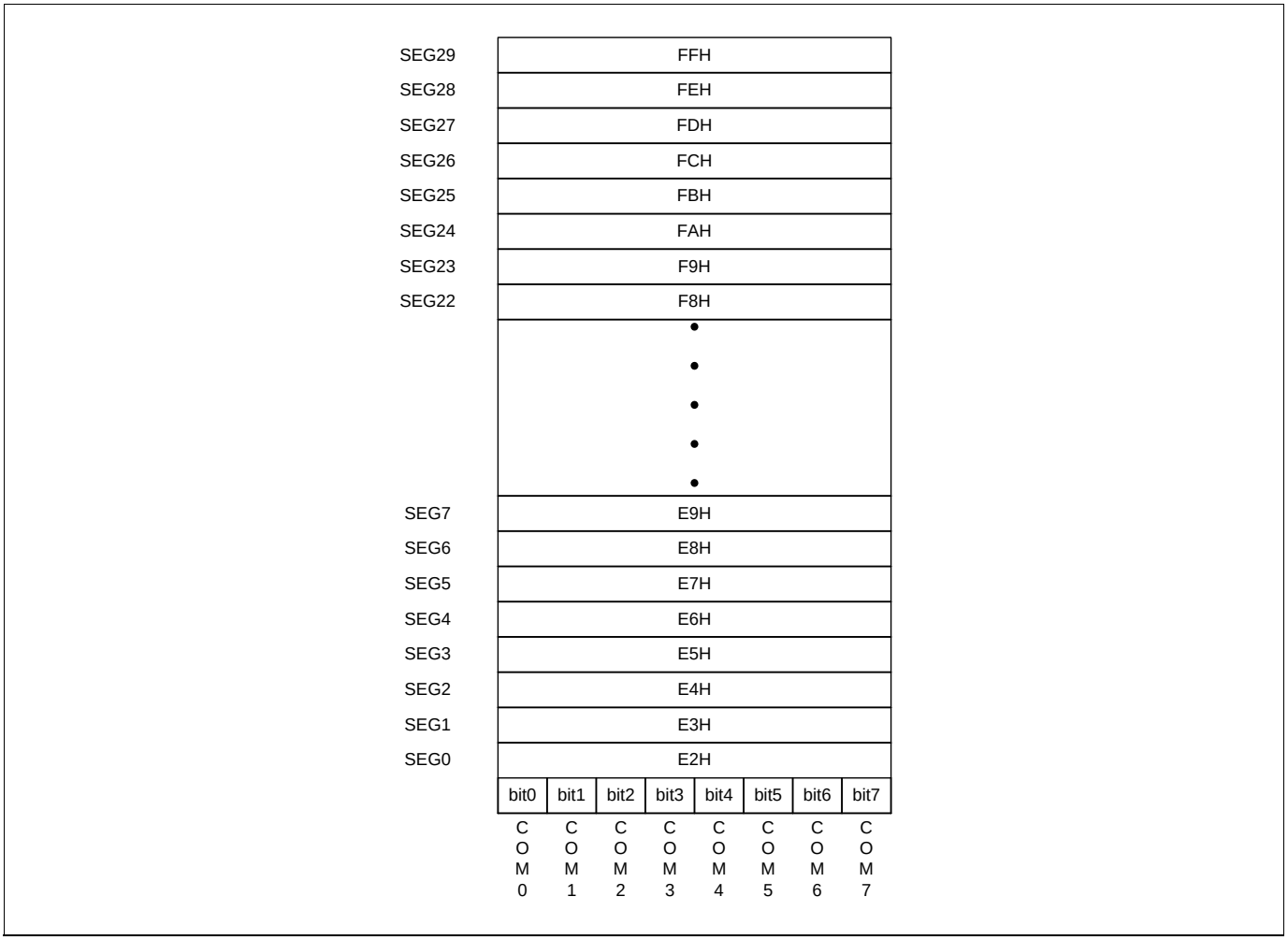


Figure 11.42 LCD Circuit Block Diagram

11.10.3 LCD Signal Waveform

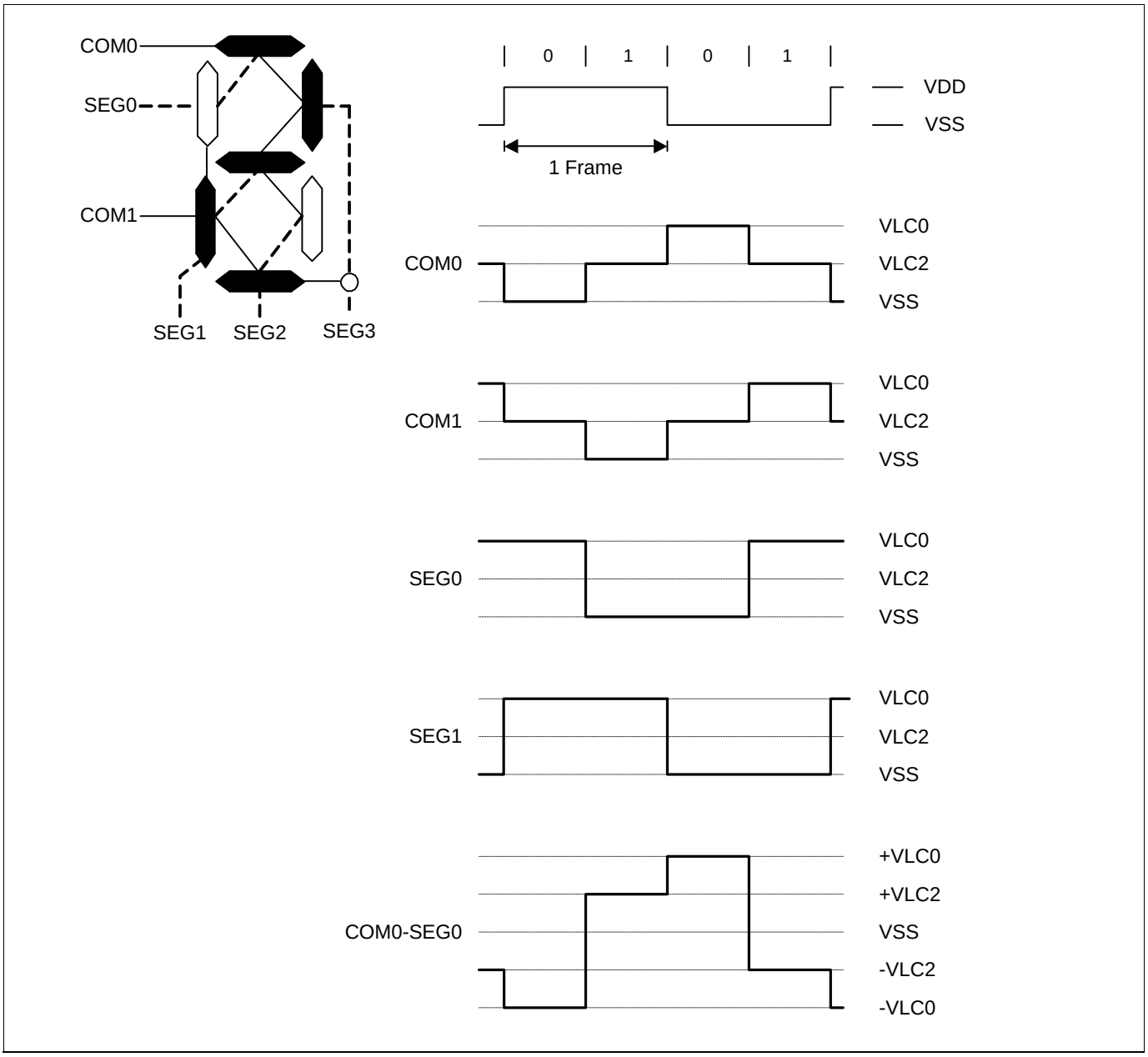


Figure 11.43 LCD Signal Waveforms (1/2Duty, 1/2Bias)

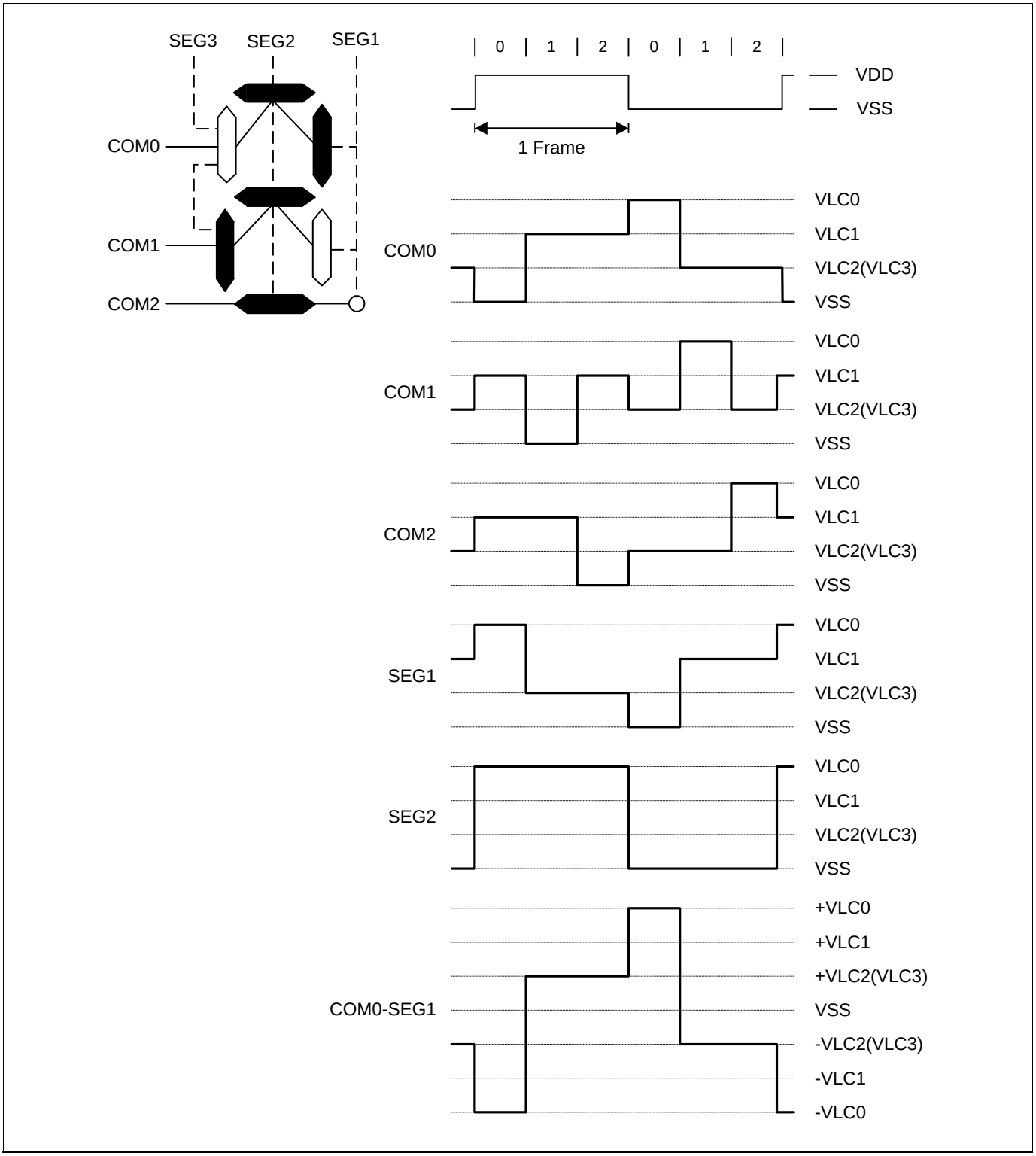


Figure 11.44 LCD Signal Waveforms (1/3Duty, 1/3Bias)

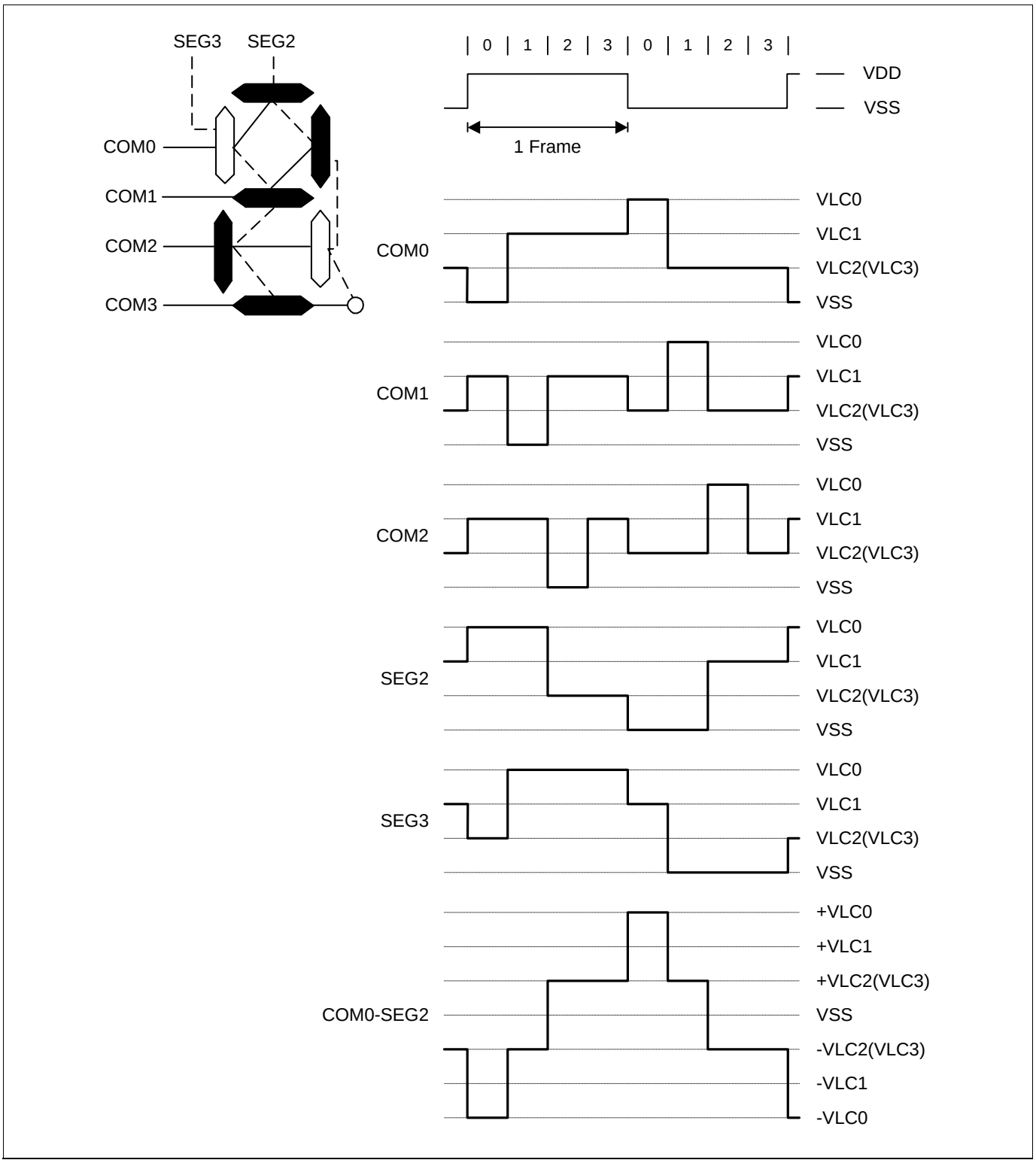


Figure 11.45 LCD Signal Waveforms (1/4Duty, 1/3Bias)

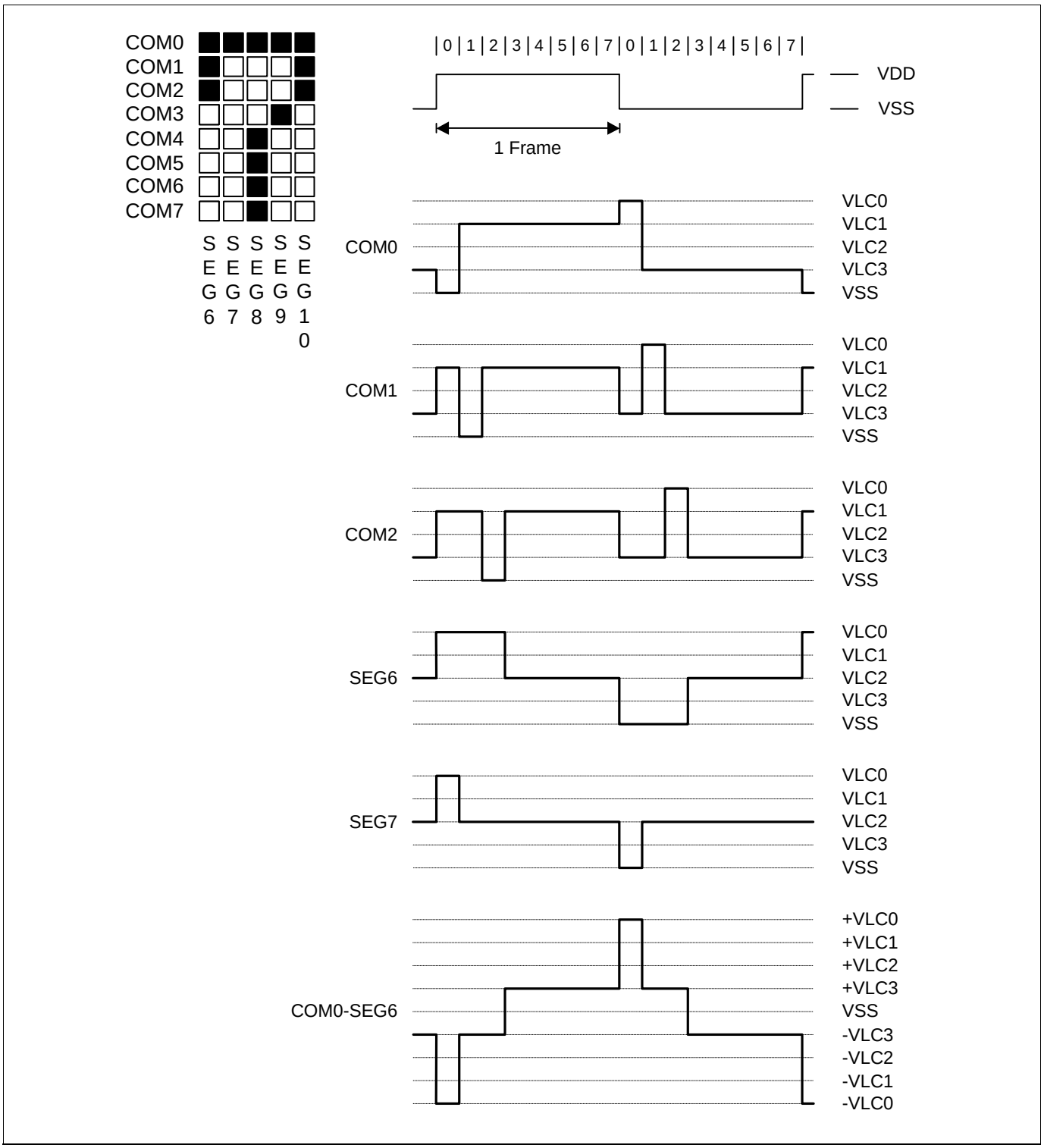
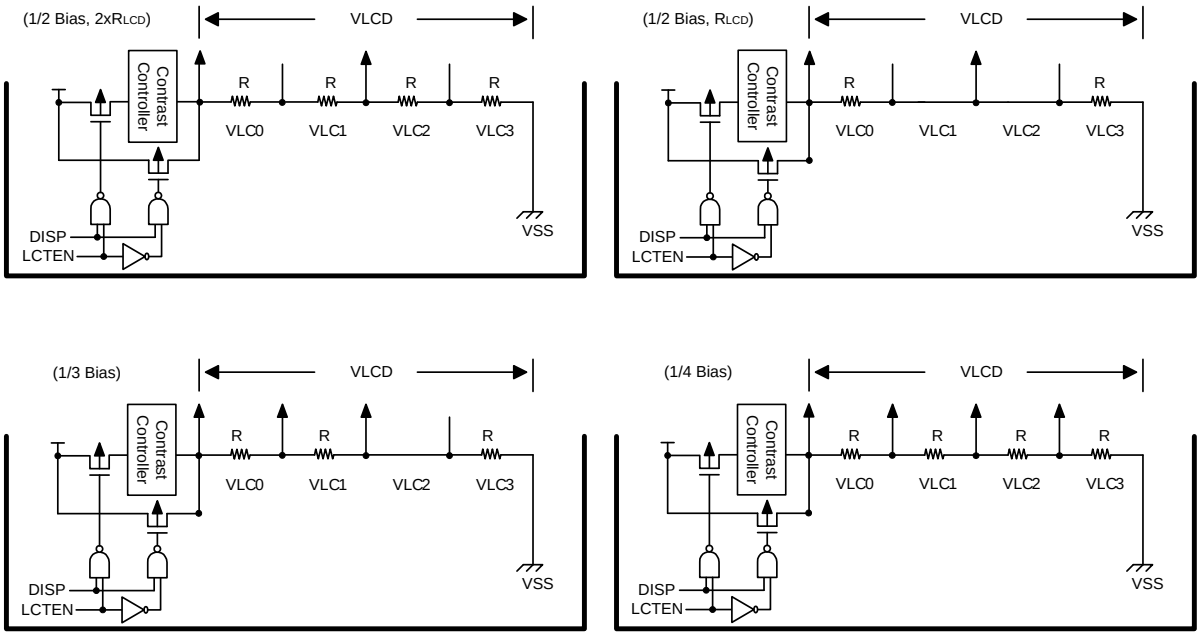


Figure 11.46 LCD Signal Waveforms (1/8Duty, 1/4Bias)

11.10.4 LCD Voltage Dividing Resistor Connection



NOTE)

1. When 1/2 bias are selected, the VLC0, VLC1 and VLC2, VLC3 are internally connected.
2. When 1/3 bias are selected, the VLC2 and VLC3 are internally connected.

Figure 11.47 Internal Resistor Bias Connection

11.10.5 Block Diagram

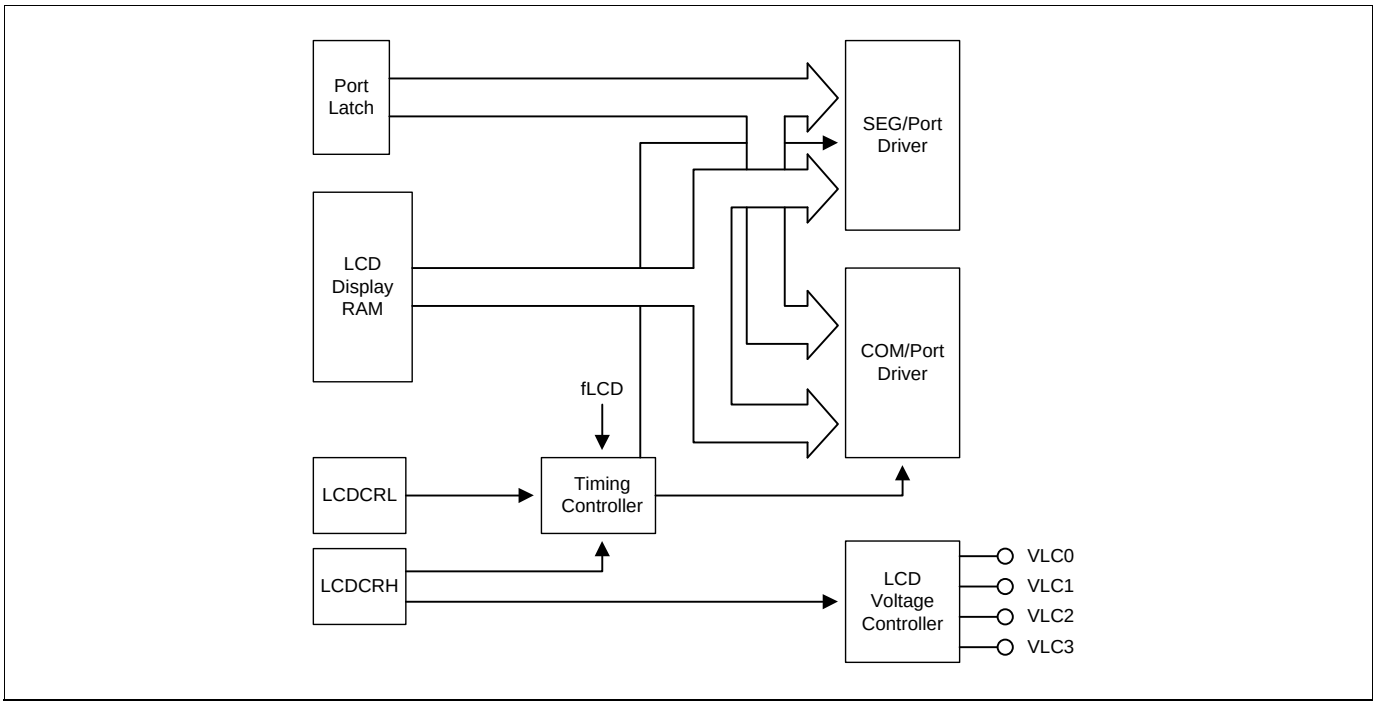


Figure 11.48 LCD Circuit Block Diagram

NOTE)

1. The clock and duty for LCD driver is automatically initialized by hardware, whenever LCDCRH register data value is rewritten. So, don't rewrite LCDCRH frequently

11.10.6 Register Map

Name	Address	Dir	Default	Description
LCDCRH	ECH	R/W	00H	LCD Driver Control High Register
LCDCRL	EBH	R/W	00H	LCD Driver Control Low Register
LCDCCR	F5H	R/W	00H	LCD Contrast Control Register

Table 11-15. LCD Register Map

11.10.7 LCD Driver Register Description

LCD driver register has three control registers, LCD driver control high register (LCDCRH), LCD driver control low register (LCDCRL) and LCD contrast control register (LCDCCR)..

11.10.8 Register Description for LCD Driver

LCDCRH (LCD Driver Control High Register) : ECH

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DISP
–	–	–	–	–	–	–	R/W

Initial value :00H

DISP LCD Display Control

0 Display off

1 Normal Display on

LCDCRL (LCD Driver Control Low Register) : EBH

7	6	5	4	3	2	1	0
IRSEL	–	DBS3	DBS2	DBS1	DBS0	LCLK1	LCLK0
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

IRSEL Internal LCD Bias Dividing Resistor Select

0 R_{LCD} = 60kΩ (RLCD1)

0 R_{LCD} = 120kΩ (RLCD2)

DBS[3:0] LCD Duty and Bias Select

DBS3	DBS2	DBS1	DBS0	Description
0	0	0	0	1/8Duty, 1/4Bias, R_{LCD}
0	0	0	1	1/6Duty, 1/4Bias, R_{LCD}
0	0	1	0	1/5Duty, 1/3Bias, R_{LCD}
0	0	1	1	1/4Duty, 1/3Bias, R_{LCD}
0	1	0	0	1/3Duty, 1/3Bias, R_{LCD}
0	1	0	1	1/3Duty, 1/2Bias, R_{LCD}
0	1	1	0	1/3Duty, 1/2Bias, 2x R_{LCD}
0	1	1	1	1/2Duty, 1/2Bias, R_{LCD}
1	0	0	0	1/2Duty, 12Bias, 2x R_{LCD}
Other values				Not available

LCLK[1:0] LCD Clock Select (When f_{WCK}(Watch timer clock)= 32.768 kHz)

LCLK1	LCLK0	Description
0	0	f_{LCD} = 128Hz
0	1	f_{LCD} = 256Hz
1	0	f_{LCD} = 512Hz
1	1	f_{LCD} = 1024Hz

NOTE)

1. The LCD clock is generated by watch timer clock (f_{WCK}). So the watch timer should be enabled when the LCD display is turned on.

LCD Clock Frequency (f_{LCD})	LCD Frame Frequency(f_{FRAME})						Unit
	1/2 Duty	1/3 Duty	1/4 Duty	1/5 Duty	1/6 Duty	1/8 Duty	
128	64	43	32	26	21	16	Hz
256	128	85	64	51	43	32	
512	256	171	128	102	85	64	
1024	512	341	256	205	171	128	

Table 11-16. LCD Frame Frequency

The LCD frame frequency is calculated by the following formula:

$$\text{LCD Frame Frequency } (f_{FRAME}) = f_{LCD} \times \text{Duty[Hz]}$$

Ex) In case of 1/4 duty and f_{LCD}=512Hz, $f_{FRAME} = f_{LCD} \times 1/4 = 512 \times 1/4 = 128$[Hz]

LCDCCR (LCD Driver Contrast Control Register) : F5H

7	6	5	4	3	2	1	0
LCTEN	–	–	–	VLCD3	VLCD2	VLCD1	VLCD0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

LCTEN Control LCD Driver Contrast

0 LCD Driver Contrast Disable

0 LCD Driver Contrast Enable

VLCD[3:0] VLC0 Voltage Control when the Contrast is enabled

VLCD3	VLCD2	VLCD1	VLCD0	Description
0	0	0	0	VLC0 = VDD x 16/31 step
0	0	0	1	VLC0 = VDD x 16/30 step
0	0	1	0	VLC0 = VDD x 16/29 step
0	0	1	1	VLC0 = VDD x 16/28 step
0	1	0	0	VLC0 = VDD x 16/27 step
0	1	0	1	VLC0 = VDD x 16/26 step
0	1	1	0	VLC0 = VDD x 16/25 step
0	1	1	1	VLC0 = VDD x 16/24 step
1	0	0	0	VLC0 = VDD x 16/23 step
1	0	0	1	VLC0 = VDD x 16/22 step
1	0	1	0	VLC0 = VDD x 16/21 step
1	0	1	1	VLC0 = VDD x 16/20 step
1	1	0	0	VLC0 = VDD x 16/19 step
1	1	0	1	VLC0 = VDD x 16/18 step
1	1	1	0	VLC0 = VDD x 16/17 step
1	1	1	1	VLC0 = VDD x 16/16 step

NOTE)

1. The contrast step is based on 1/4 bias and RLCD = 60kΩ.
2. 1/4 bias: VDD x 16/(31 – VLCD[3:0]) when RLCD = 60Kω
   VDD x 32/(47 – VLCD[3:0]) when RLCD = 120kΩ
3. 1/3 bias: VDD x 12/(27– VLCD[3:0]) when RLCD = 60kΩ
   VDD x 24/(39– VLCD[3:0]) when RLCD = 120kΩ
4. 1/2 bias: VDD x 8/(23 – VLCD[3:0]) when RLCD = 60kΩ
   VDD x 16/(31 – VLCD[3:0]) when RLCD = 120kΩ

12 Power Down Operation

12.1 Overview

The MC96F6508A has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, Sub-IDLE and STOP mode. In three modes, program is stopped.

12.2 Peripheral Operation in IDLE/STOP Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~3	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
BUZ	Operates Continuously	Stop
UART	Operates Continuously	Stop
SIO	Operates Continuously	Only operate with external clock
LCD Controller	Operates Continuously	Stop (Can be operated with sub clock)
Internal OSC (16MHz)	Oscillation	Stop when the system clock (fx) is f_{IRC}
WDTRC OSC (5kHz)	Can be operated with setting value	Can be operated with setting value
Main OSC (1~12MHz)	Oscillation	Stop when fx = f_{XIN}
Sub OSC (32.768kHz)	Oscillation	Stop when fx = f_{SUB}
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0,EC2), SIO (External clock), External Interrupt, UART by RX, WT (sub clock), WDT

Table 12-1. Peripheral Operation during Power Down Mode

12.3 IDLE Mode

The power control register is set to ‘01h’ to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

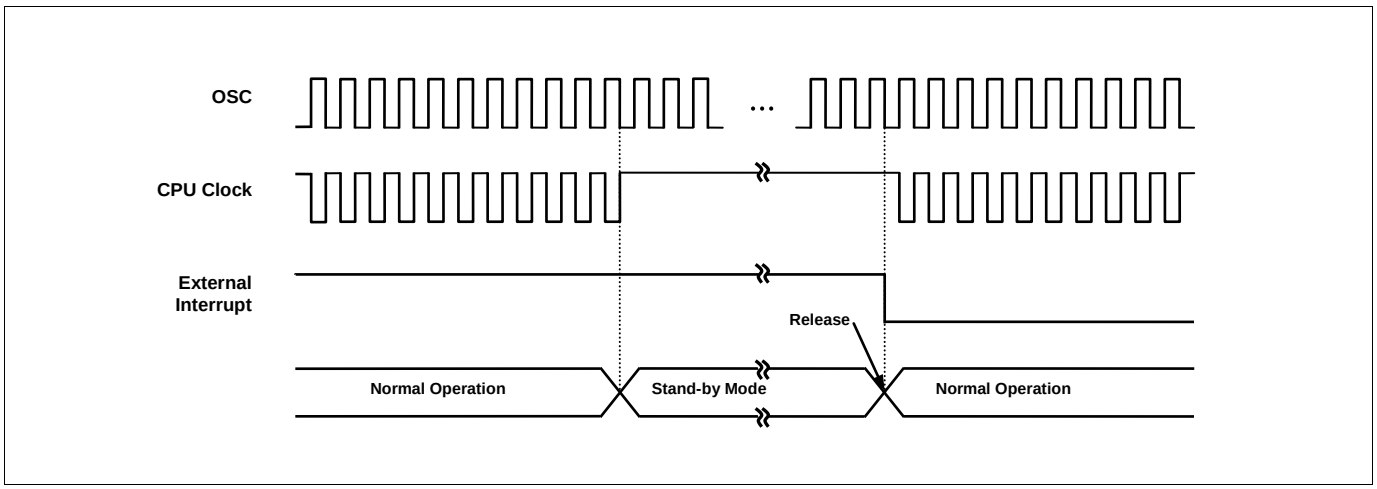


Figure 12.1 IDLE Mode Release Timing by External Interrupt

12.4 STOP Mode

The power control register is set to '03H' to enter the STOP Mode. In the stop mode, the selected oscillator, system clock and peripheral clock is stopped, but watch timer can be continued to operate with sub clock. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held. For example, If the internal RC oscillator (f_{IRC}) is selected for the system clock and the sub clock (f_{SUB}) is oscillated, the internal RC oscillator stops oscillation and the sub clock is continuously oscillated in stop mode. At that time, the watch timer and LCD controller can be operated with the sub clock.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers.

When exit from STOP mode, enough oscillation stabilization time is required to normal operation. Figure 12.2 shows the timing diagram. When released from STOP mode, the Basic interval timer is activated on wake-up. Therefore, before STOP instruction, user must be set its relevant prescale divide ratio to have long enough time. This guarantees that oscillator has started and stabilized.

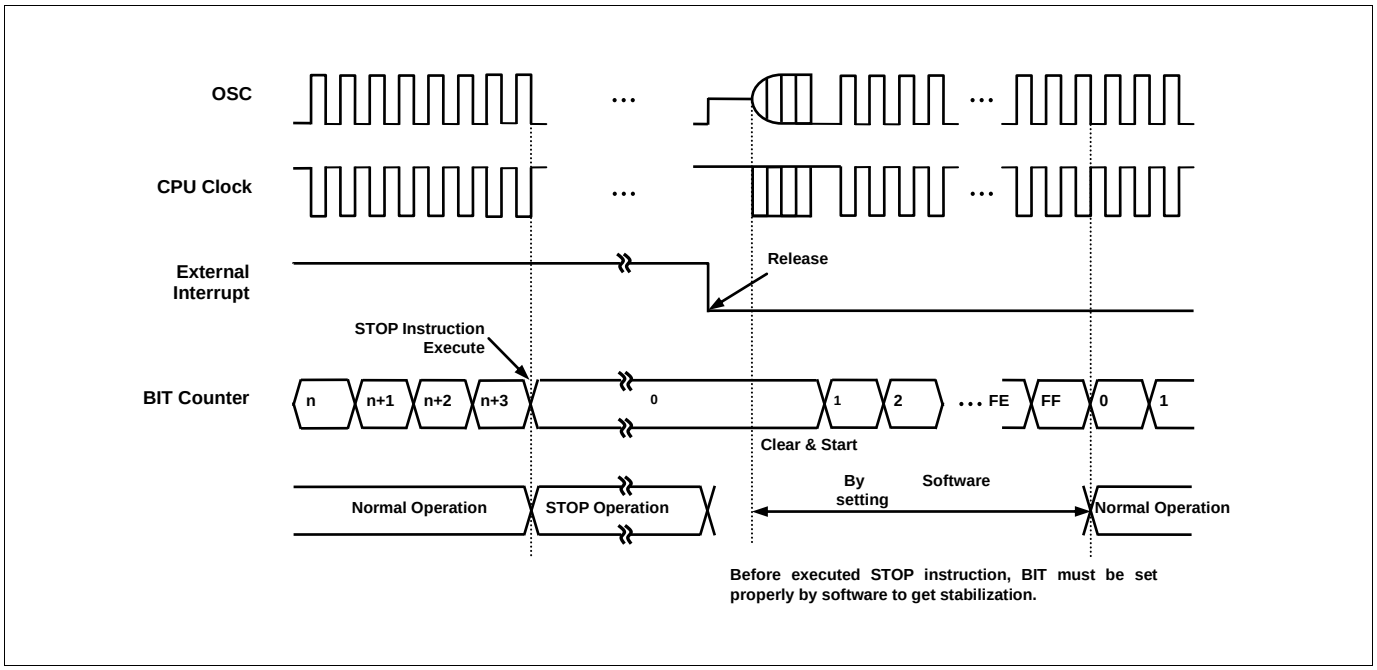


Figure 12.2 STOP Mode Release Timing by External Interrupt

12.5 Release Operation of STOP Mode

After STOP mode is released, the operation begins according to content of related interrupt register just before STOP mode start (Figure 12.3).If the global interrupt Enable Flag (IE.EA)is set to `1`, the STOP mode isreleased by the interrupt which each interrupt enable flag = `1` and the CPU jumps to the relevant interrupt service routine. Even if the IE.EA bit is cleared to '0', the STOP mode is released by the interrupt of which the interrupt enable flag is set to '1'.

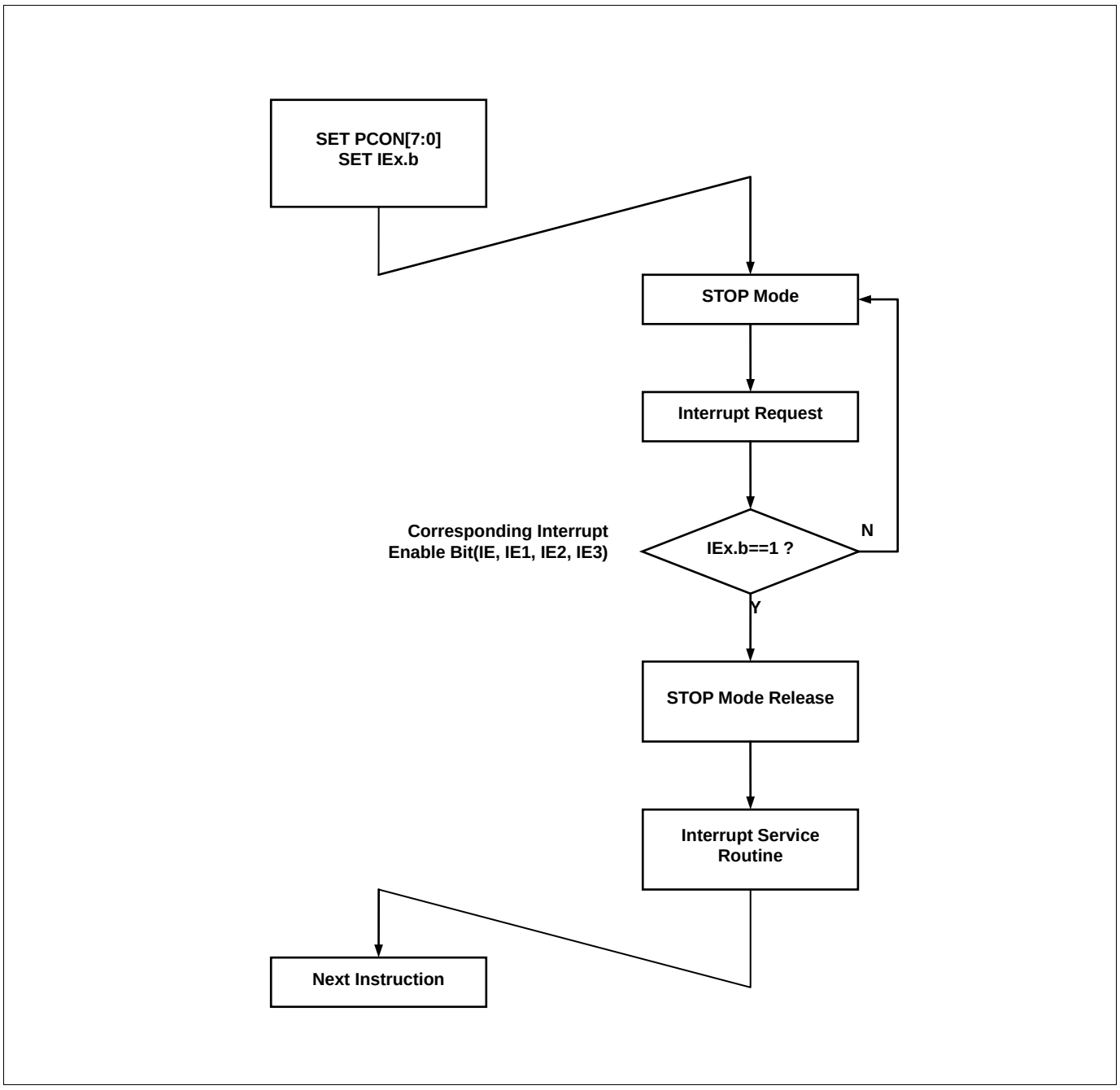


Figure 12.3 STOP Mode Release Flow

12.6 Register Map

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register

Table 12-2. Power Down Operation Register Map

12.7 Power Down Operation Register Description

The power down operation register consists of the power control register (PCON).

12.8 Register Description for Power Down Operation

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

PCON[7:0] Power Control

01H IDLE mode enable

03H STOP mode enable

NOTE)

1. To enter IDLE mode, PCON must be set to '01H'.
2. To enter STOP mode, PCON must be set to '03H'.
3. The PCON register is automatically cleared by a release signal in STOP/IDLE mode.
4. Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples.

Ex1)
```
MOV     PCON, #01H; IDLE mode
NOP
NOP
NOP
 •
 •
 •
```

Ex2)
```
MOV     PCON, #03H; STOP mode
NOP
NOP
NOP
 •
 •
 •
```

13 RESET

13.1 Overview

The following is the hardware setting value.

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

Table 13-1. Reset State

13.2 Reset Source

The MC96F6508A has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

13.3 RESET Block Diagram

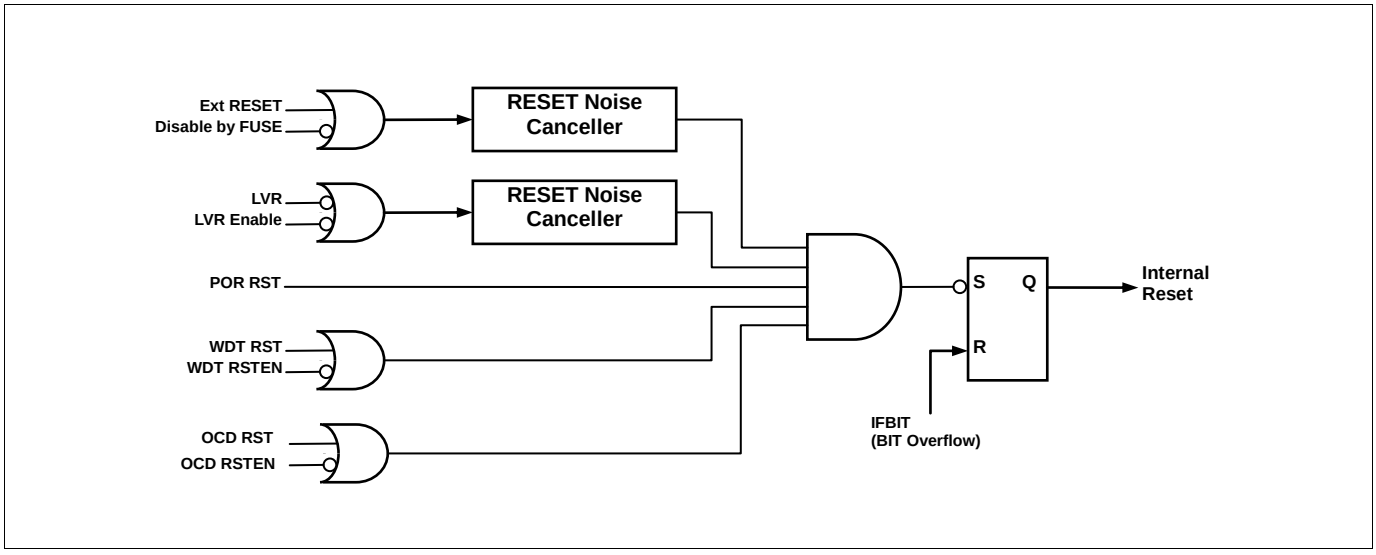


Figure 13.1 RESET Block Diagram

13.4 RESET Noise Canceller

The Figure 13.2 is the noise canceller diagram for noise cancellation of RESET. It has the noise cancellation value of about 2us(@V_{DD}=5V) to the low input of system reset.

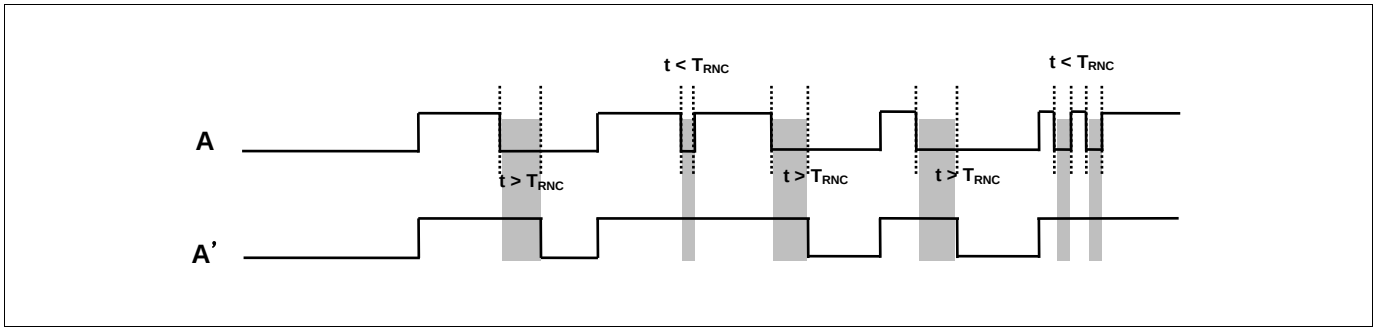


Figure 13.2 Reset noise canceller timer diagram

13.5 Power On RESET

When rising device power, the POR (Power On Reset) has a function to reset the device. If POR is used, it executes the device RESET function instead of the RESET IC or the RESET circuits.

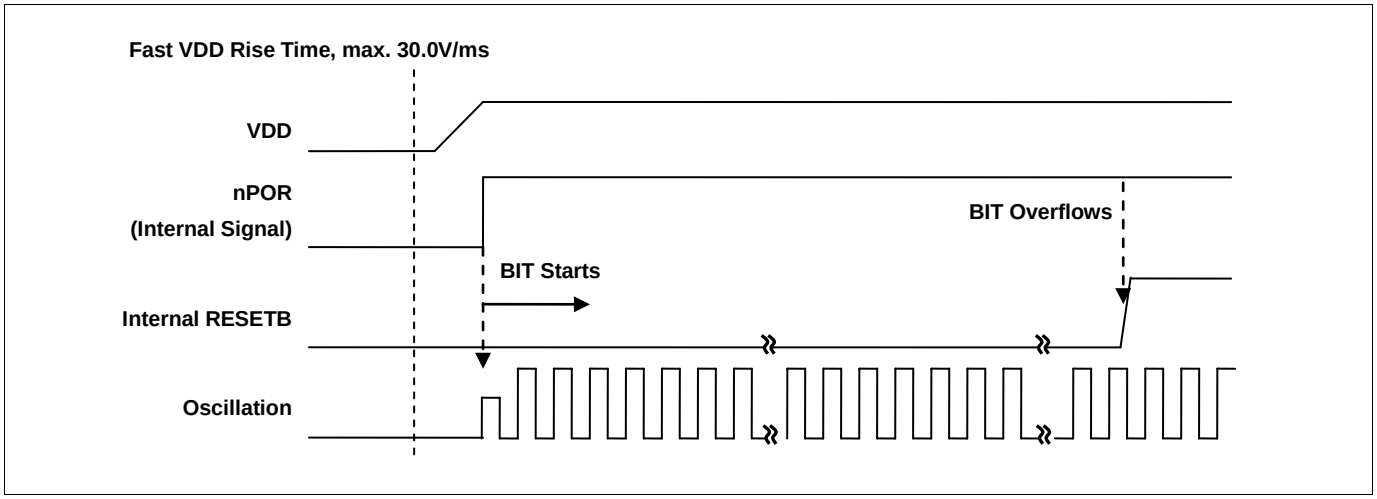


Figure 13.3 Fast VDD Rising Time

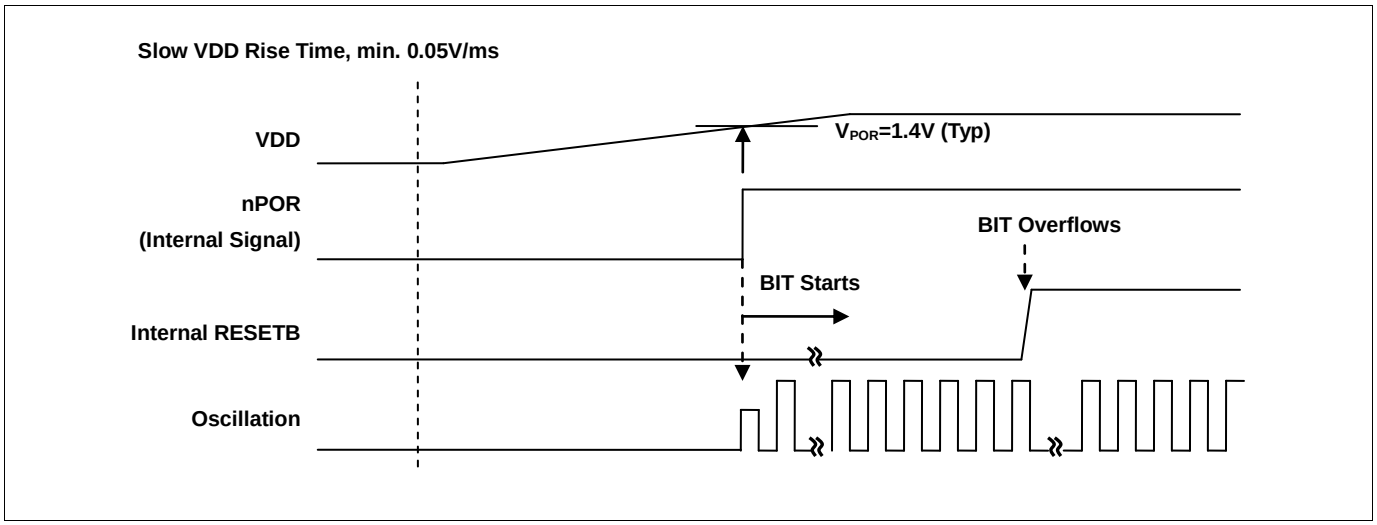


Figure 13.4 Internal RESET Release Timing On Power-Up

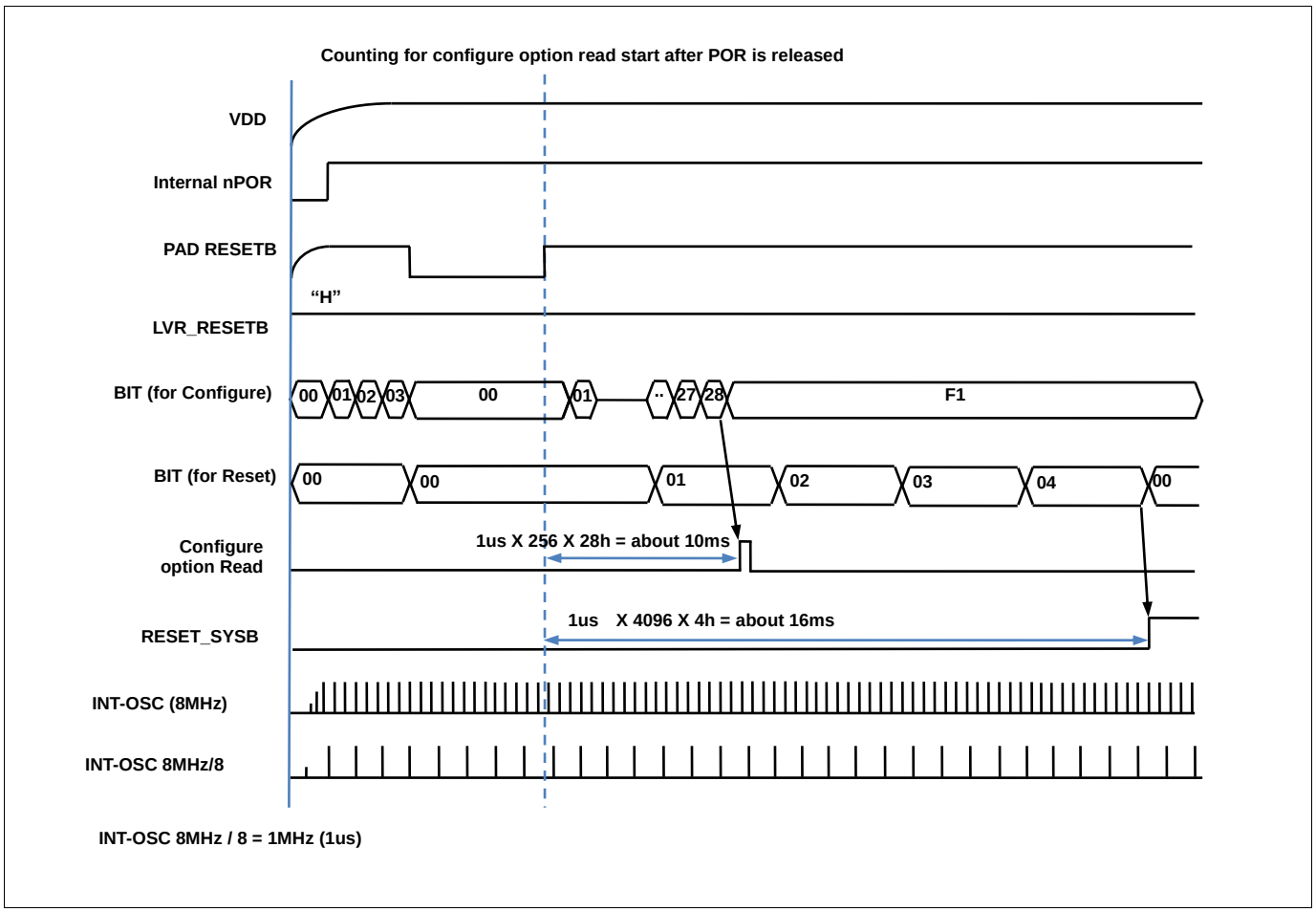


Figure 13.5 Configuration Timing when Power-on

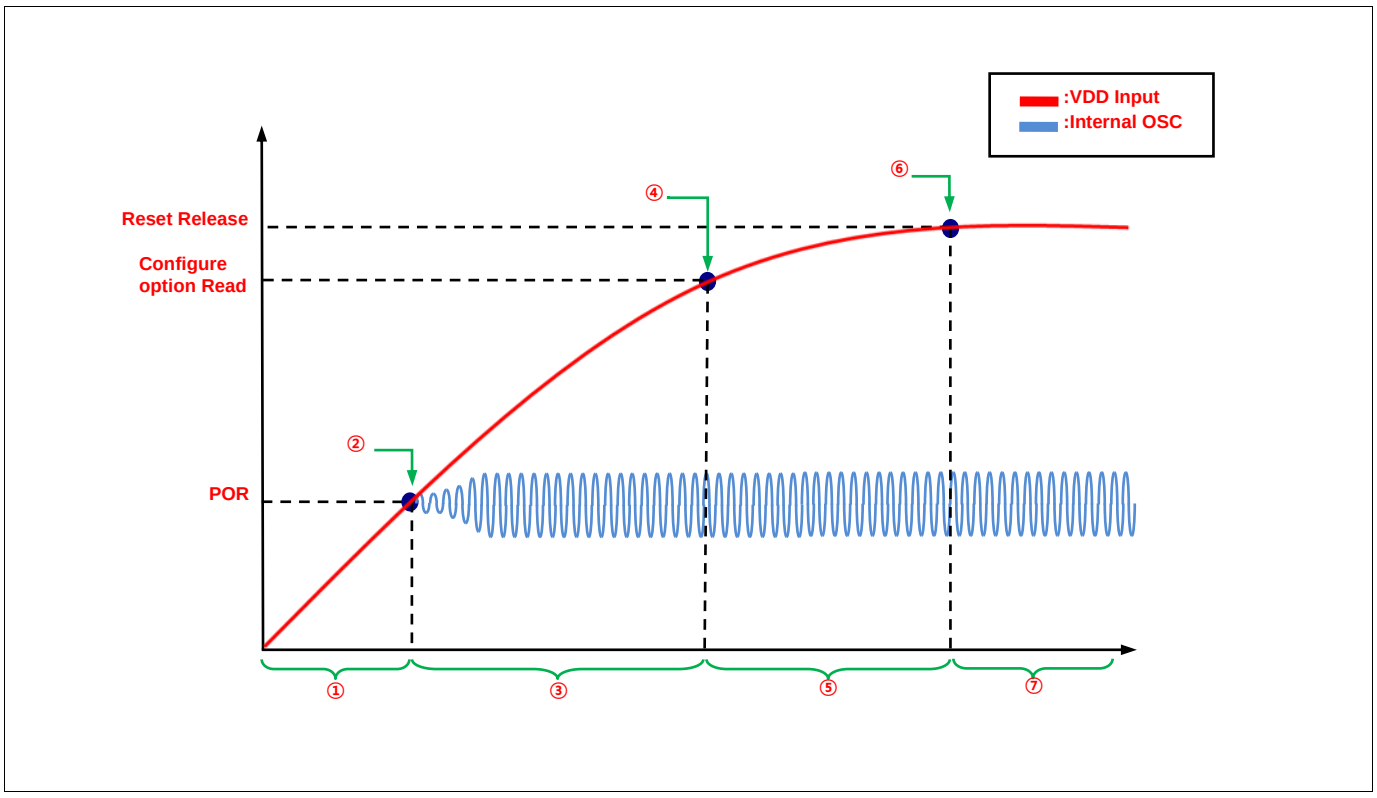


Figure 13.6 Boot Process WaveForm

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection	-about 1.4V
③	- (INT-OSC 16MHz/16)x256x28h Delay section (=10ms) -VDD input voltage must rise over than flash operating voltage for Configure option read	-Slew Rate >= 0.05V/ms
④	- Configure option read point	- about 1.5V ~ 1.6V -Configure Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR or Ext_reset release
⑥	- Reset Release section (BIT overflow) i) after 16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

Table 13-2. Boot Process Description

13.6 External RESETB Input

The External RESETB is the input to a Schmitt trigger. If RESETB pin is held with low for at least 10us over within the operating voltage range and stable oscillation, it is applied and the internal state is initialized. After reset state becomes '1', it needs the stabilization time with 16ms and after the stable state, the internal RESET becomes '1'. The Reset process step needs 5 oscillator clocks. And the program execution starts at the vector address stored at address 0000H.

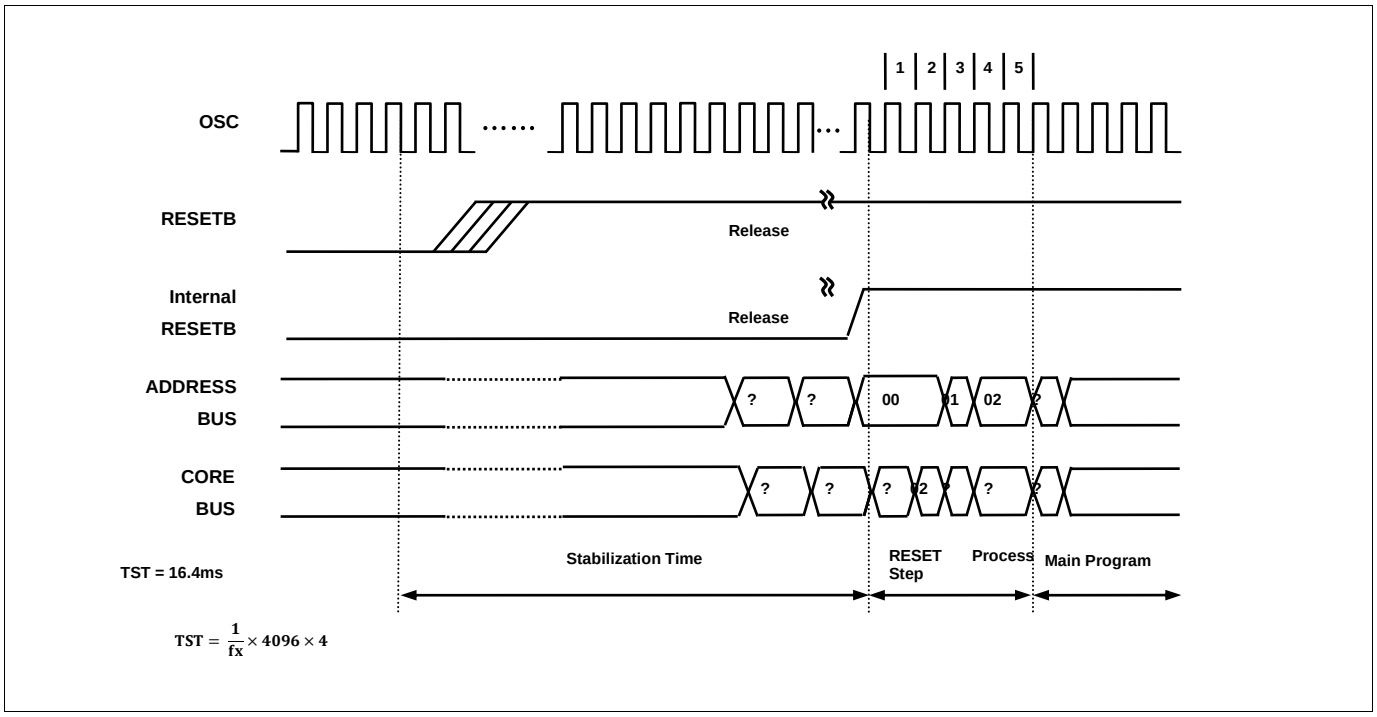


Figure 13.7 Timing Diagram after RESET

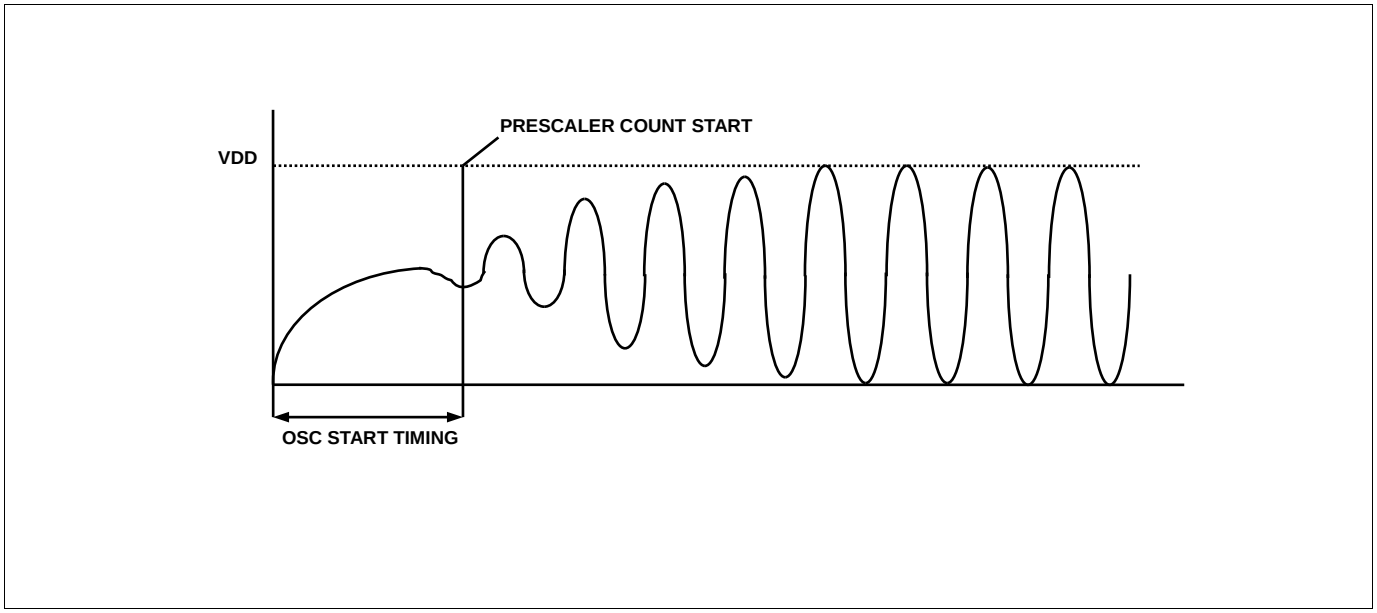


Figure 13.8 Oscillator generating waveform example

NOTE)

1. As shown Figure 13.8, the stable generating time is not included in the start-up time.
2. The RESETB pin has a pull-up resistor by H/W.

13.7 Brown Out Detector Processor

The MC96F6508A has an On-chip brown-out detection circuit (BOD) for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by LVRVS[3:0]. In the STOP mode, this will contribute significantly to the total current consumption. So to minimize the current consumption, the LVREN bit is set to off by software.

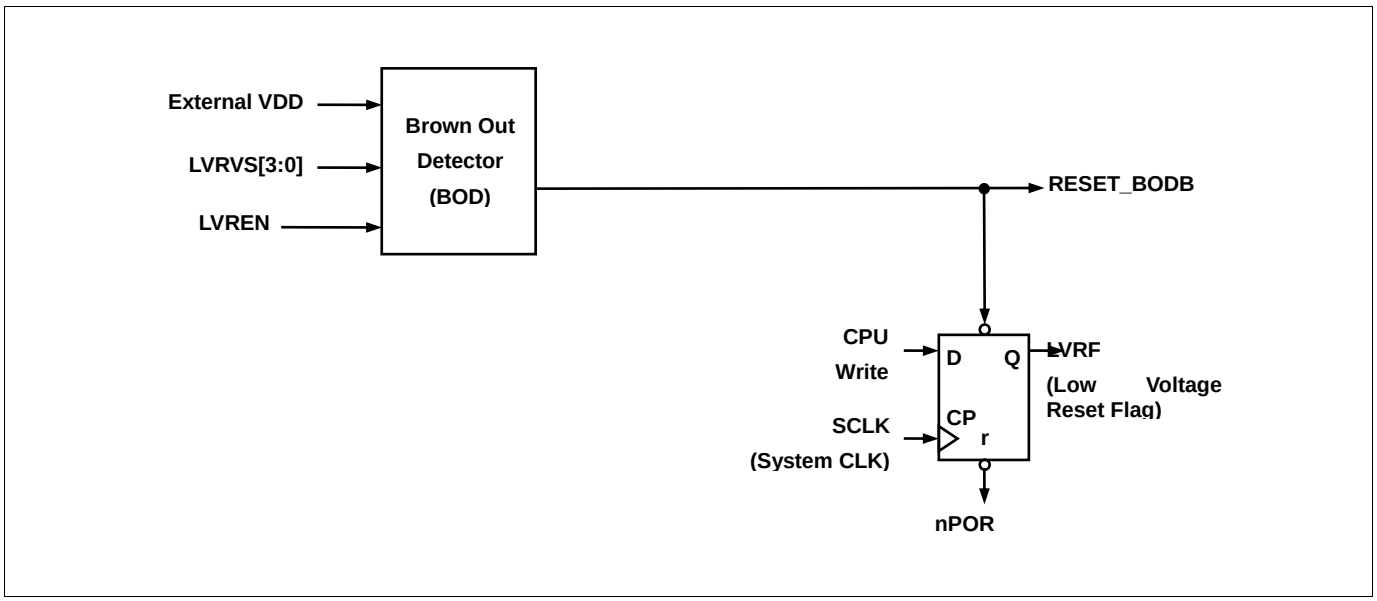


Figure 13.9 Block Diagram of BOD

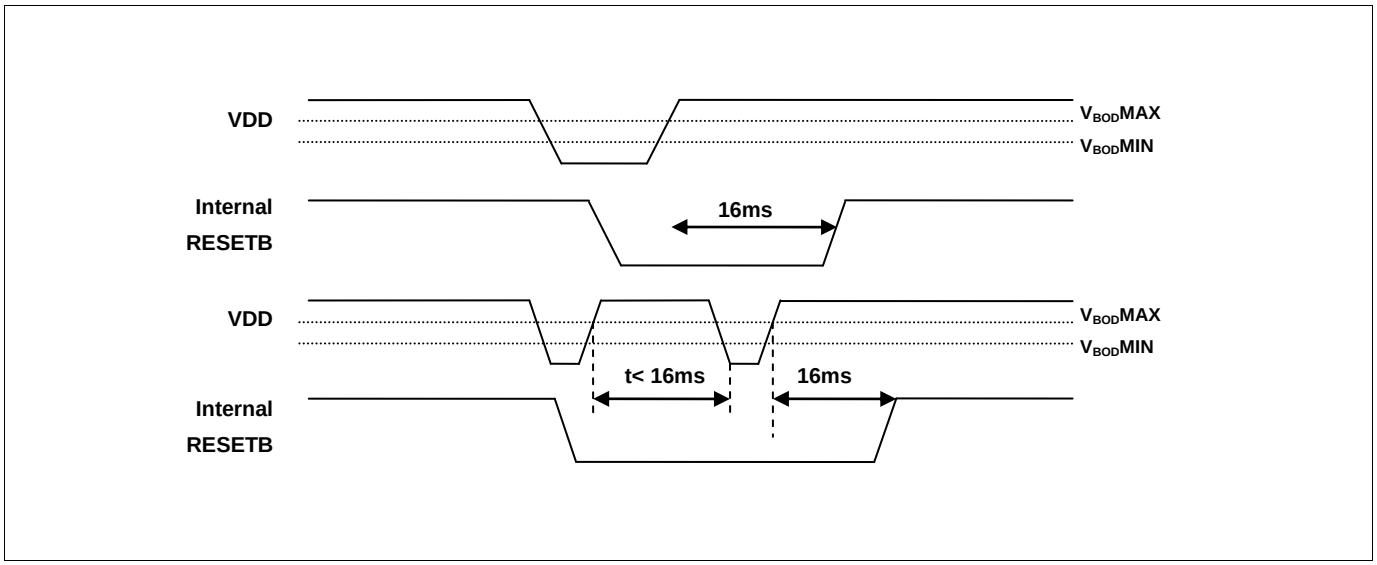


Figure 13.10 Internal Reset at the power fail situation

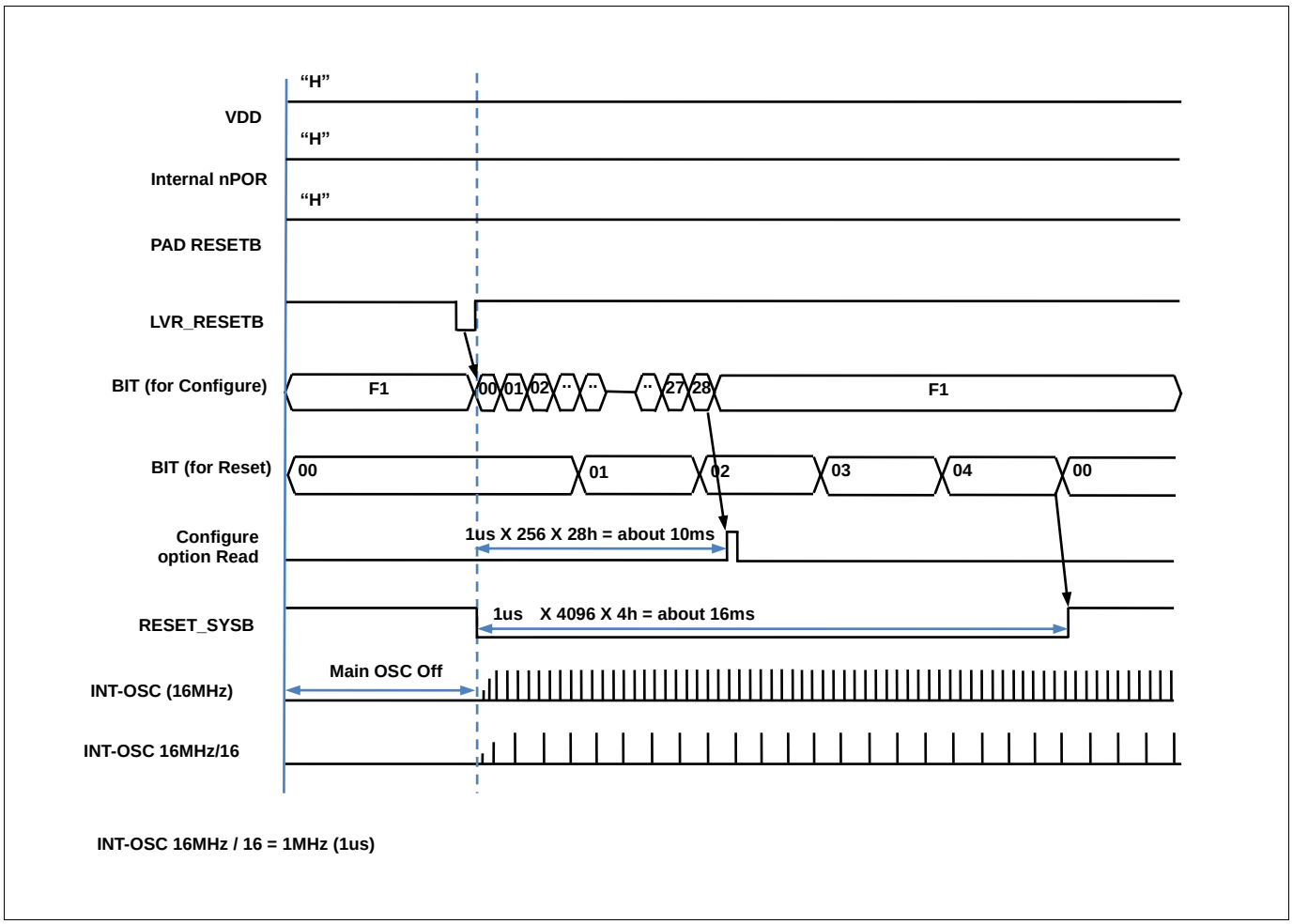


Figure 13.11 Configuration timing when BOD RESET

13.8 LVI Block Diagram

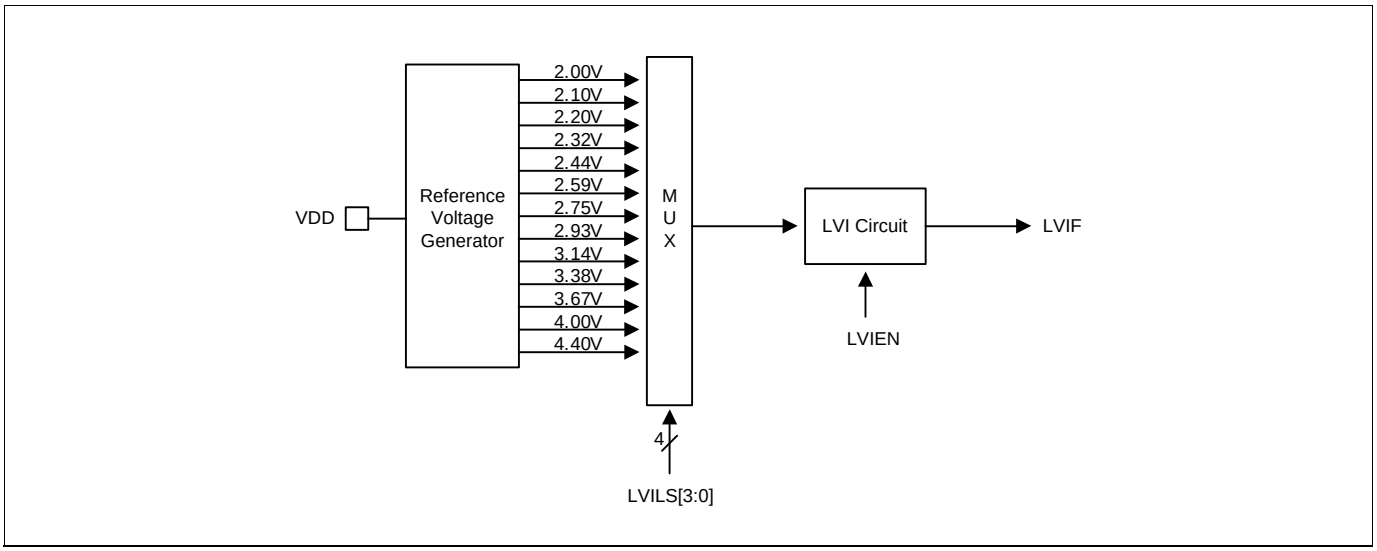


Figure 13.12 LVI Diagram

13.9 Register Map

Name	Address	Dir	Default	Description
RSTFR	86H	R/W	80H	Reset Flag Register
LVRCR	D8H	R/W	00H	Low Voltage Reset Control Register
LVICR	E1H	R/W	00H	Low Voltage Indicator Control Register

Table 13-3. Reset Operation Register Map

13.10 Reset Operation Register Description

The reset control register consists of the reset flag register (RSTFR), low voltage reset control register (LVRCR), and low voltage indicator control register (LVICR).

13.11 Register Description for Reset Operation

RSTFR (Reset Flag Register) : 86H

7	6	5	4	3	2	1	0
PORF	EXTRF	WDTRF	OCDRF	LVRF	–	–	–
R/W	R/W	R/W	R/W	R/W	–	–	–

Initial value :80H

PORF Power-On Reset flag bit. The bit is reset by writing '0' to this bit.

0 No detection

1 Detection

EXTRF External Reset (RESETB) flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

WDTRF Watch-Dog Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

LVRF Low Voltage Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

NOTE)

1. When the Power-On Reset occurs, the PORF bit is set to "1" and the WDTRF/OCDRF bits are all cleared to "0".
2. When the Power-On Reset occurs, the EXTRF bit is unknown, At that time, the EXTRF bit can be set to "1" when External Reset (RESETB) occurs.
3. When the Power-On Reset occurs, the LVRF bit is unknown, At that time, the LVRF bit can be set to "1" when Low Voltage Reset(LVR) occurs.
4. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous values.

LVRCR (Low Voltage Reset Control Register) :D8H

7	6	5	4	3	2	1	0
LVRST	–	–	LVRVS3	LVRVS2	LVRVS1	LVRVS0	LVREN
R/W	–	–	R/W	R/W	R/W	R/W	R/W

Initial value :00H

LVRST LVR Enable when Power-down Mode Release

0 Not effect at Power-down Mode release

1 LVR enable at Power-down Mode release

NOTE)

1. When this bit is '1', the LVREN bit is cleared to '0' by power-down (STOP/IDLE) mode release. (LVR enable)
2. When this bit is '0', the LVREN bit is not effect by power-down mode release.

LVRVS[3:0] LVR Voltage Select

LVRVS3	LVRVS2	LVRVS1	LVRVS0	Description
0	0	0	0	1.60V
0	0	0	1	2.00V
0	0	1	0	2.10V
0	0	1	1	2.20V
0	1	0	0	2.32V
0	1	0	1	2.44V
0	1	1	0	2.59V
0	1	1	1	2.75V
1	0	0	0	2.93V
1	0	0	1	3.14V
1	0	1	0	3.38V
1	0	1	1	3.67V
1	1	0	0	4.00V
1	1	0	1	4.40V
1	1	1	0	Not available
1	1	1	1	Not available

LVREN LVR Operation

0 LVR Enable

1 LVR Disable

NOTE)

1. The LVRST, LVRVS[3:0] bits are cleared by a power-on reset but are retained by other reset signals.
2. The LVRVS[3:0] bits should be set to '0000b' while LVREN bit is "1".

LVICR (Low Voltage Indicator Control Register) :E1H

7	6	5	4	3	2	1	0
–	–	LVIF	LVIEN	LVILS3	LVILS2	LVILS1	LVILS0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

LVIF Low Voltage Indicator Flag Bit

0 No detection

1 Detection

LVIEN LVI Enable/Disable

0 Disable

1 Enable

LVILS[3:0] LVI Level Select

LVILS3	LVILS2	LVILS1	LVILS0	Description
0	0	0	0	2.00V
0	0	0	1	2.10V
0	0	1	0	2.20V
0	0	1	1	2.32V
0	1	0	0	2.44V
0	1	0	1	2.59V
0	1	1	0	2.75V
0	1	1	1	2.93V
1	0	0	0	3.14V
1	0	0	1	3.38V
1	0	1	0	3.67V
1	0	1	1	4.00V
1	1	0	0	4.40V
Other values				Not available

14 On-chip Debug System

14.1 Overview

14.1.1 Description

On-chip debug system(OCD) of MC96F6508A can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD interface can be found in the following chapter.
Figure 14.1 shows a block diagram of the OCD interface and the On-chip Debug system.

14.1.2 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Flash and Data EEPROM Memories
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the two-wire Interface
  - On-chip Debugging Supported by Dr.Choice®
- Operating frequency
  - Supports the maximum frequency of the target MCU

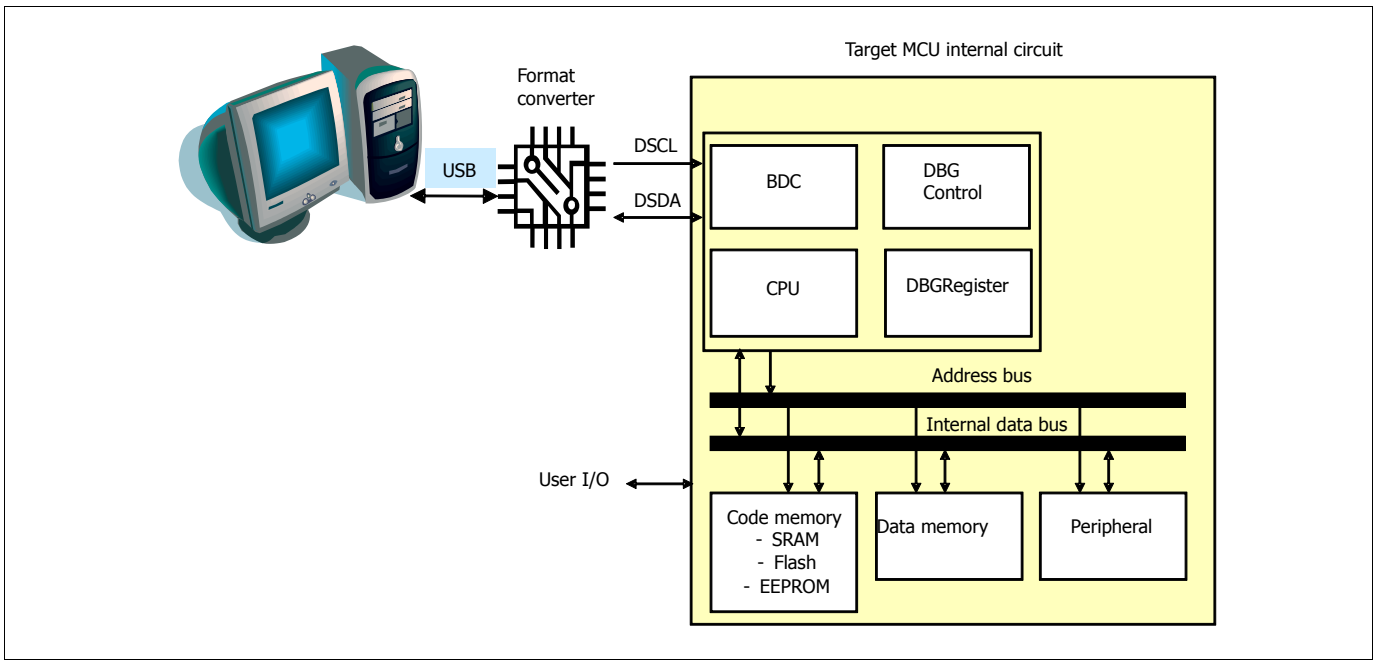


Figure 14.1 Block Diagram of On-Chip Debug System

14.2 Two-Pin External Interface

14.2.1 Basic Transmission Packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge(Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

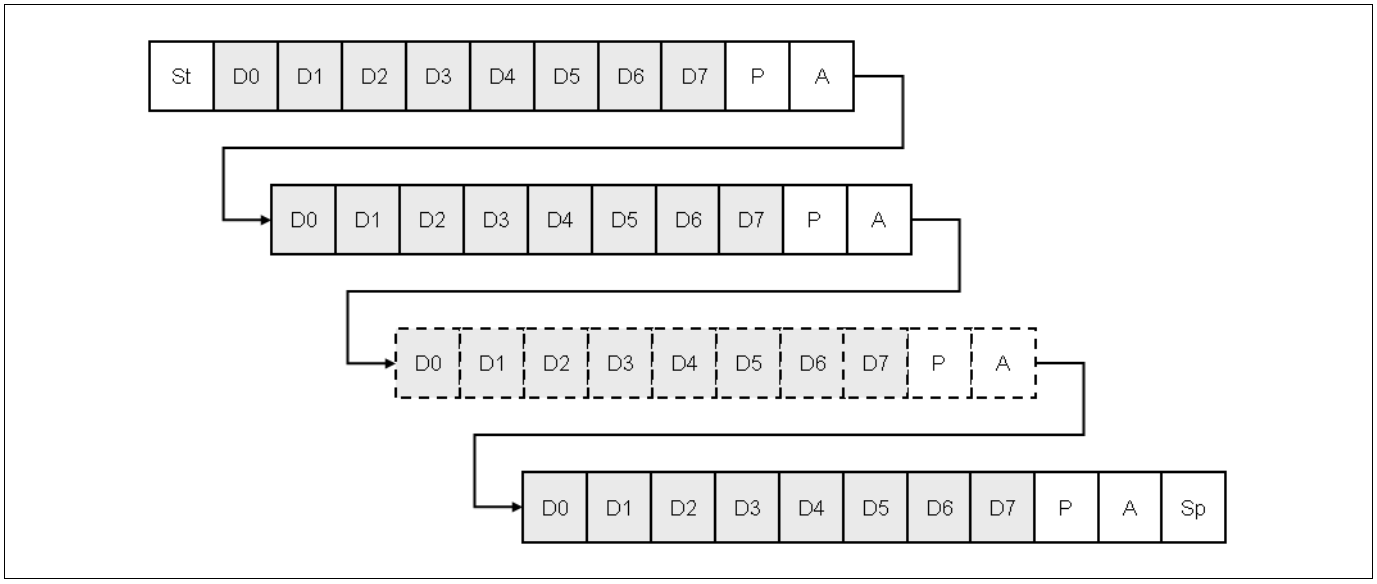


Figure 14.2 10-bit Transmission Packet

14.2.2 Packet Transmission Timing

14.2.2.1 Data Transfer

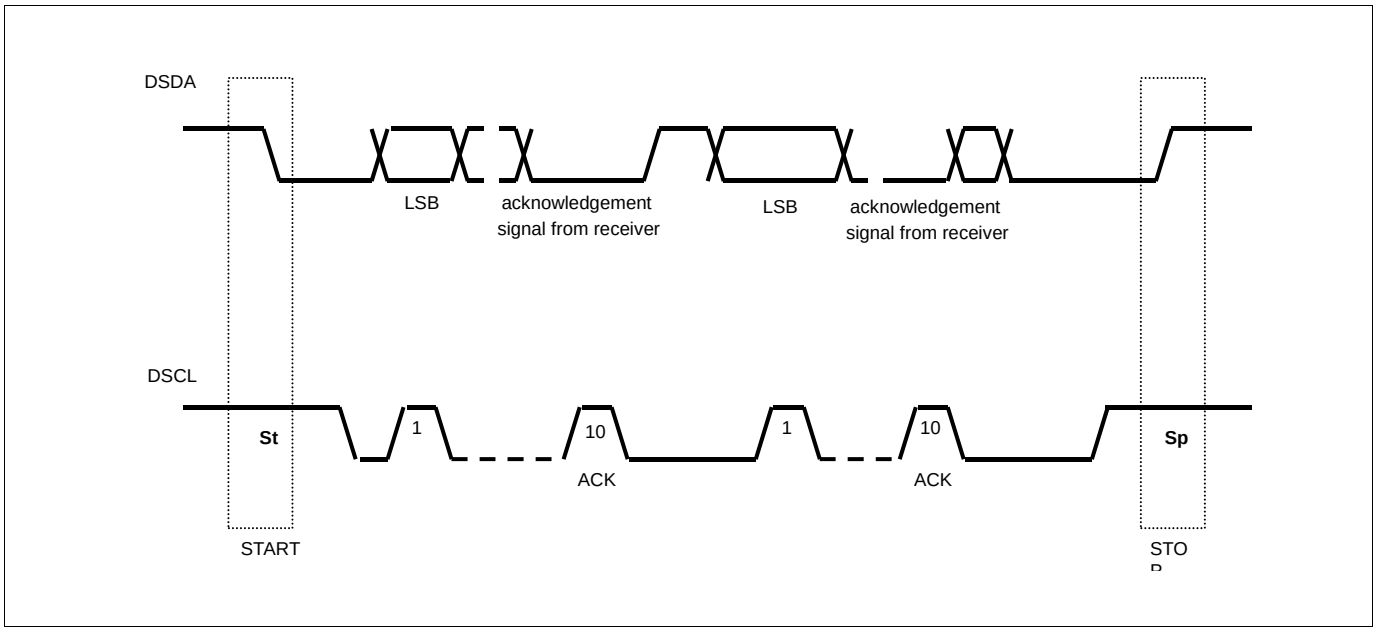


Figure 14.3 Data Transfer on the Twin Bus

14.2.2.2 Bit Transfer

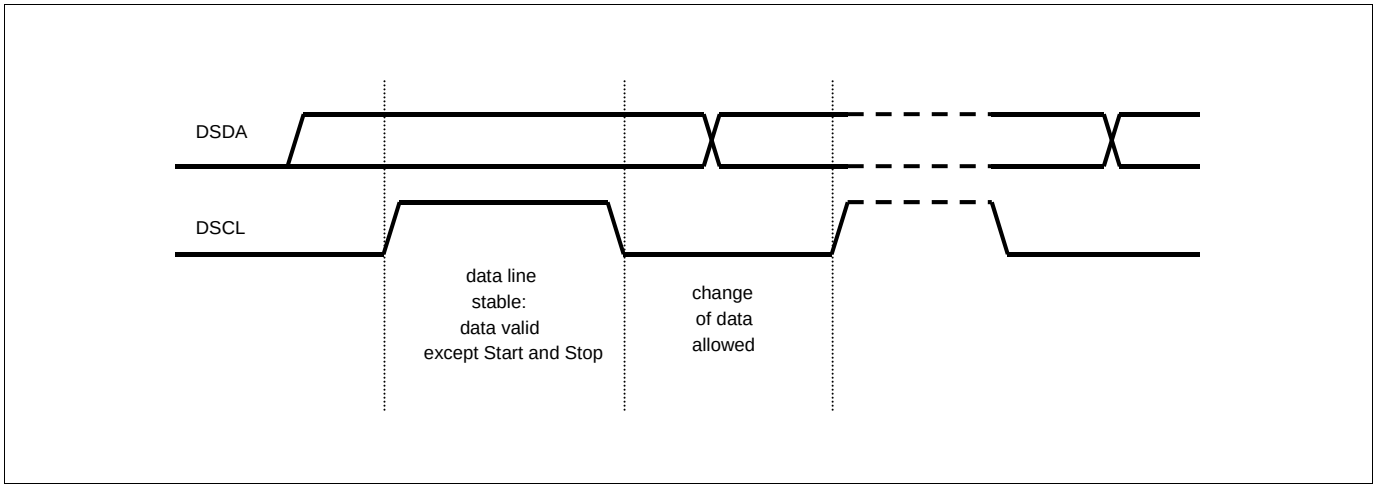


Figure 14.4 Bit Transfer on the Serial Bus

14.2.2.3 Start and Stop Condition

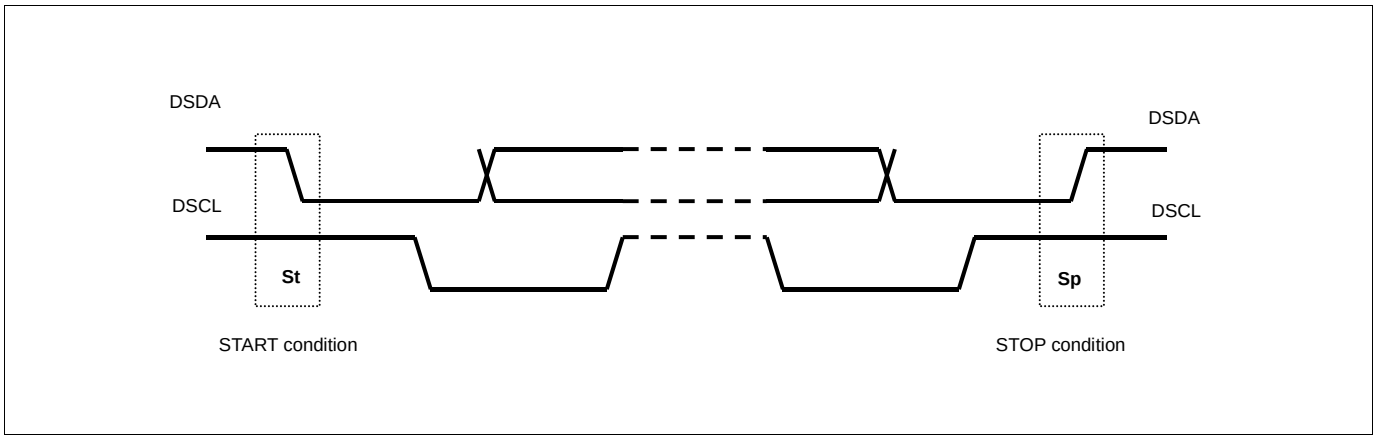


Figure 14.5 Start and Stop Condition

14.2.2.4 Acknowledge Bit

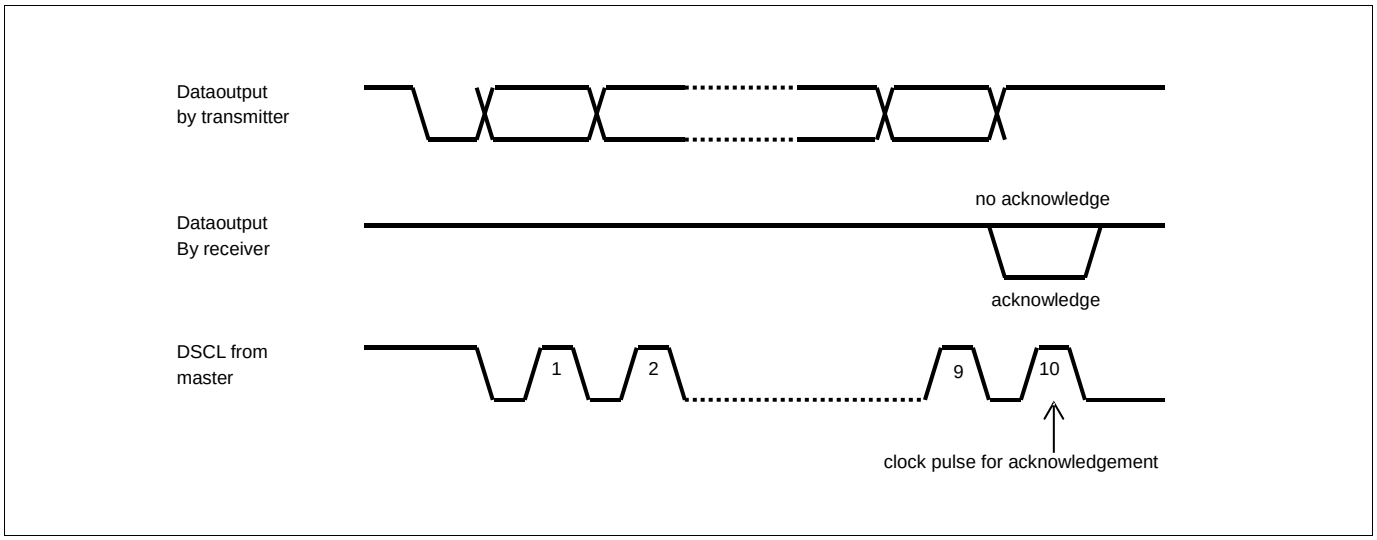


Figure 14.6 Acknowledge on the Serial Bus

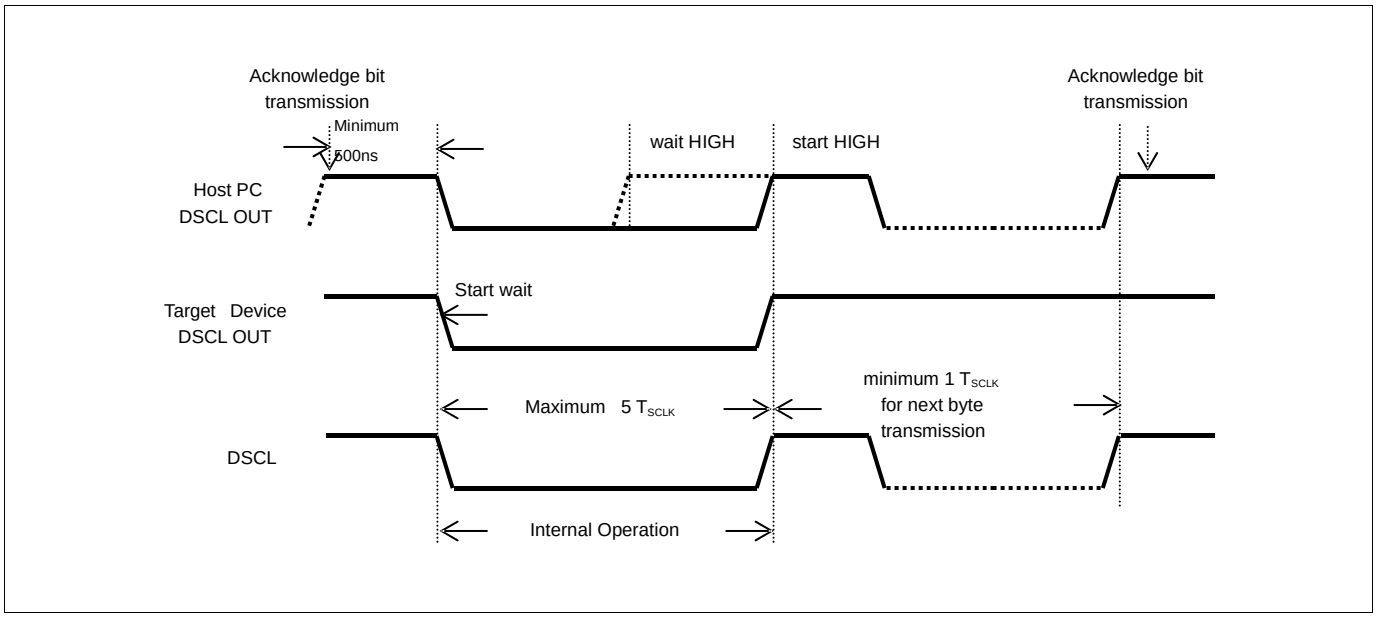


Figure 14.7 Clock Synchronization during Wait Procedure

14.2.3 Connection of Transmission

Two-pin interface connection uses open-drain(wire-AND bidirectional I/O).

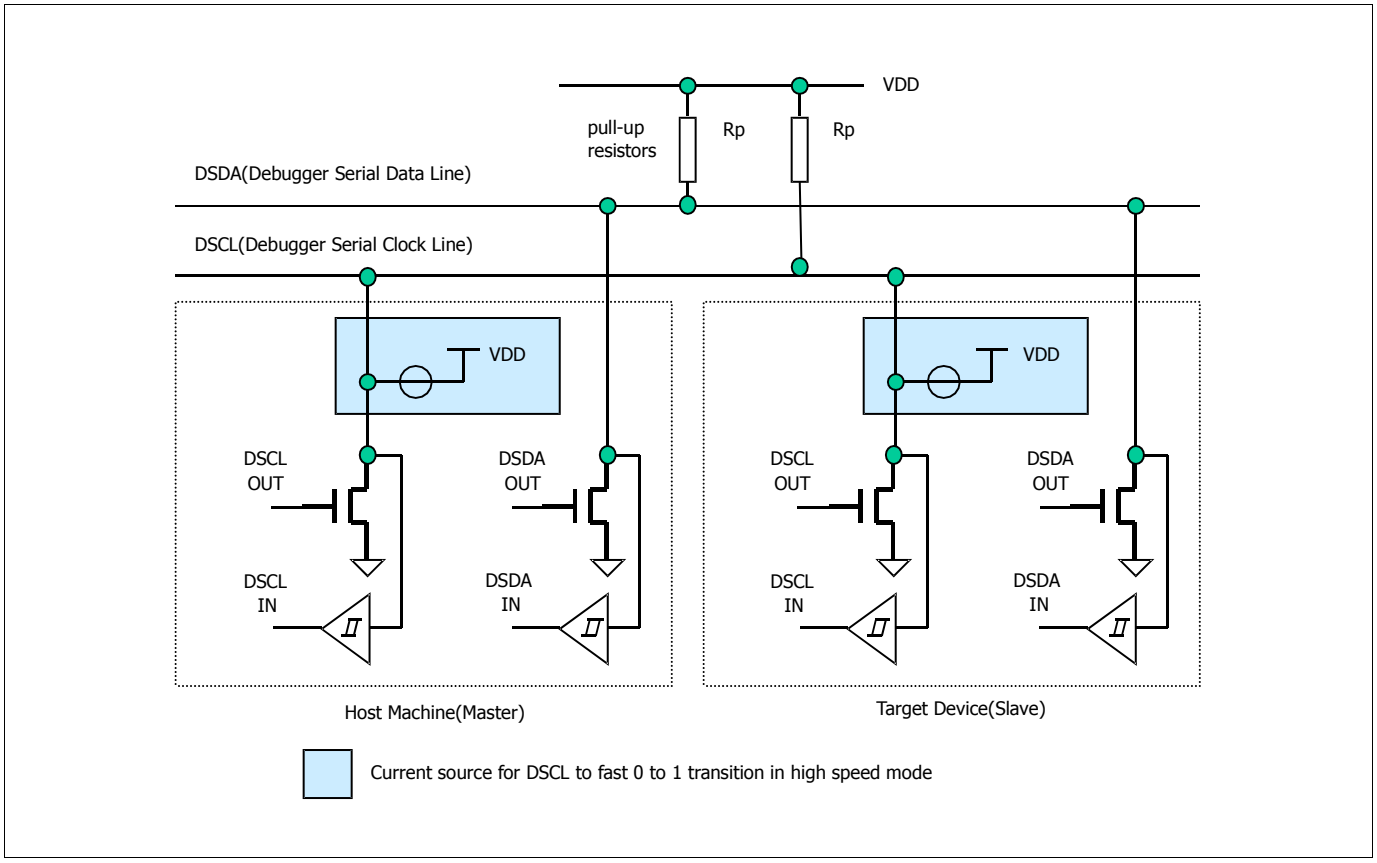


Figure 14.8 Connection of Transmission

15 Flash Memory

15.1 Overview

15.1.1 Description

MC96F6508A incorporates flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory can be read by 'MOVC' instruction and it can be programmed in OCD, serial ISP mode or user program mode.

- Flash Size : 8Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory

NOTE) The RXE bit of UARTCR2 register should be disabled before flash memory erase and write start.

15.1.2 Flash Program ROM Structure

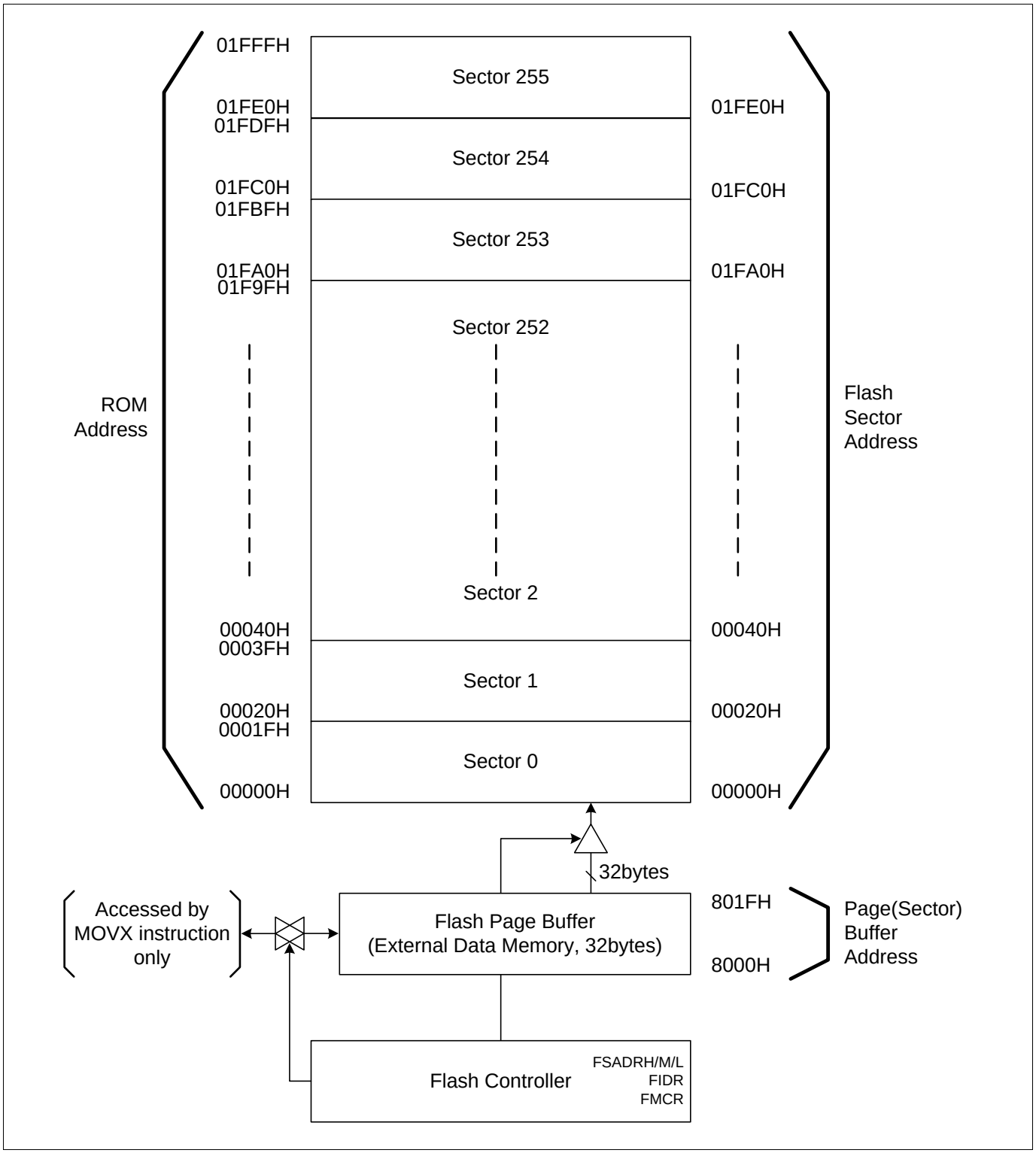


Figure 15.1 Flash Program ROM Structure

15.1.3 Register Map

Name	Address	Dir	Default	Description
FSADRH	FAH	R/W	00H	Flash Sector Address High Register
FSADRM	FBH	R/W	00H	Flash Sector Address Middle Register
FSADRL	FCH	R/W	00H	Flash Sector Address Low Register
FIDR	FDH	R/W	00H	Flash Identification Register
FMCR	FEH	R/W	00H	Flash Mode Control Register

Table 15-1. Flash Memory Register Map

15.1.4 Register Description for Flash Memory Control and Status

Flash control register consists of the flash sector address high register (FSADRH), flash sector address middle register (FSADRM), flash sector address low register (FSADRL), flash identification register (FIDR), and flash mode control register (FMCR). They are mapped to SFR area and can be accessed only in programming mode.

15.1.5 Register Description for Flash

FSADRH (Flash Sector Address High Register) : FAH

7	6	5	4	3	2	1	0
–	–	–	–	FSADRH3	FSADRH2	FSADRH1	FSADRH0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value :00H

FSADRH[3:0] Flash Sector Address High

FSADRM (Flash Sector Address Middle Register) :FBH

7	6	5	4	3	2	1	0
FSADRM7	FSADRM6	FSADRM5	FSADRM4	FSADRM3	FSADRM2	FSADRM1	FSADRM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

FSADRM[7:0] Flash Sector Address Middle

FSADRL (Flash Sector Address Low Register) :FCH

7	6	5	4	3	2	1	0
FSADRL7	FSADRL6	FSADRL5	FSADRL4	FSADRL3	FSADRL2	FSADRL1	FSADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

FSADRL[7:0] Flash Sector Address Low

FIDR (Flash Identification Register) :FDH

7	6	5	4	3	2	1	0
FIDR7	FIDR6	FIDR5	FIDR4	FIDR3	FIDR2	FIDR1	FIDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value :00H

FIDR[7:0] Flash Identification

Others No identification value

10100101 Identification value for a flash mode

(These bits are automatically cleared to logic ‘00H’ immediately after one time operation except “flash page buffer reset mode”)

FMCR (Flash Mode Control Register) :FEH

7	6	5	4	3	2	1	0
FMBUSY	–	–	–	–	FMCR2	FMCR1	FMCR0
R	–	–	–	–	R/W	R/W	R/W

Initial value :00H

FMBUSY Flash Mode Busy Bit. This bit will be used for only debugger.

0 No effect when “1” is written

1 Busy

FMCR[2:0] Flash Mode Control Bits. During a flash mode operation, the CPU is hold and the global interrupt is on disable state regardless of the IE.7 (EA) bit.

FMCR2	FMCR1	FMCR0	Description
0	0	1	Select flash page buffer reset mode and start regardless of the FIDR value (Clear all 32bytes to ‘0’)
0	1	0	Select flash sector erase mode and start operation when the FIDR=”10100101b’
0	1	1	Select flash sector write mode and start operation when the FIDR=”10100101b’
1	0	0	Select flash sector Code Write Protection and start operation when the FIDR=”10100101b’

Others Values: No operation

(These bits are automatically cleared to logic ‘00H’ immediately after one time operation)

15.1.6 Serial In-System Program (ISP) Mode

Serial in-system program uses the interface of debugger which uses two wires. Refer to chapter 14 in details about debugger

15.1.7 Protection Area (User program mode)

MC96F6508A can program its own flash memory (protection area). The protection area can not be erased or programmed. The protection areas are available only when the PAEN bit is cleared to '0', that is, enable protection area at the configure option 2 if it is needed. If the protection area isn't enabled (PAEN ='1'), this area can be used as a normal program memory.

The size of protection area can be varied by setting of configure option 2.

Protection Area Size Select		Size of Protection Area	Address of Protection Area
PASS1	PASS0		
0	0	3.7Kbytes	0100H – 0FFFH
0	1	1.7Kbytes	0100H – 07FFH
1	0	768bytes	0100H – 03FFH
1	1	256bytes	0100H – 01FFH

Table 15-2. Protection Area size

NOTE)

1. Refer to chapter 16 in configure option control.

15.1.8 Erase Mode

The sector erase program procedure in user program mode

1. Page buffer clear (FMCR=0x01)
2. Write '0' to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work(Note).
6. Set flash mode control register (FMCR).
7. Erase verify

NOTE)

1. Please refer to the chapter "Protection for Invalid Erase/Write"
2. On flash memory erase and write, it should be disabled the RXE bit of UARTCR2 register.

Program Tip – sector erase

```
            ANL     EO,#0xF8              ;Set DPTR0
            MOV     FMCR,#0x01            ;page buffer clear
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            MOV     A,#0
            MOV     R0,#SectorSize        ;Sector size of Device
            MOV     DPH,#0x80             ;Page Buffer Address is 8000H
            MOV     DPL,#0

Pgbuf_clr:
            MOVX    @DPTR,A
            INC     DPTR
            DJNZ    R0,Pgbuf_clr          ;Write '0' to all page buffer

            MOV     FSADRH,#SAH           ;Sector Address High Byte.
            MOV     FSADRM,#SAM           ;Sector Address Middle Byte
            MOV     FSADRL,#SAL           ;Sector Address Low Byte
            MOV     FIDR,#0xA5            ;Identification value

            MOV     A,#ID_DATA_1          ;Check the UserID(written by user)
            CJNE    A,UserID1,No_WriteErase;This routine for UserID must be needed.
            MOV     A,#ID_DATA_2
            CJNE    A,UserID2,No_WriteErase

            MOV     FMCR,#0x02            ;Start flash erase mode
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            LJMP    Erase_verify
            ---
No_WriteErase:
            MOV     FIDR,#00H
            MOV     UserID1,#00H
            MOV     UserID2,#00H
            ---
Erase_verify:
            ---
Verify_error:
            ---
```

15.1.9 Write Mode

The sector Write program procedure in user program mode

1. Page buffer clear (FMCR=0x01)
2. Write data to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work(Note1).
6. Set flash mode control register (FMCR).
7. Erase verify

NOTE)

1. Please refer to the chapter “Protection for Invalid Erase/Write”.
2. All data of the sector should be “00H” before writing data to a sector.
3. On flash memory erase and write, it should be disabled the RXE bit of UARTCR2 register.

Program Tip – sector write

```
            ANL     EO,#0xF8              ;Set DPTR0
            MOV     FMCR,#0x01            ;page buffer clear
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            MOV     A,#0
            MOV     R0,#SectorSize        ;Sector size of Device
            MOV     DPH,#0x80             ;Page Buffer Address is 8000H
            MOV     DPL,#0

Pgbuf_WR:   MOVX    @DPTR,A
            INC     A
            INC     DPTR
            DJNZ    R0,Pgbuf_WR           ;Write data to all page buffer

            MOV     FSADRH,#SAH           ;Sector Address High Byte.
            MOV     FSADRM,#SAM           ;Sector Address Middle Byte
            MOV     FSADRL,#SAL           ;Sector Address Low Byte
            MOV     FIDR,#0xA5            ;Identification value

            MOV     A,#ID_DATA_1          ;Check the UserID(written by user)
            CJNE    A,UserID1,No_WriteErase;This routine for UserID must be needed.
            MOV     A,#ID_DATA_2
            CJNE    A,UserID2,No_WriteErase

            MOV     FMCR,#0x03            ;Start flash write mode
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            LJMP    Write_verify
            ---
No_WriteErase:
            MOV     FIDR,#00H
            MOV     UserID1,#00H
            MOV     UserID2,#00H
            ---
Write_verify:
            ---
Verify_error:
            ---
```

The Byte Write program procedure in user program mode

1. Page buffer clear (FMCR=0x01)
2. Write data to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work(Note1).
6. Set flash mode control register (FMCR).
7. Erase verify

NOTE)

1. Please refer to the chapter “Protection for Invalid Erase/Write”.
2. Data of the address should be “00H” before writing data to an address.
3. On flash memory erase and write, it should be disabled the RXE bit of UARTCR2 register.

Program Tip – byte write

```
            ANL     EO,#0xF8              ;Set DPTR0
            MOV     FMCR,#0x01            ;page buffer clear
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            MOV     A,#5
            MOV     DPH,#0x80
            MOV     DPL,#0
            MOVX    @DPTR,A         ;Write data to page buffer

            MOV     A,#6
            MOV     DPH,#0x80
            MOV     DPL,#0x05
            MOVX    @DPTR,A         ;Write data to page buffer

            MOV     FSADRH,#SAH           ;Sector Address High Byte.
            MOV     FSADRM,#SAM           ;Sector Address Middle Byte
            MOV     FSADRL,#SAL           ;Sector Address Low Byte
            MOV     FIDR,#0xA5            ;Identification value

            MOV     A,#ID_DATA_1          ;Check the UserID(written by user)
            CJNE    A,UserID1,No_WriteErase;This routine for UserID must be needed.
            MOV     A,#ID_DATA_2
            CJNE    A,UserID2,No_WriteErase

            MOV     FMCR,#0x03            ;Start flash write mode
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.
            NOP                           ;Dummy instruction, This instruction must be needed.

            LJMP    Write_verify
            ---
No_WriteErase:
            MOV     FIDR,#00H
            MOV     UserID1,#00H
            MOV     UserID2,#00H
            ---
Write_verify:
            ---
Verify_error:
            ---
```

15.1.10 Protection for Invalid Erase/Write

It should be taken care to the flash erase/write programming in code.

You must make preparations for invalid jump to the flash erase/write code by malfunction, noise, and power off.

NOTE) For more information, please refer to the appendix “Flash Protection for Invalid Erase/Write”.

1. User ID check routine for the flash erase/write code.

```
ErWt_rtn:
      ---
      MOV     FIDR,#10100101B       ;ID Code
      MOV     A,#ID_DATA_1          ;Ex) ID_DATA_1: 93H, ID_DATA_2: 85H, ID_DATA_3: 5AH
      CJNE    A,UserID1,No_WriteErase
      MOV     A,#ID_DATA_2
      CJNE    A,UserID2,No_WriteErase
      MOV     A,#ID_DATA_3
      CJNE    A,UserID3,No_WriteErase
      MOV     FMCR,#0x??            ;0x03 if write, 0x02 if erase
      ---
      ---
      RET

No_WriteErase:
      MOV     FIDR,#00H
      MOV     UserID1,#00H
      MOV     UserID2,#00H
      MOV     UserID3,#00H
      MOV     Flash_flag,#00H
      RET
```

If code is like the above lines, an invalid flash erase/write can be avoided.

NOTE) On flash memory erase and write, it should be disabled the RXE bit of UARTCR2 register.

2. It is important where the UserID1/2/3 is written. It will be remain the invalid flash erase/write problem if the UserID1/2/3 is written at the above line of the instruction ″MOV FIDR,#10100101B″. So. It had better writing the UserID1/2/3 in another routine after return.

```
Decide_ErWt:
      ---
      MOV     Flash_flag1,#38H   ;Random value for example, in case of erase/write needs
      MOV     FSADRL,#20H        ;Here 20H is example,
      MOV     Flash_flag2,#75H
      RET
```

3. The flash sector address (FSADRH/FSADRM/FSADRL) should always keep the address of the flash which is used for data area. For example, The FSADRH/FSADRM is always 0x00/0x1f″ if 0x1f00 to 0x1fff is used for data.

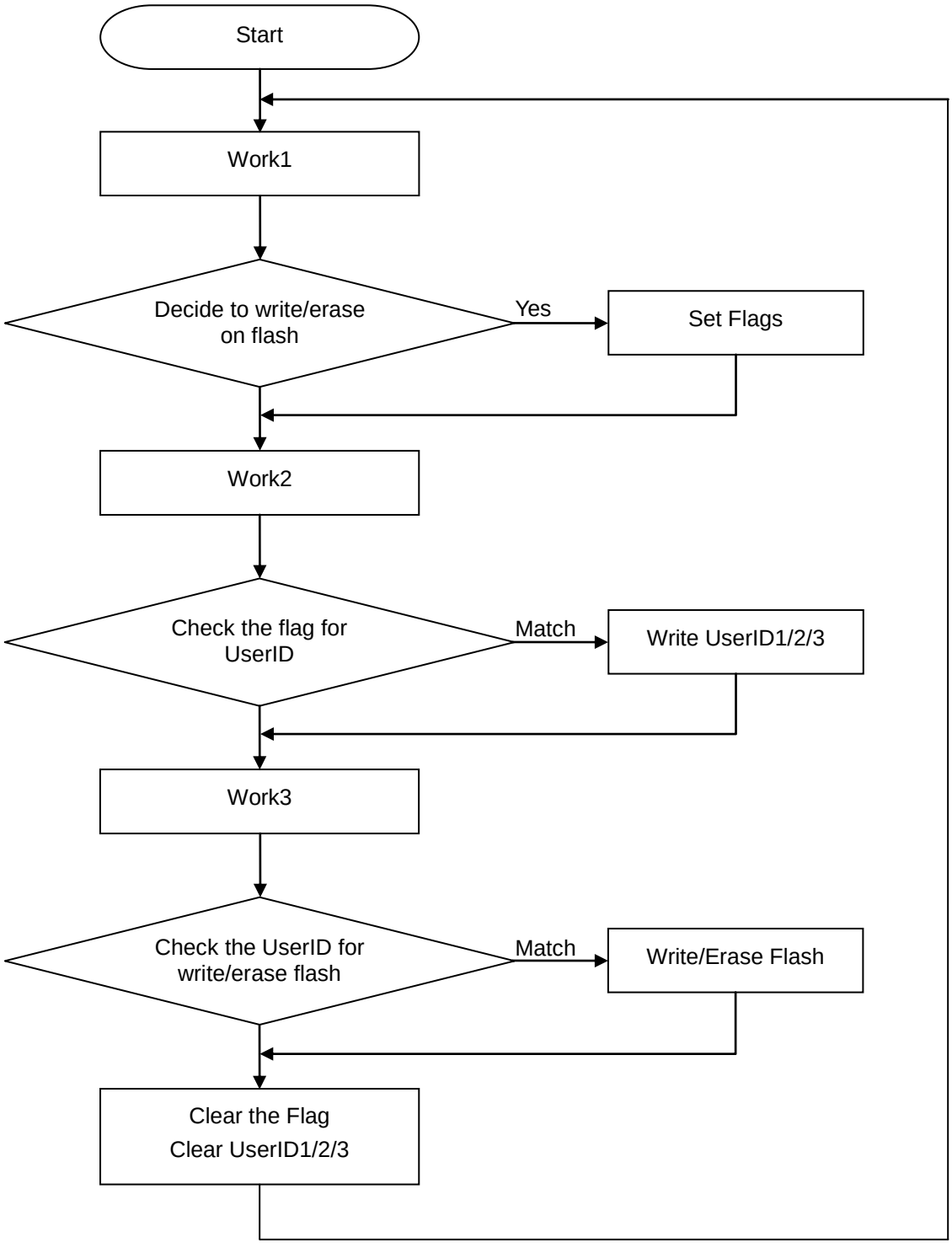
4. Overview of main

```
      ---
      CALL    Work1
      CALL    Decide_ErWt
      CALL    Work2
      CALL    ID_write
      CALL    Work3
      CALL    Flash_erase
      CALL    Flash_write
      ---
      ---
      ---

ID_write:
      MOV     A,#38H
      CJNE    A,Flash_flag1,No_write_ID
      MOV     A,#75H
      CJNE    A,Flash_flag2,No_write_ID
      MOV     UserID1,#ID_DATA_1      ;Write User ID1
      MOV     A,#38H
      CJNE    A,Flash_flag1,No_write_ID
      MOV     A,#75H
      CJNE    A,Flash_flag2,No_write_ID
      MOV     UserID2,#ID_DATA_2      ;Write User ID2
      MOV     A,#38H
      CJNE    A,Flash_flag1,No_write_ID
      MOV     A,#75H
      CJNE    A,Flash_flag2,No_write_ID
      MOV     UserID3,#ID_DATA_3      ;Write User ID3
      RET

No_write_ID:
      MOV     UserID1,#00H
      MOV     UserID2,#00H
      MOV     UserID3,#00H
      RET
```

15.1.10.1 Flow of Protection for Invalid Erase/Write



NOTE)

1. This method is helpful to reduce the case for flash memory to be erased by malfunction, noise and power off.

Figure 15.2 Flow of Protection for Invalid Erase/Write

15.1.11 Read Mode

The Reading program procedure in user program mode

1. Load receive data from flash memory on MOVC instruction by indirectly addressing mode.

Program Tip – reading

```
MOV     A,#0
MOV     DPH,#0x1F
MOV     DPL,#0xA0       ;flash memory address

MOVC    A,@A+DPTR       ;read data from flash memory
```

15.1.12 Code Write Protection Mode

The Code Write Protection program procedure in user program mode

1. Set flash identification register (FIDR).
2. Check the UserID for to prevent the invalid work(Note).
3. Set flash mode control register (FMCR).

NOTE) Please refer to the chapter “Protection for Invalid Erase/Write”

Program Tip – Code Write Protection

```
            MOV     FIDR,#0xA5              ;Identification value

            MOV     A,#ID_DATA_1            ;Check the UserID(written by user)
            CJNE    A,UserID1,No_WriteErase;This routine for UserID must be needed.
            MOV     A,#ID_DATA_2
            CJNE    A,UserID2,No_WriteErase

            MOV     FMCR,#0x04              ;Start flash Code Write Protection mode
            NOP                             ;Dummy instruction, This instruction must be needed.
            NOP                             ;Dummy instruction, This instruction must be needed.
            NOP                             ;Dummy instruction, This instruction must be needed.

No_WriteErase:
            MOV     FIDR,#00H
            MOV     UserID1,#00H
            MOV     UserID2,#00H
            ---
```

16 Configure Option

16.1 Configure Option Control

The data for configure option should be written in the configure option area (001EH – 001FH) by programmer (Writer tools).

CONFIGURE OPTION 1 :ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	VAPEN	–	–	–	–	RSTS

Initial value :00H

R_P Code Read Protection
- 0 Disable
- 1 Enable

HL Code Write Protection
- 0 Disable
- 1 Enable

VAPEN Vector Area(00H – FFH) Write Protection
- 0 Disable Protection (Erasable by instruction)
- 1 Enable Protection (Not erasable by instruction)

RSTS Select RESETB pin
- 0 Disable RESETB pin(P62)
- 1 Enable RESETB pin

CONFIGURE OPTION 2 :ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	–	PAEN	PASS1	PASS0

Initial value :00H

PAEN Enable Specific Area Write Protection
- 0 Disable Protection (Erasable by instruction)
- 1 Enable Protection (Not erasable by instruction)

PASS [1:0] Select Specific Area for Write Protection

NOTE)

1. When PAEN = '1', it is applied.

PASS1	PASS0	Description
0	0	3.7Kbytes (Address 0100H – 0FFFH)
0	1	1.7 Kbytes (Address 0100H – 07FFH)
1	0	768 bytes (Address 0100H – 03FFH)
1	1	256 bytes (Address 0100H – 01FFH)

17 APPENDIX

17.1 Instruction Table

Instructions are either1, 2 or 3 bytes long as listed in the 'Bytes' column below.

Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,directjne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediatejne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

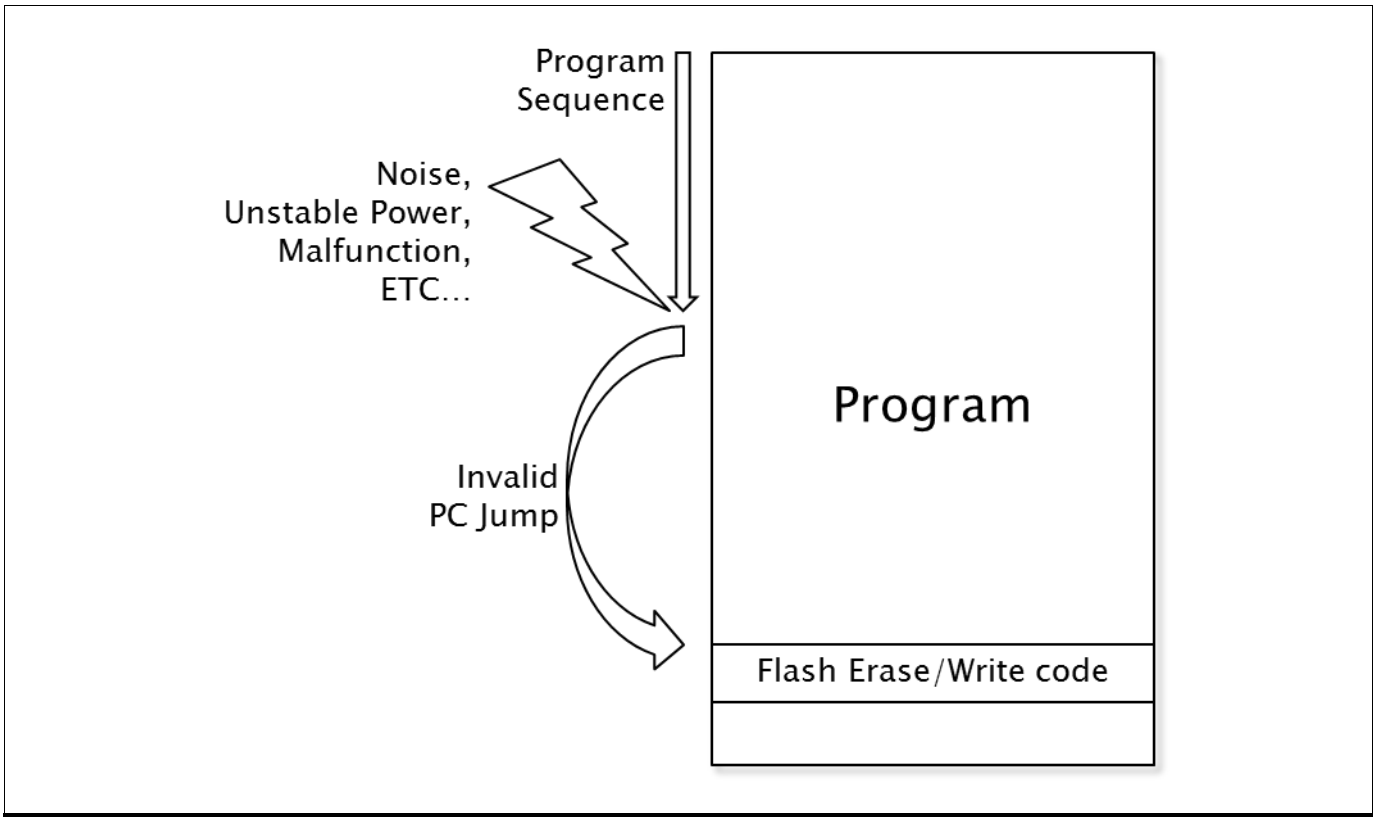
In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

17.2 Flash Protection for Invalid Erase/Write

➢ Overview

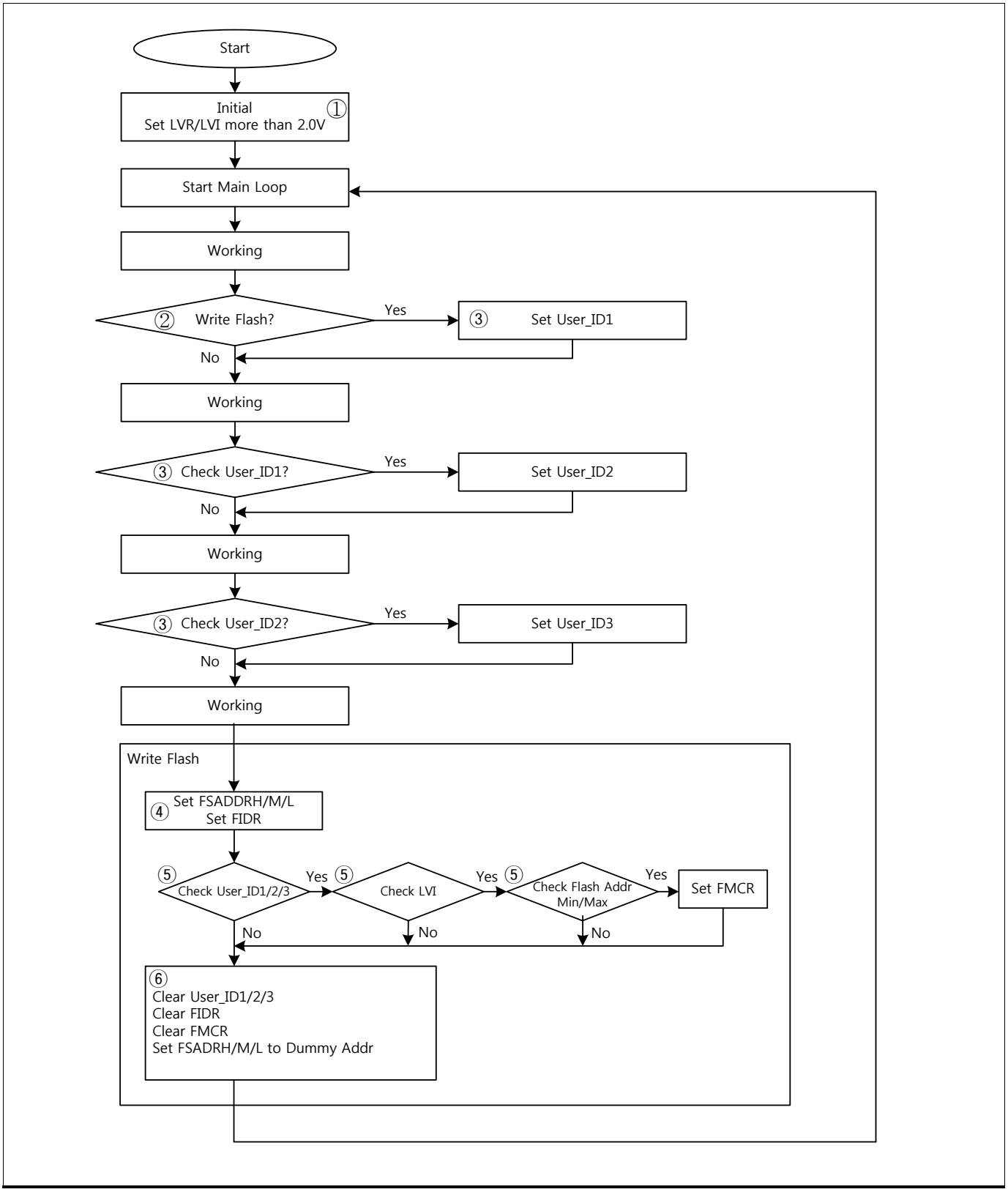
This is example to prevent changing code or data in flash by abnormal operation(noise, unstable power, malfunction, etc…).



➢ How to protect the flash

- Divide into decision and execution to Erase/Write in flash.
  - Check the program sequence from decision to execution in order of precedence about Erase/Write.
  - Setting the flags in program and check the flags in main loop at the end
  - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
  - If the flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
  - Set the flash sector address to dummy address in usually run time.
  - Change the flash sector address to real area range shortly before Erase/Write.
  - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in flash.
- Use the LVR/LVI
  - Unstable or low powers give an adverse effect on MCU. So use the LVR/LVI

➢ Flowchart


Start
Initial
Set LVR/LVI more than 2.0V ①
Start Main Loop
Working
② Write Flash?
Yes
③ Set User_ID1
No
Working
③ Check User_ID1?
Yes
Set User_ID2
No
Working
③ Check User_ID2?
Yes
Set User_ID3
No
Working
Write Flash
④ Set FSADDRH/M/L
Set FIDR
⑤ Check User_ID1/2/3
Yes
⑤ Check LVI
Yes
⑤ Check Flash Addr Min/Max
Yes
Set FMCR
No
No
No
⑥
Clear User_ID1/2/3
Clear FIDR
Clear FMCR
Set FSADRH/M/L to Dummy Addr

➢ Descript of Flowchart

- ① Initialization
  - Set the LVR/LVI
    Check the power by LVR/LVI and do not execute under unstable or low power.
  - Initialize User_ID1/2/3
  - Set Flash Sector Address High/Middle/Low to Dummy address
    Dummy address is set to unused area range in flash.
- ② Decide to Write
  - When the Erase/Write are determined, set flag. Do not directly Erase/Write in flash.
  - Make the user data.
- ③ Check and Set User_ID1/2/3
  - In the middle of source, insert code which can check and set the flags.
  - By setting the User_ID 1/2/3 sequentially and identify the flow of the program.
- ④ Set Flash Sector Address
  - Set address to real area range shortly before Erase/Write in flash.
    Set to Dummy address after Erase/Write
    Even if invalid work occurred, it will be Erase/Write in Dummy address in flash.
- ⑤ Check Flags
  - If every flag(User_ID1/2/3, LVI, Flash Address Min/Max) was set, than do Erase/Write.
  - If the Flash Sector Address is outside of Min/Max, do not execute
  - Address Min/Max is set to unused area.
- ⑥ Initialize Flags
  - Initialize User_ID1/2/3
  - Set Flash Sector Address to Dummy Address
- Sample Source
  - Refer to the ABOV homepage.
  - It is created based on the MC97F2664.
  - Each product should be modified according to the Page Buffer Size and Flash Size

➢ Etc

- Protection by Configure option
  - Set flash protection by MCU Write Tool(OCD, PGM+, etc…)
    Vector Area :
    00H~FFH
    Specific Area :
    3.7k Bytes (Address 0100H – 0FFFH)
    1.7k Bytes (Address 0100H – 07FFH)
    768 Bytes (Address 0100H – 03FFH)
    256 Bytes (Address 0100H – 01FFH)
  - The range of protection may be different each product.

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